

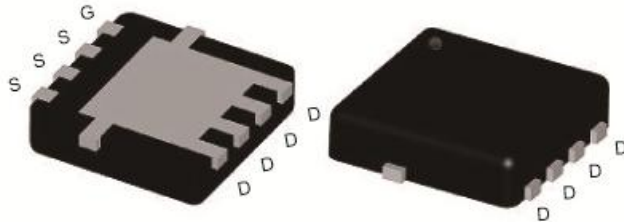
GENERAL DESCRIPTION

The ME7824CS-G is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where Low-side switching , and low in-line power loss are needed in a very small outline surface mount package.

PIN CONFIGURATION

DFN(S) 3X3

Top View

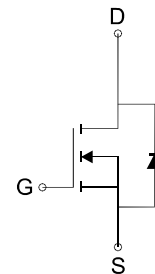


FEATURES

- $R_{DS(ON)}$: 1.8 m Ω (typ.) @ $V_{GS}=10V$
- $R_{DS(ON)}$: 2.6 m Ω (typ.) @ $V_{GS}=4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- Halogen free

APPLICATIONS

- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch



N-Channel MOSFET

Ordering Information: ME7824CS-G (Green product-Halogen free)

Absolute Maximum Ratings (TA=25°C Unless Otherwise Noted)

Parameter		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current*	$T_C=25^\circ C$	I_D	88.8	A
	$T_C=70^\circ C$		71.1	
	$T_A=25^\circ C$		27.4	
	$T_A=70^\circ C$		21.9	
Pulsed Drain Current		I_{DM}	266.6	A
Maximum Power Dissipation*	$T_C=25^\circ C$	P_D	29	W
	$T_C=70^\circ C$		18.6	
	$T_A=25^\circ C$		2.7	
	$T_A=70^\circ C$		1.7	
Operating Junction Temperature		T_J	150	$^\circ C$
Storage Temperature Range		T_{stg}	-55 to 150	$^\circ C$
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	45	$^\circ C/W$
Thermal Resistance-Junction to Case*		$R_{\theta JC}$	4.3	

*The device mounted on 1in² FR4 board with 2 oz copper

*Chip silicon limitation current is 100A

Electrical Characteristics (T_A=25°C Unless Otherwise Specified)

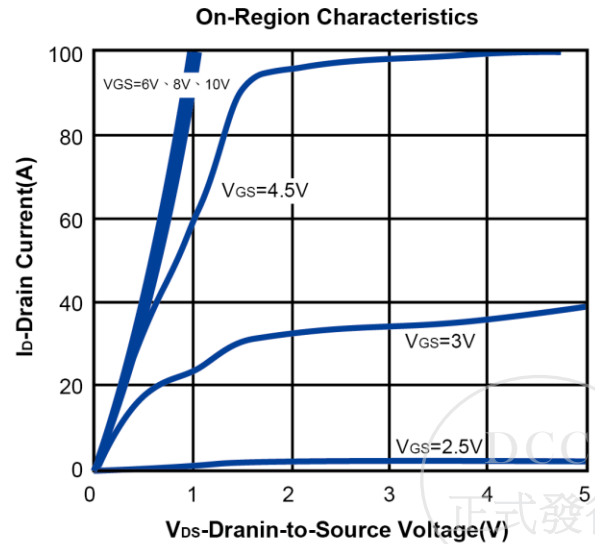
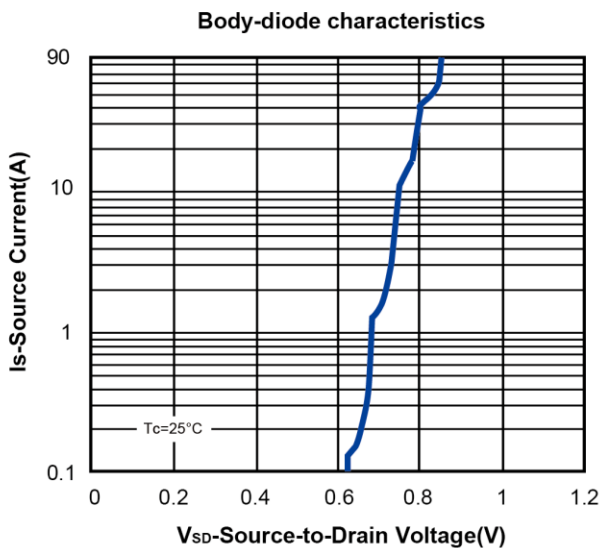
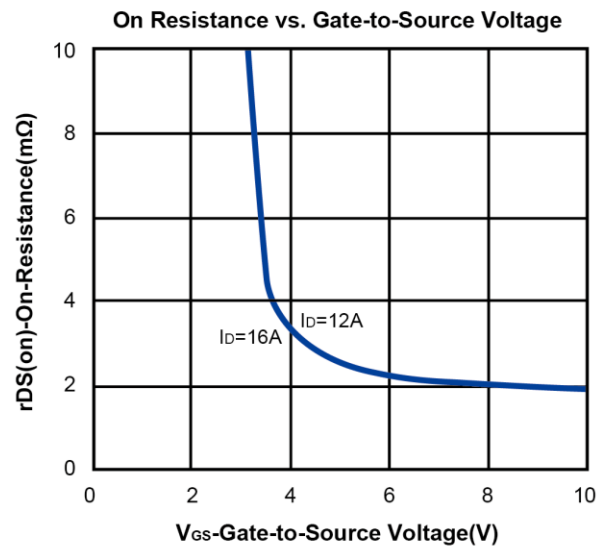
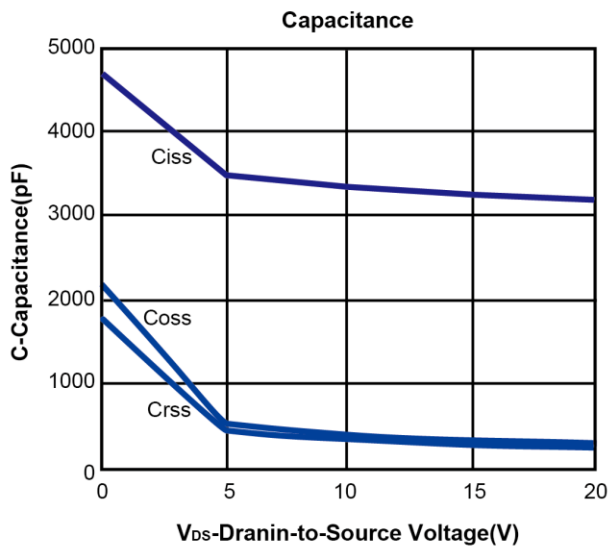
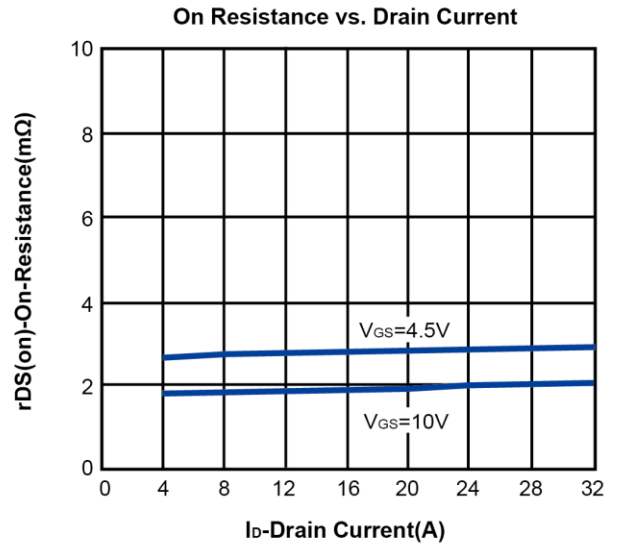
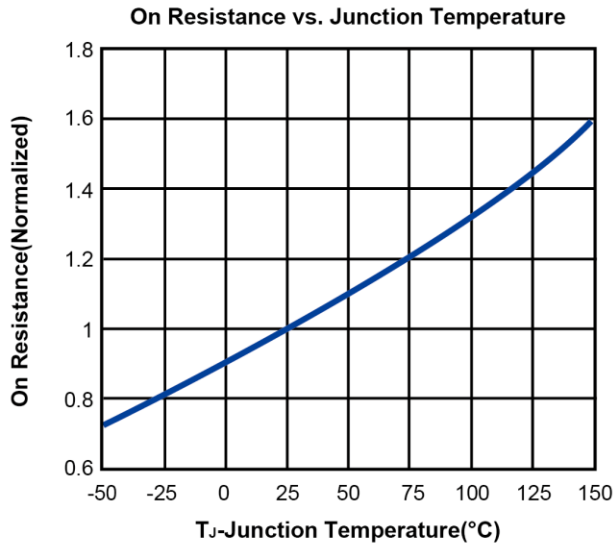
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
STATIC						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	30			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1		3	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±20V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V			1	μA
R _{DS(ON)}	Drain-Source On-State Resistance ^a	V _{GS} =10V, I _D =16A		1.8	2.3	mΩ
		V _{GS} =4.5V, I _D =12A		2.6	3.4	
V _{SD}	Diode Forward Voltage	I _S =1.0A, V _{GS} =0V			1	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DS} =15V, V _{GS} =10V, I _D =16A		66.1		nC
Q _g	Total Gate Charge	V _{DS} =15V, V _{GS} =4.5V, I _D =16A		31.9		
Q _{gs}	Gate-Source Charge			11.3		
Q _{gd}	Gate-Drain Charge			12.8		
C _{iss}	Input Capacitance	V _{DS} =15V, V _{GS} =0V, F=1MHz		3280		pF
C _{oss}	Output Capacitance			356		
C _{rss}	Reverse Transfer Capacitance			303		
t _{d(on)}	Turn-On Delay Time	V _{DS} =15V, R _L =0.938Ω V _{GS} =10V, R _G =3Ω		10.1		ns
t _r	Turn-On Rise Time			52.1		
t _{d(off)}	Turn-Off Delay Time			48.8		
t _f	Turn-Off Fall Time			21.1		
Single pulse Avalanche Energy						
Single pulse Avalanche Energy L=0.1mH		I _{AS}	28.1			A
Single pulse Avalanche Energy L=0.1mH		E _{AS}	40			mJ

Note: a. Pulse test: pulse width ≤ 300us, duty cycle ≤ 2%, Guaranteed by design, not subject to production testing.

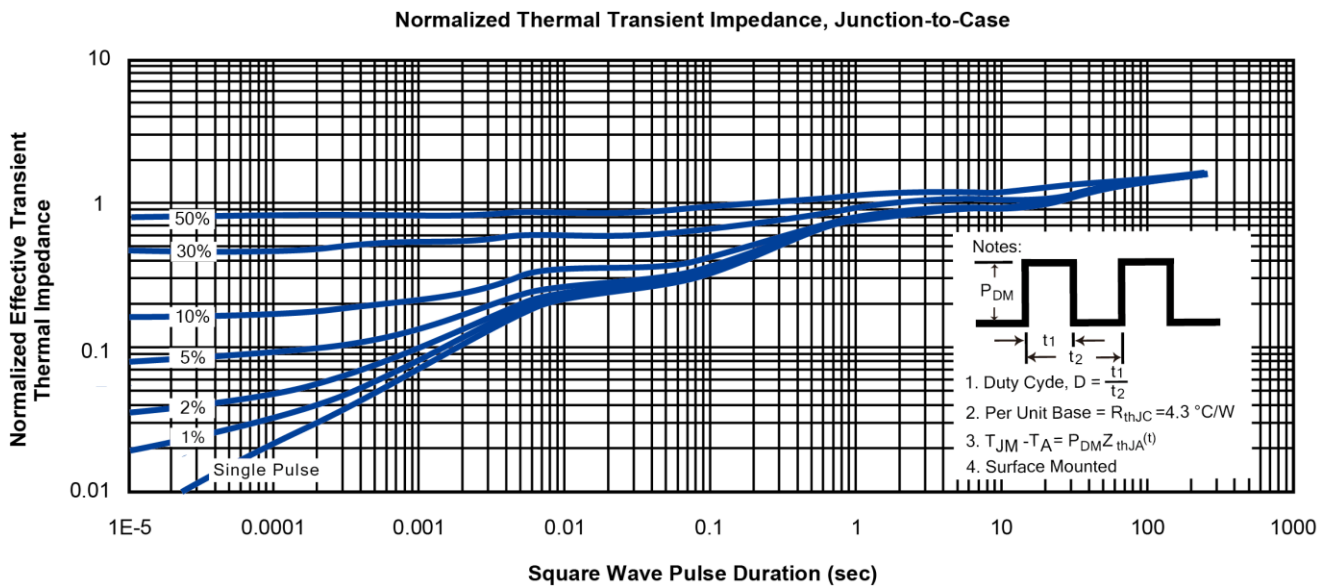
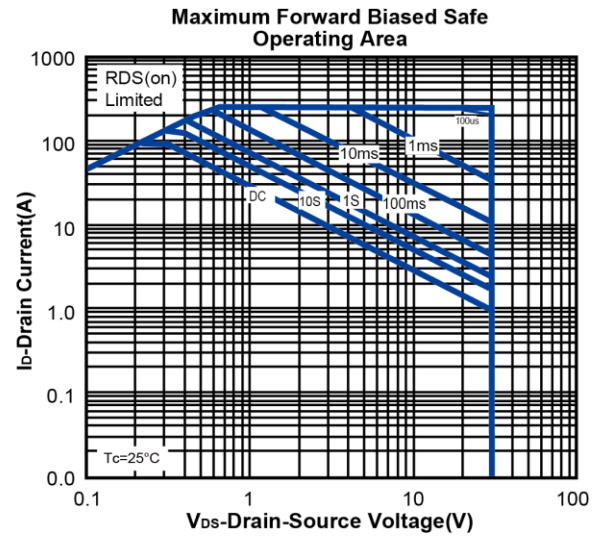
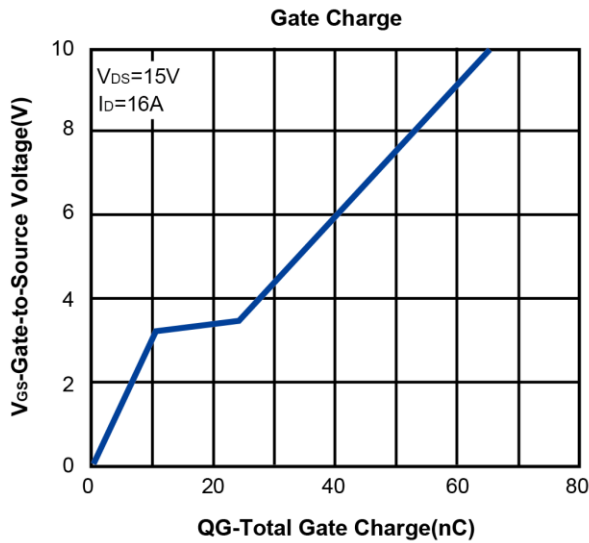
b. Force mos reserves the right to improve or change product design, functions, reliability, qualified manufacturer without notice.



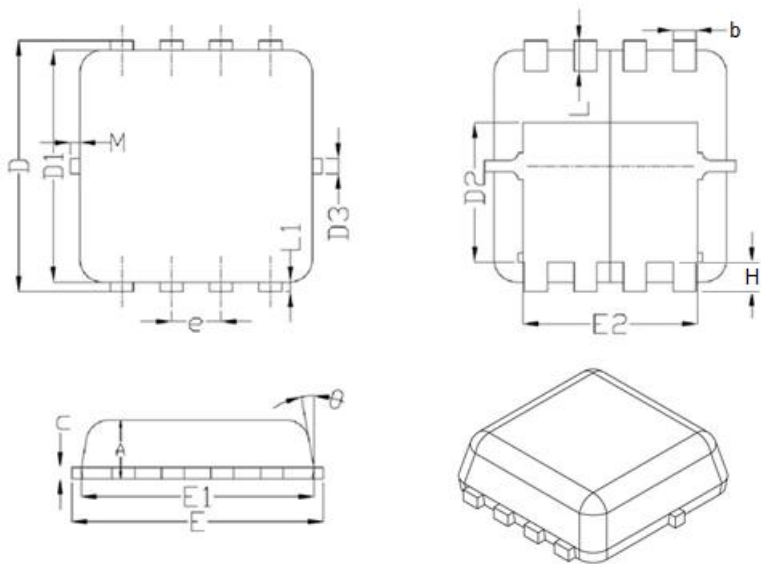
Typical Characteristics (T_J =25°C Noted)



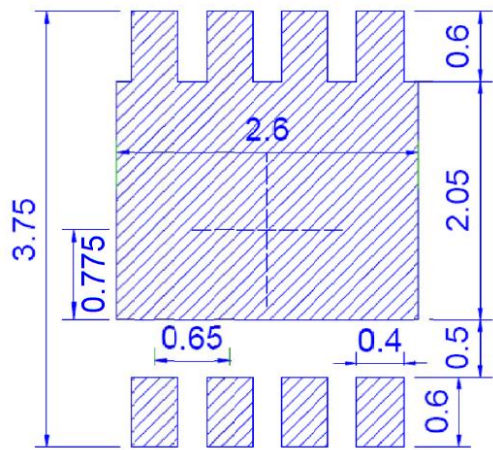
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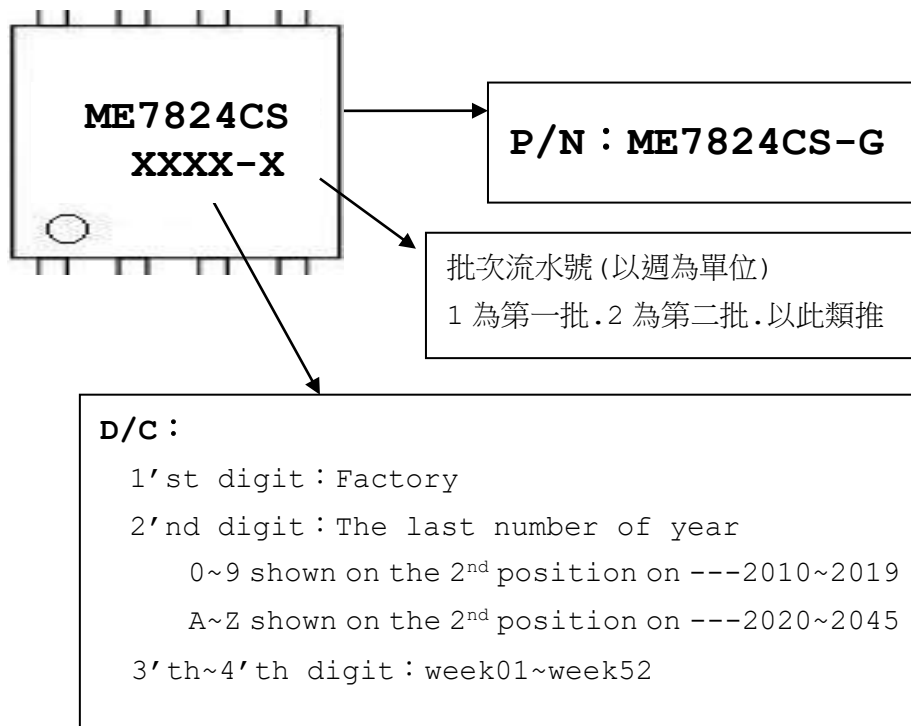
DFN(S) 3x3 Package Outline



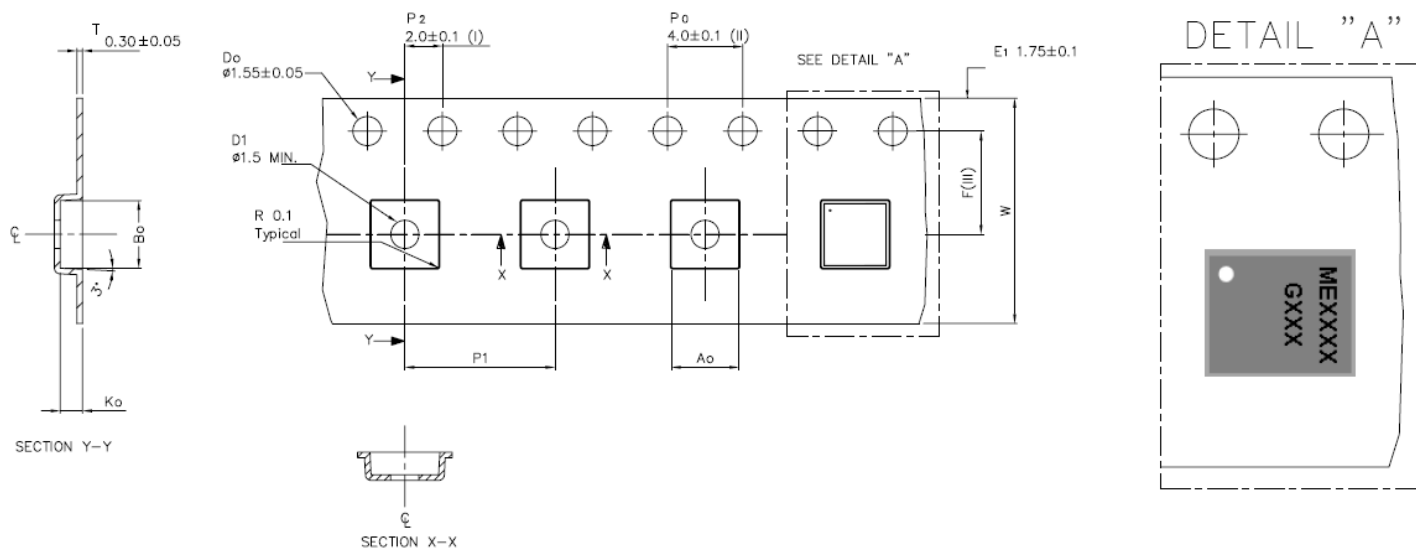
FOOTPRINT



SYMBOL	MILLIMETERS (mm)		
	MIN	Typ	MAX
A	0.7	0.775	0.85
b	0.2	0.3	0.4
c	0.1	0.175	0.25
D	3.15	3.3	3.45
D1	2.9	3.05	3.2
D2	1.54	1.74	1.94
D3	0.1	0.2	0.3
E	3.15	3.3	3.45
E1	3	3.125	3.25
E2	2.29	2.47	2.65
e	0.65BSC		
H	0.28	0.465	0.65
L	0.28	0.39	0.5
L1	0.06	0.13	0.2
θ	10°	12°	14°
M	0	0.075	0.13
* Not specified			



DFN3*3 Carrier Tape & Reel



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包裝規範

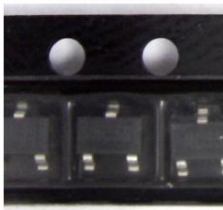
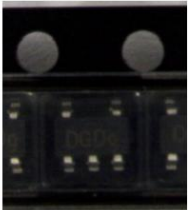
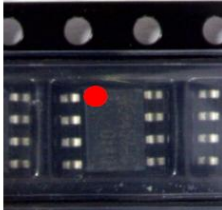
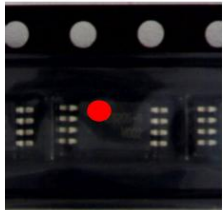
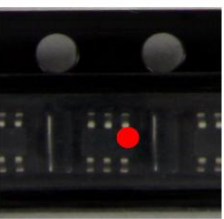
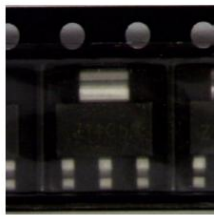
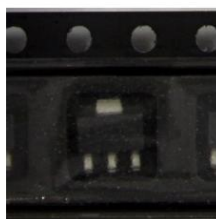
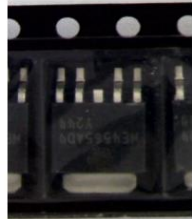
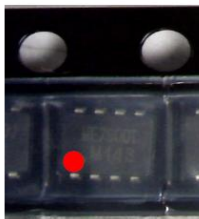
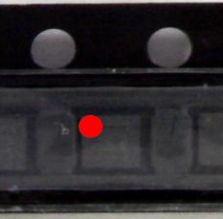
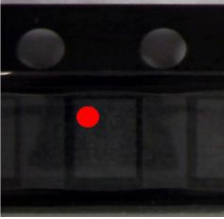
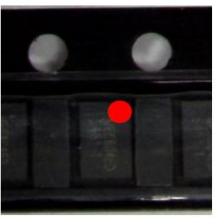
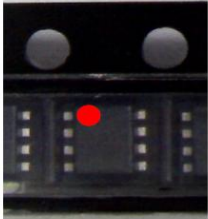
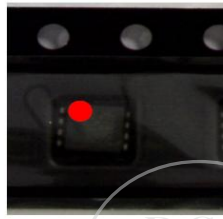
修定日期：2019 年 5 月 9 日

製作者：林 群 杰

文件編號：FM-E003

版本：E

各封裝對應捲盤、數量、零件方向

Package Type	SOT-23 SOT-小23	SOT-25	SOT-26 TSOP-6	SOP-8	TSSOP-8
PIC					
說明	單PIN朝圓孔	雙PIN朝圓孔	PIN1朝圓孔反方向	PIN1朝圓孔方向	PIN1朝圓孔方向
Reel size	7"	7"	7"	13"	13"
數量	3K	3K	3K	2.5K	3K
Package Type	SC-70 3L (SOT-323)	SC-70 5L (SOT-353)	SC-70 6L (SOT-363)	SOT-523	SOT-723
PIC					
說明	單PIN朝圓孔	雙PIN朝圓孔	PIN1朝圓孔方向	單PIN朝圓孔	單PIN朝圓孔
Reel size	7"	7"	7"	7"	7"
數量	3K	3K	3K	3K	8K
Package Type	SOT-223	SOT-89	TO-252-3L	TO-252-4L	J2928
PIC					
說明	單PIN朝圓孔	單PIN朝圓孔	PIN朝圓孔	PIN朝圓孔	PIN1朝圓孔反方向
Reel size	13"	7"	13"	13"	7"
數量	2.5K	1K	2.5K	2.5K	3K
Package Type	DFN2*2	DFN3*2	TDFN2*3	DFN3*3	DFN3.3*3.3
PIC					
說明	PIN1朝圓孔方向	PIN1朝圓孔方向	PIN1朝圓孔方向	PIN1朝圓孔方向	PIN1朝圓孔方向
Reel size	7"	7"	13"	13"	13"
數量	3K	3K	3K	3K	3K

包裝規範

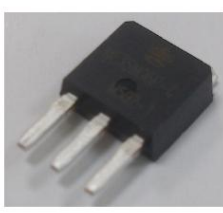
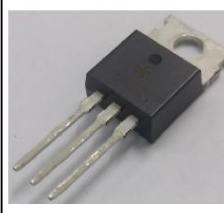
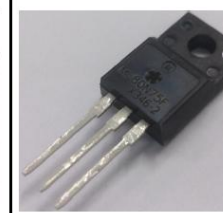
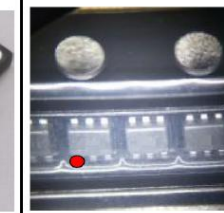
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各封裝對應捲盤、數量、零件方向

Package Type	PPAK(DFN) 5*6	TO-251	TO-220	TO-220F	SOT-563
PIC					
說明	PIN1 朝圓孔方向				PIN1 朝圓孔反方向
Reel size	13"	tube	tube	tube	7"

料帶設定及標籤(Reel)



不併批 Reel 的標籤位置



併批 Reel 的標籤位置

1. 依照各封裝採用對應 Reel。
2. 料帶前空 400mm 以上(含載帶、蓋帶)，後空 160mm 以上(含載帶、蓋帶)。(依照 EIA-481)
3. 所有標籤貼於載帶圓孔相反側，Date code 不併批時，RoHS 標籤需黏貼於力士標籤正下方。
4. 不同料號不可合併。
5. 同料號不同 Date code 可合併，於 Reel 上各貼上併批標籤。

即一個 Reel 中僅可有 2 個 Date code，一個 Date code 僅可合併一次。

併批說明：Date code A 的尾數可跟 Date code B 併批；Date code B 的尾數可跟 Date code C 併批。

但 Date code A 的尾數已經 Date code B 併批，不可再跟 Date code C 併批。

DCC
正式發行

包裝規範

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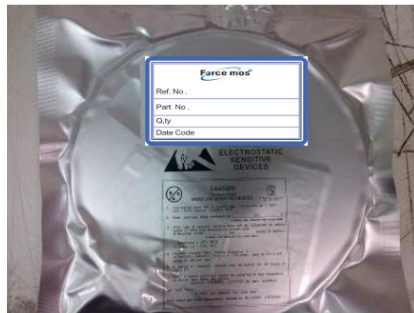
版本：E

真空包裝(Reel)



1. 產品用防靜電袋真空包裝，並抽真空密封；**MSL1 等級除外**。

MSL3 包裝(特別指定)



1. 依照MSL(MSD) 3使用防靜電鋁箔袋(真空靜電袋)=>客戶指定，擺放乾燥劑及濕度指示卡(3或6點)於袋中後，抽真空。(乾燥劑及指示卡須符合綠色產品要求)
2. 防靜電鋁箔袋上須有警示標示。
3. 防靜電鋁箔袋上需貼上產品標籤，內容格式同Reel。

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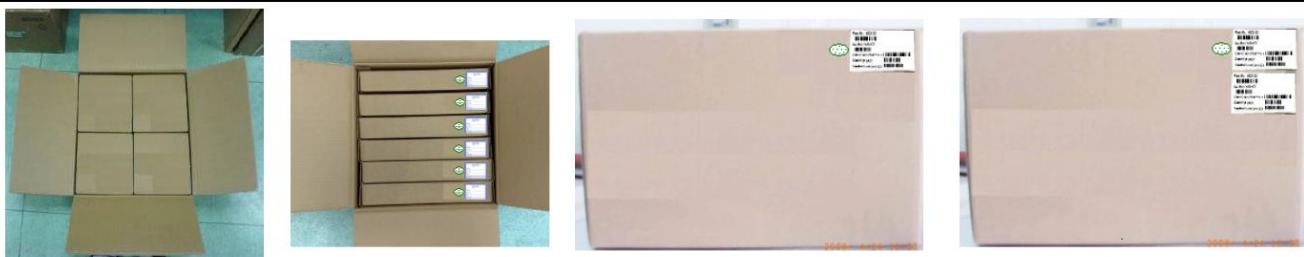
版本：E

內箱包裝(Reel)



1. 捲盤(Reel) 7" 一個內箱(Box)裝 5 個 Reel；捲盤(Reel)13" 一個內箱(Box)裝 2 個(Reel)
2. 不拼批時，力士標籤貼於內箱正面右方，RoHS 標籤貼附於力士標籤左方。
3. 不同料號不可合併。
4. 同料號不同 Date code 可合併，一個 Date code 僅可並批一次，於內箱側邊正面貼上併批標籤。

外箱包裝方式(Reel)



1. 7"：一個外箱(Carton)裝 12 個內箱(Box)。13"：一個外箱(Carton)裝 6 個內箱(Box)。
2. 不足數量以空箱或填充物補足，封箱用寬度為 4.8cm 之透明膠帶。
3. 7"：內箱標籤面朝與外箱標籤朝同一方向。13"：內箱標籤面朝上，且需同一方向性。
4. 不拼批時，外箱標籤貼於外箱寬面右上方，RoHS 標籤貼附於外箱標籤左方。
5. 不同料號不可合併。
6. 同料號不同 Date code 可併箱出貨，一個外箱僅限二個 Date code，不同 Date code 的外箱標籤必須分別標示貼附，外箱標籤貼於外箱寬面右上方，依 Date code 順序逐次向下貼附，RoHS 標籤貼附於外箱標籤最上列左方。
7. 外箱標籤上貼透明膠帶，避免標籤油墨因搬運磨擦導致字跡不清。