

P-Channel 30V (D-S) MOSFET

GENERAL DESCRIPTION

The ME2303S is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where low in-line power loss are needed in a very small outline surface mount package.

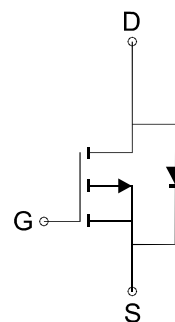
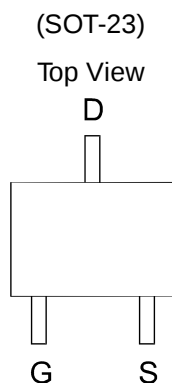
FEATURES

- $R_{DS(ON)} \leq 75m\Omega @ V_{GS} = -10V$
- $R_{DS(ON)} \leq 100m\Omega @ V_{GS} = -4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$

APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- Load Switch
- DSC

PIN CONFIGURATION



P-Channel MOSFET

Ordering Information: ME2303S(Pb-free)

ME2303S-G (Green product-Halogen free)

Absolute Maximum Ratings (TA=25°C Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current *	$T_A = 25^\circ C$	I_D	-3.2	A
	$T_A = 70^\circ C$		-2.6	
Pulsed Drain Current		I_{DM}	-13	A
Maximum Power Dissipation	$T_A = 25^\circ C$	P_D	1.3	W
	$T_A = 70^\circ C$		0.8	
Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ C$
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	100	$^\circ C/W$

* The device mounted on 1in² FR4 board with 2 oz copper

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Electrical Characteristics ($T_A=25^{\circ}\text{C}$ Unless Otherwise Specified)

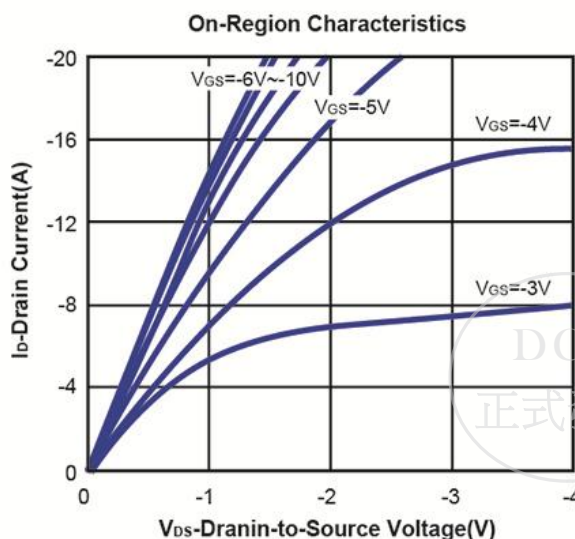
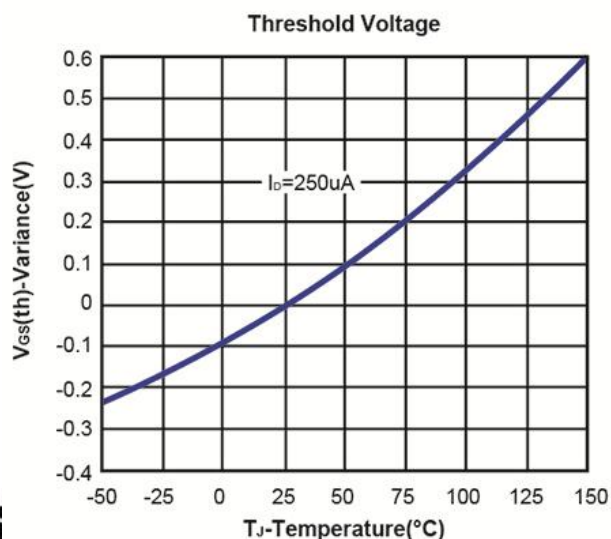
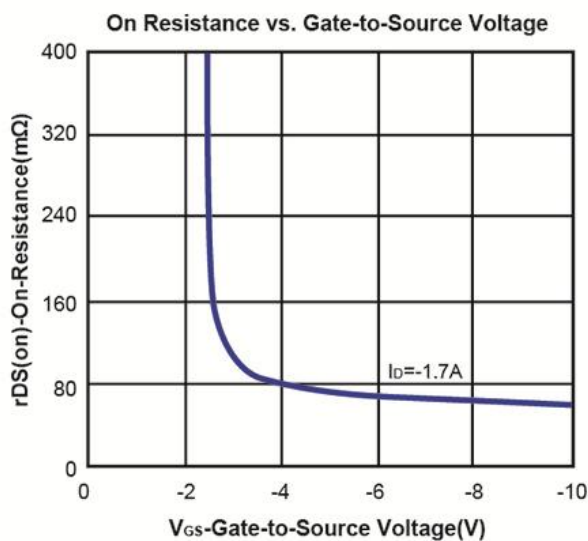
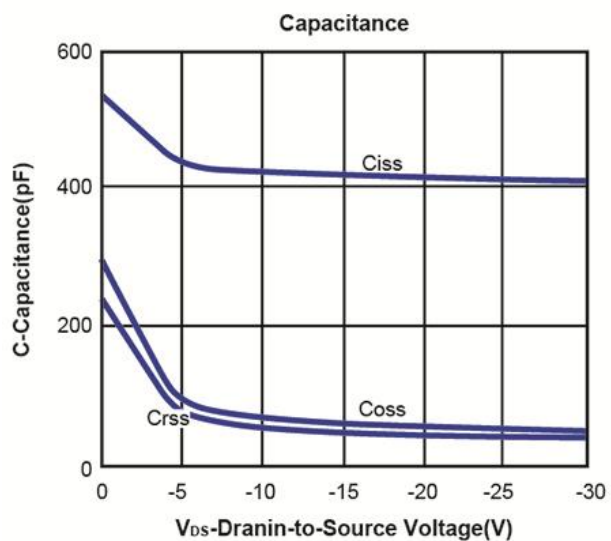
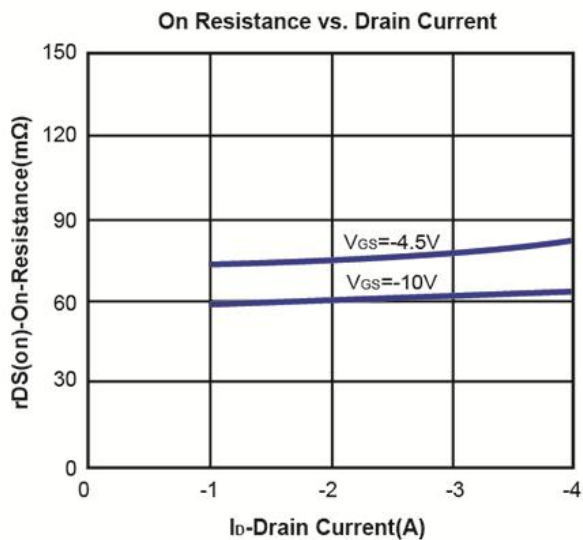
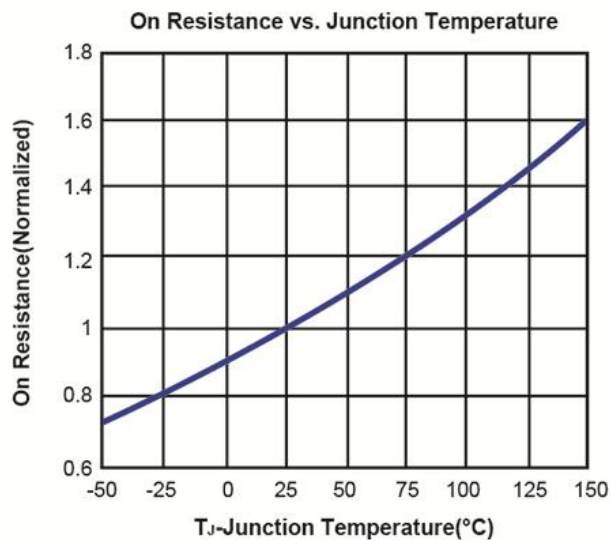
Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-30			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1		-3.0	V
I_{GSS}	Gate Leakage Current	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-30V, V_{GS}=0V$			-1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance ^a	$V_{GS}=-10V, I_D=-1.7A$		60	75	m Ω
		$V_{GS}=-4.5V, I_D=-1.3A$		75	100	
V_{SD}	Diode Forward Voltage	$I_S=-1.25A, V_{GS}=0V$		-0.7	-1.4	V
DYNAMIC						
Q_g	Total Gate Charge	$V_{DS}=-15V, V_{GS}=-10V, I_D=-1.7A$		14		nC
Q_g	Total Gate Charge	$V_{DS}=-15V, V_{GS}=-4.5V, I_D=-1.7A$		6.7		
Q_{gs}	Gate-Source Charge			2.6		
Q_{gd}	Gate-Drain Charge			2.1		
C_{iss}	Input Capacitance	$V_{DS}=-15V, V_{GS}=0V, f=1MHz$		416		pF
C_{oss}	Output Capacitance			56		
C_{rss}	Reverse Transfer Capacitance			46		
$t_{d(on)}$	Turn-On Delay Time	$V_{DS}=-15V, R_L=15\Omega$ $R_{GS}=6\Omega, V_{GS}=-10V$ $I_D=-1A$		34.4		ns
t_r	Turn-On Rise Time			18		
$t_{d(off)}$	Turn-Off Delay Time			43.9		
t_f	Turn-Off Fall time			5.6		

Notes: a. Pulse test; pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

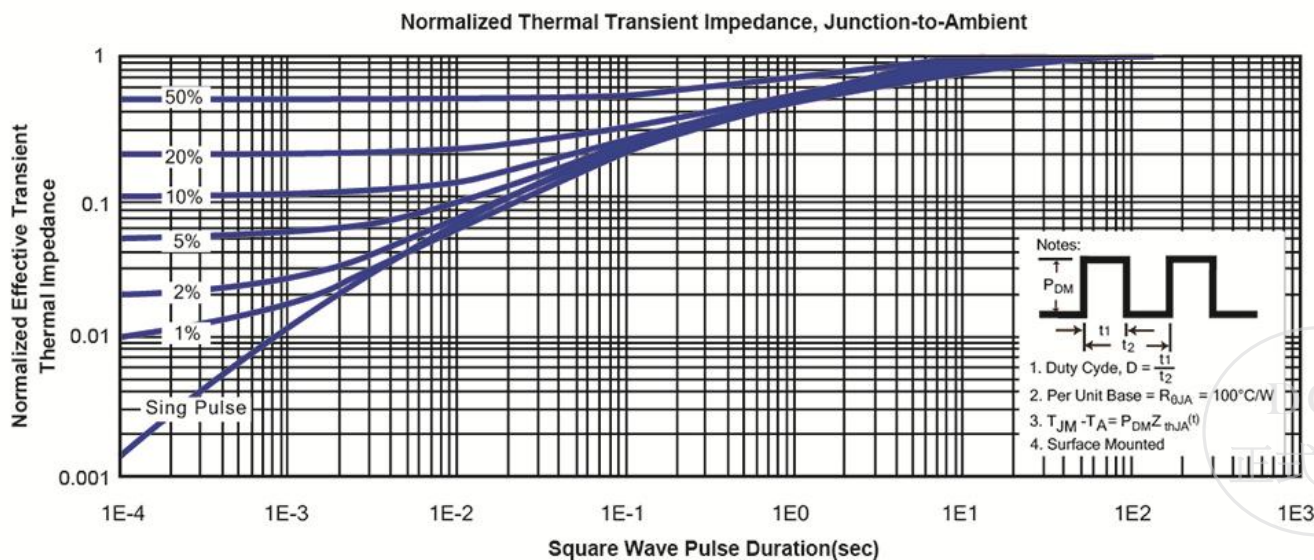
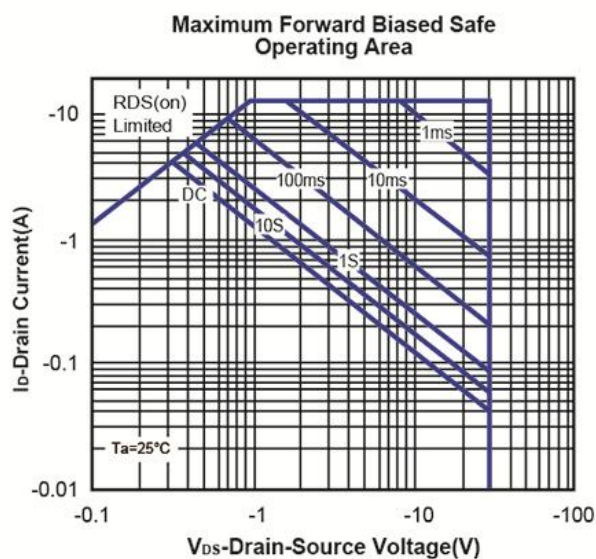
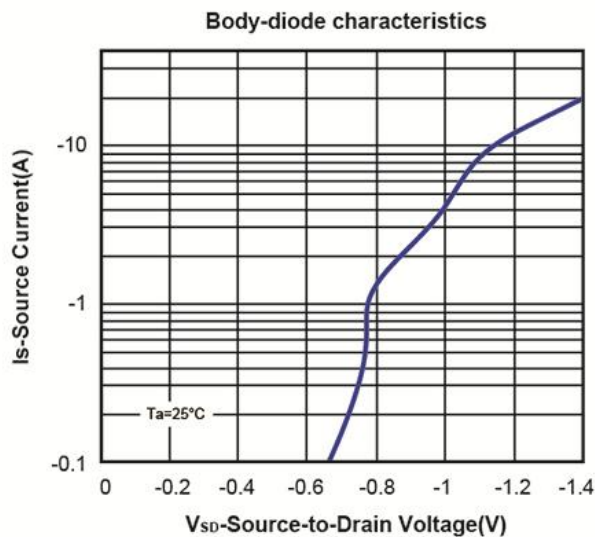
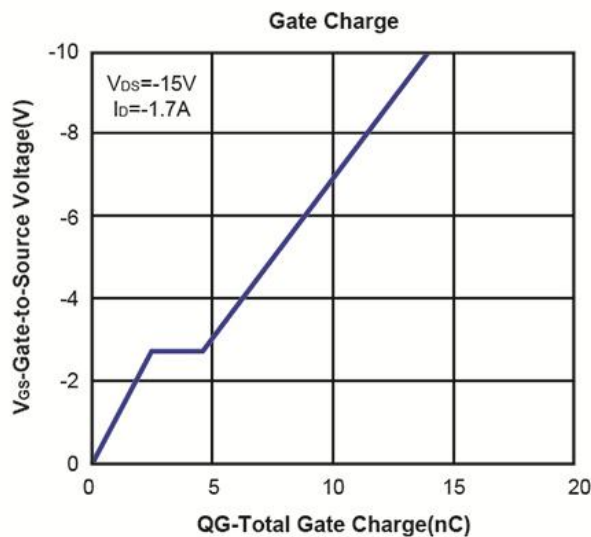
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Typical Characteristics (T_J = 25°C Noted)

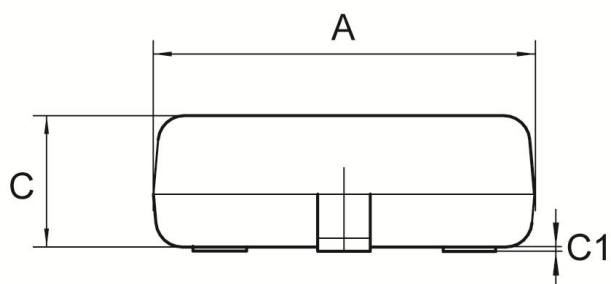
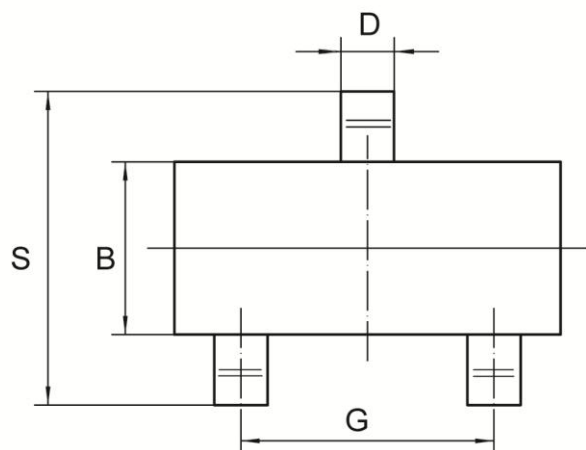


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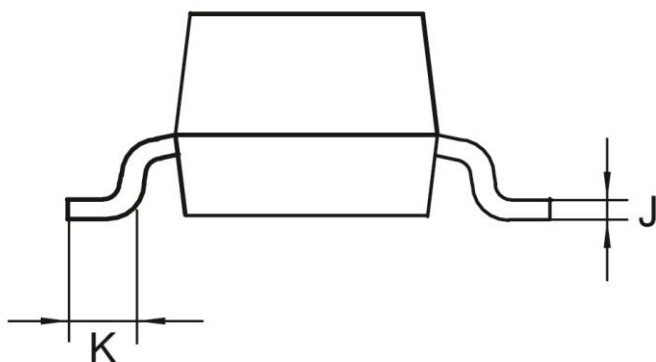
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SOT-23 Package Outline



Symbol	MILLIMETERS	
	MIN	MAX
A	2.8	3.0
B	1.2	1.4
C	0.9	1.1
C1	-	0.1
D	0.3	0.5
G	1.90 REF	
J	0.05	0.15
K	0.2	-
S	2.2	2.6



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