

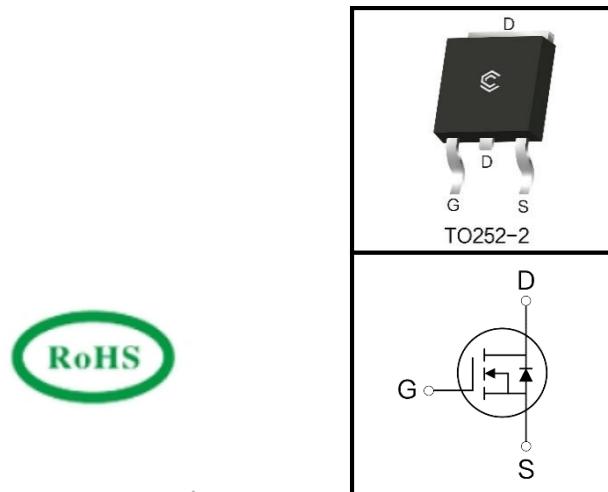
650V Super-Junction Power MOSFET

FEATURES

- Very low FOM $R_{DS(on)} \times Q_g$
- 100% avalanche tested
- RoHS compliant

APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply (UPS)
- Power Factor Correction (PFC)



RoHS

Device Marking and Package Information

Device	Package	Marking
CLD65R280R	TO252-2	CLD65R280R

Absolute Maximum Ratings at $T_c = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-Source Voltage ($V_{GS} = 0\text{V}$)	V_{DSS}	650	V
Continuous Drain Current	I_D	15	A
Continuous Drain Current $T_c = 100^\circ\text{C}$		9	
Pulsed Drain Current (note1)	I_{DM}	45	A
Gate-Source Voltage	V_{GSS}	± 30	V
Single Pulse Avalanche Energy (note2)	E_{AS}	80	mJ
Avalanche Current (note1)	I_{AS}	4	A
Repetitive Avalanche Energy (note1)	E_{AR}	0.32	mJ
Power Dissipation	P_D	132	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55~+150	°C

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-Case	$R_{\theta JC}$	0.93	°C/W
Thermal Resistance, Junction-Ambient	$R_{\theta JA}$	106	

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise specified						
Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}} = 0\text{V}$, $I_D = 250\mu\text{A}$	650	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}} = 650\text{V}$, $V_{\text{GS}} = 0\text{V}$, $T_J = 25^\circ\text{C}$	--	--	1	uA
		$V_{\text{DS}} = 650\text{V}$, $V_{\text{GS}} = 0\text{V}$, $T_J = 150^\circ\text{C}$	--	--	100	
Gate-Source Leakage	I_{GSS}	$V_{\text{GS}} = \pm 30\text{V}$	--	--	± 100	nA
Gate-Source Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}} = V_{\text{GS}}$, $I_D = 250\mu\text{A}$	2.5	--	4.0	V
Drain-Source On-Resistance (note3)	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}} = 10\text{V}$, $I_D = 7.5\text{A}$	--	0.24	0.28	Ω
Dynamic						
Input Capacitance	C_{iss}	$V_{\text{GS}} = 0\text{V}$, $V_{\text{DS}} = 100\text{V}$, $f = 100\text{kHz}$	--	1126	--	pF
Output Capacitance	C_{oss}		--	41	--	
Reverse Transfer Capacitance	C_{rss}		--	0.79	--	
Gate Resistance	R_g	$V_{\text{GS}} = 0\text{V}$, $f = 1.0\text{MHz}$	--	3.9	--	Ω
Total Gate Charge	Q_g		--	26	--	nC
Gate-Source Charge	Q_{gs}		--	3.6	--	
Gate-Drain Charge	Q_{gd}		--	10.5	--	
Gate Plateau Voltage	$V_{\text{GS}(\text{pl})}$		--	5.5	--	V
Turn-on Delay Time	$t_{\text{d}(\text{on})}$	$V_{\text{DD}} = 520\text{V}$, $I_D = 7.5\text{A}$, $V_{\text{GS}} = 10\text{V}$	--	20	--	ns
Turn-on Rise Time	t_r		--	40	--	
Turn-off Delay Time	$t_{\text{d}(\text{off})}$		--	95	--	
Turn-off Fall Time	t_f		--	43	--	
Body Diode Characteristics						
Continuous Body Diode Current	I_S	$T_C = 25^\circ\text{C}$	--	--	15	A
Pulsed Diode Forward Current	I_{SM}		--	--	45	
Body Diode Voltage	V_{SD}	$T_J = 25^\circ\text{C}$, $I_{\text{SD}} = 7.5\text{A}$, $V_{\text{GS}} = 0\text{V}$	--	0.85	1.2	V
Reverse Recovery Time	t_{rr}	$V_R = 300\text{V}$, $I_F = 7.5\text{A}$, $di_F/dt = 100\text{A}/\mu\text{s}$	--	260	--	ns
Reverse Recovery Charge	Q_{rr}		--	2.95	--	μC
Peak Reverse Recovery Current	I_{rrm}		--	21	--	A

Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. $I_{\text{AS}} = 4\text{ A}$, $V_{\text{DD}} = 50\text{V}$, $R_g = 25\Omega$, $L = 10\text{mH}$, Starting $T_J = 25^\circ\text{C}$
3. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 1\%$

Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 1. Output Characteristics

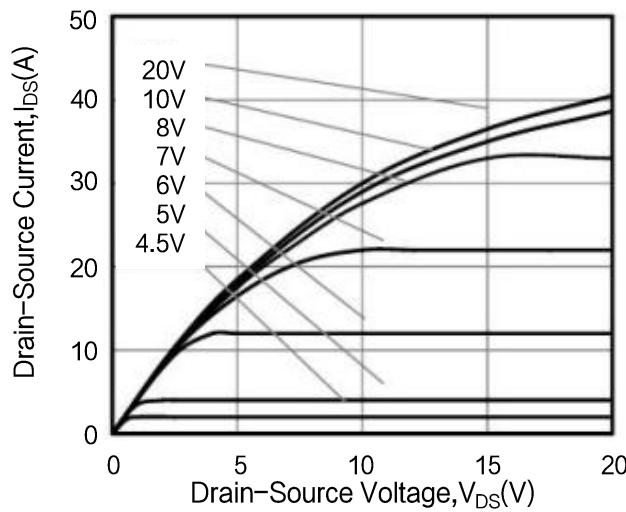


Figure 2. Transfer Characteristics

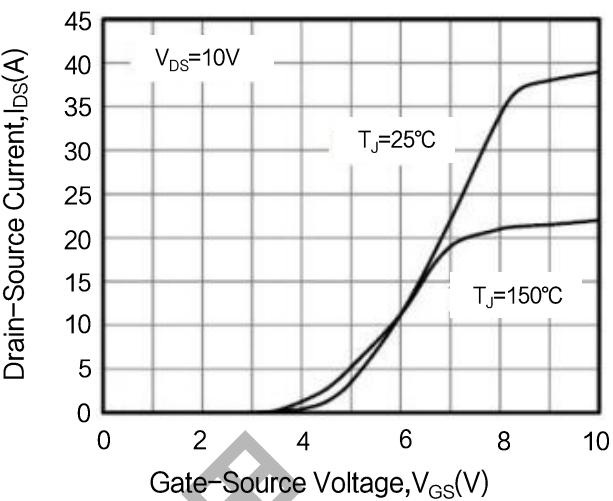


Figure 3. On-Resistance vs. Drain Current

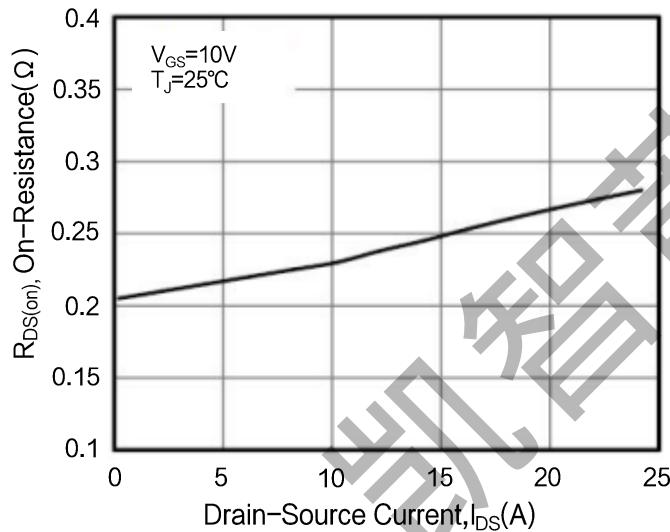


Figure 4. Capacitance

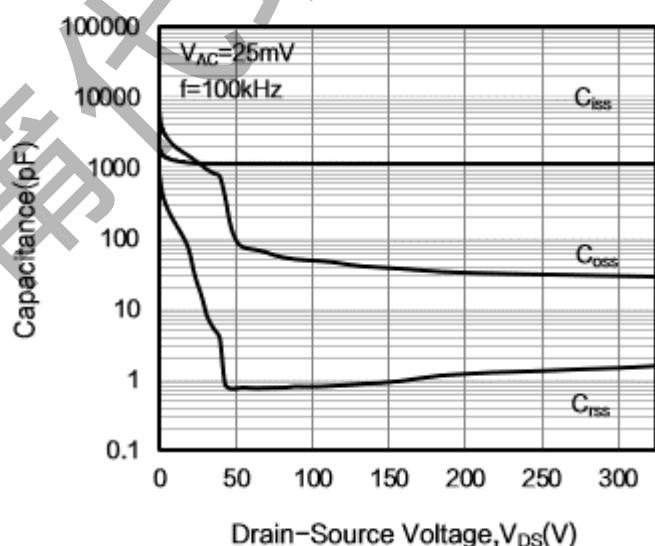


Figure 5. Gate Charge Characteristics

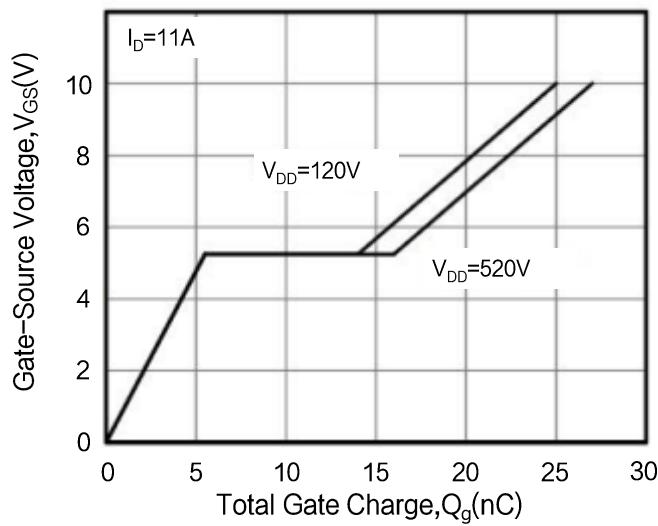
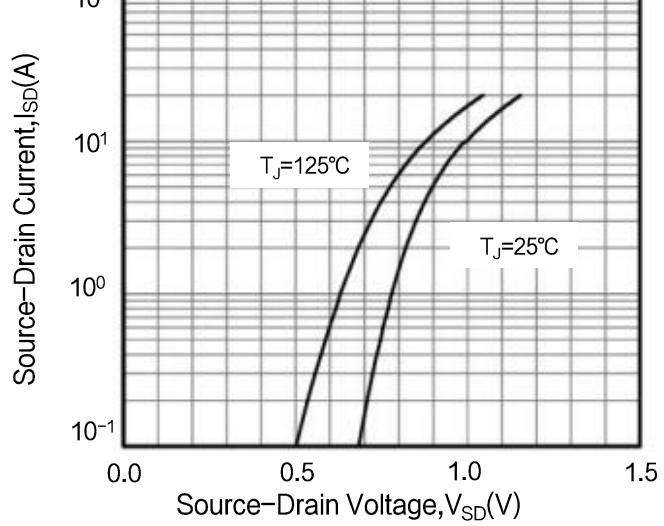


Figure 6. Body Diode Forward Voltage



Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Fig.7 Normalized On-Resistance vs. Temperature

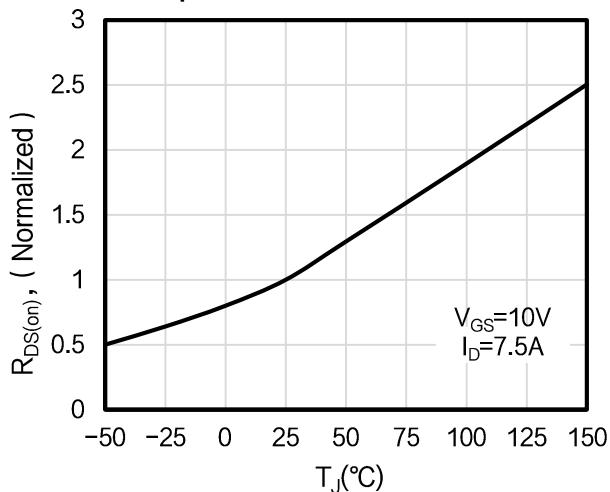


Fig.8 Normalized Threshold Voltage vs. Temperature

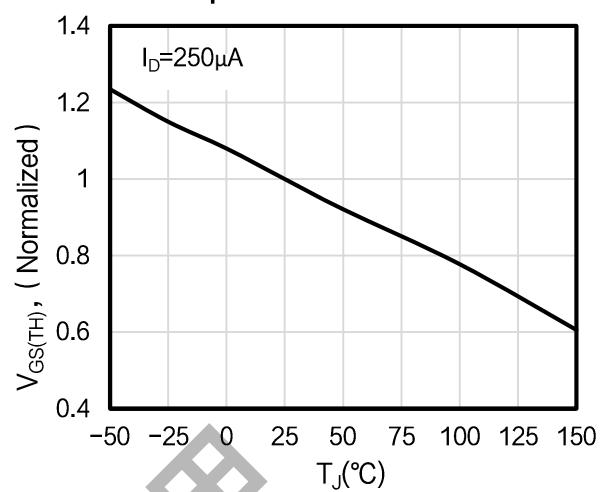


Figure 9. Transient Thermal Impedance

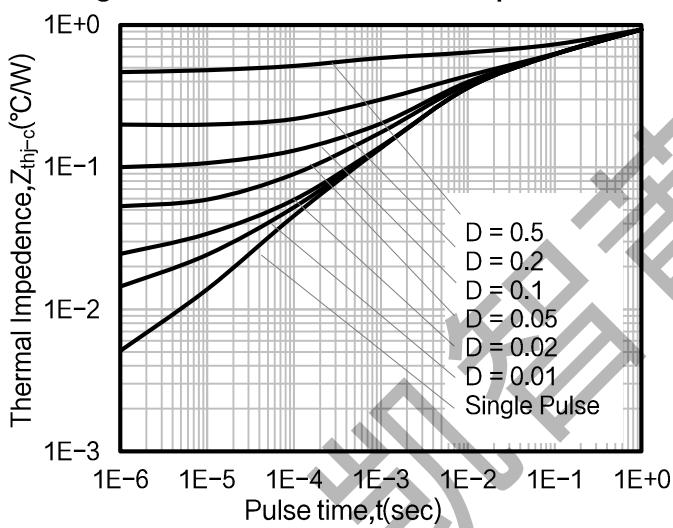


Figure 10. Safe Operation Area

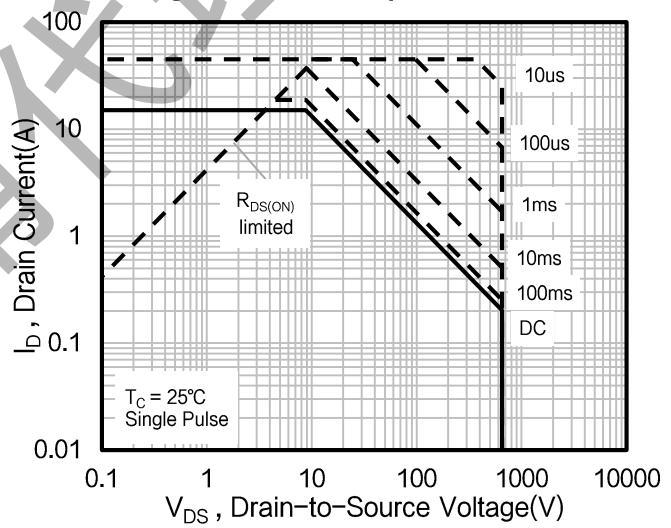


Figure A: Gate Charge Test Circuit and Waveform

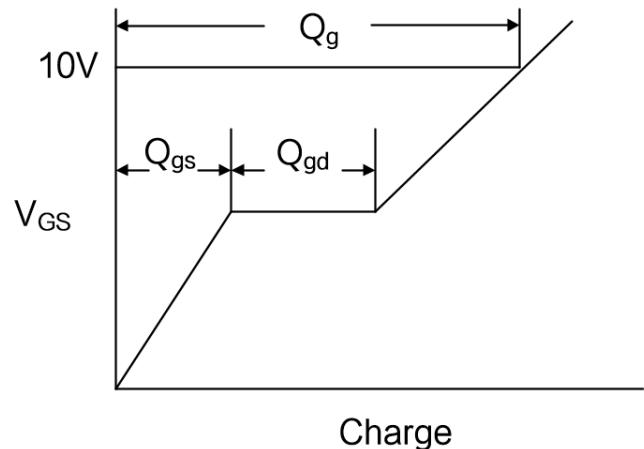
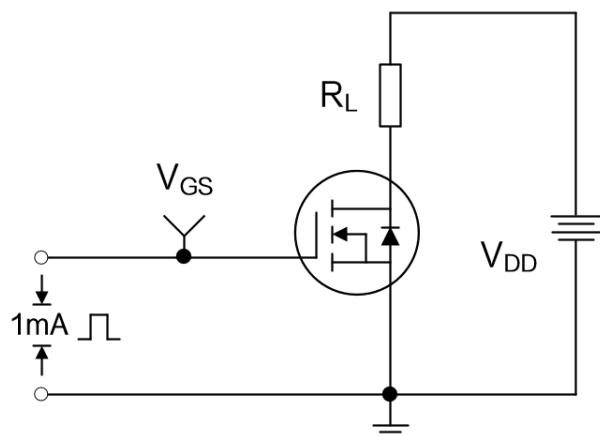


Figure B: Resistive Switching Test Circuit and Waveform

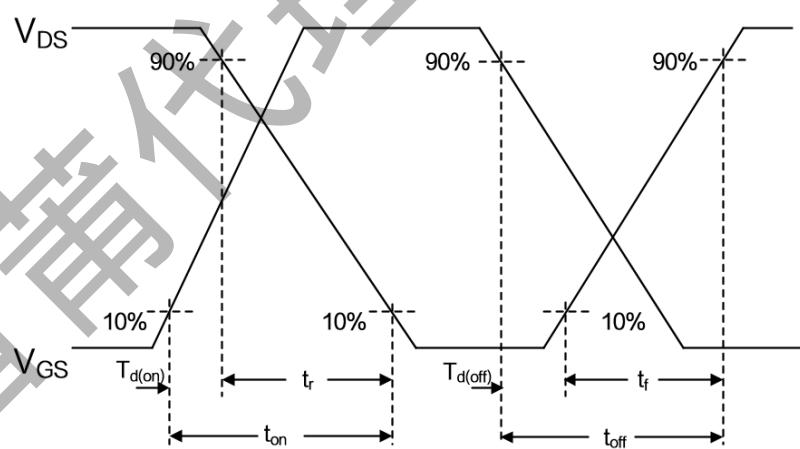
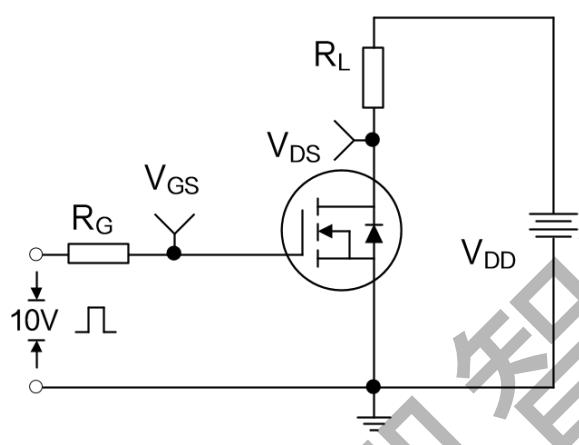
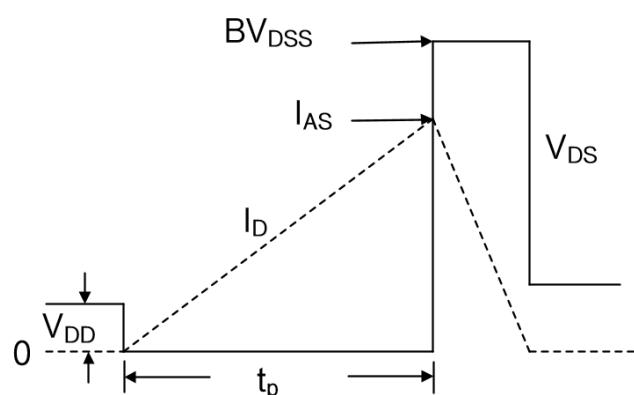
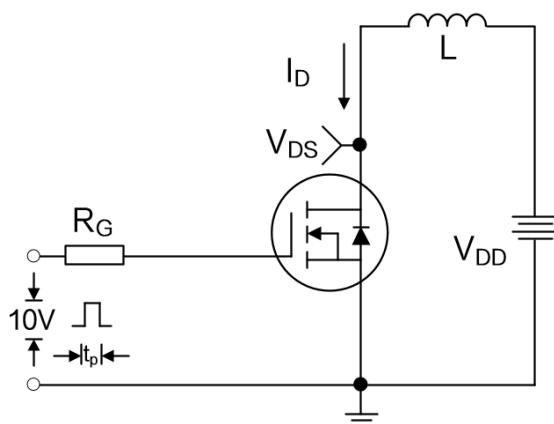
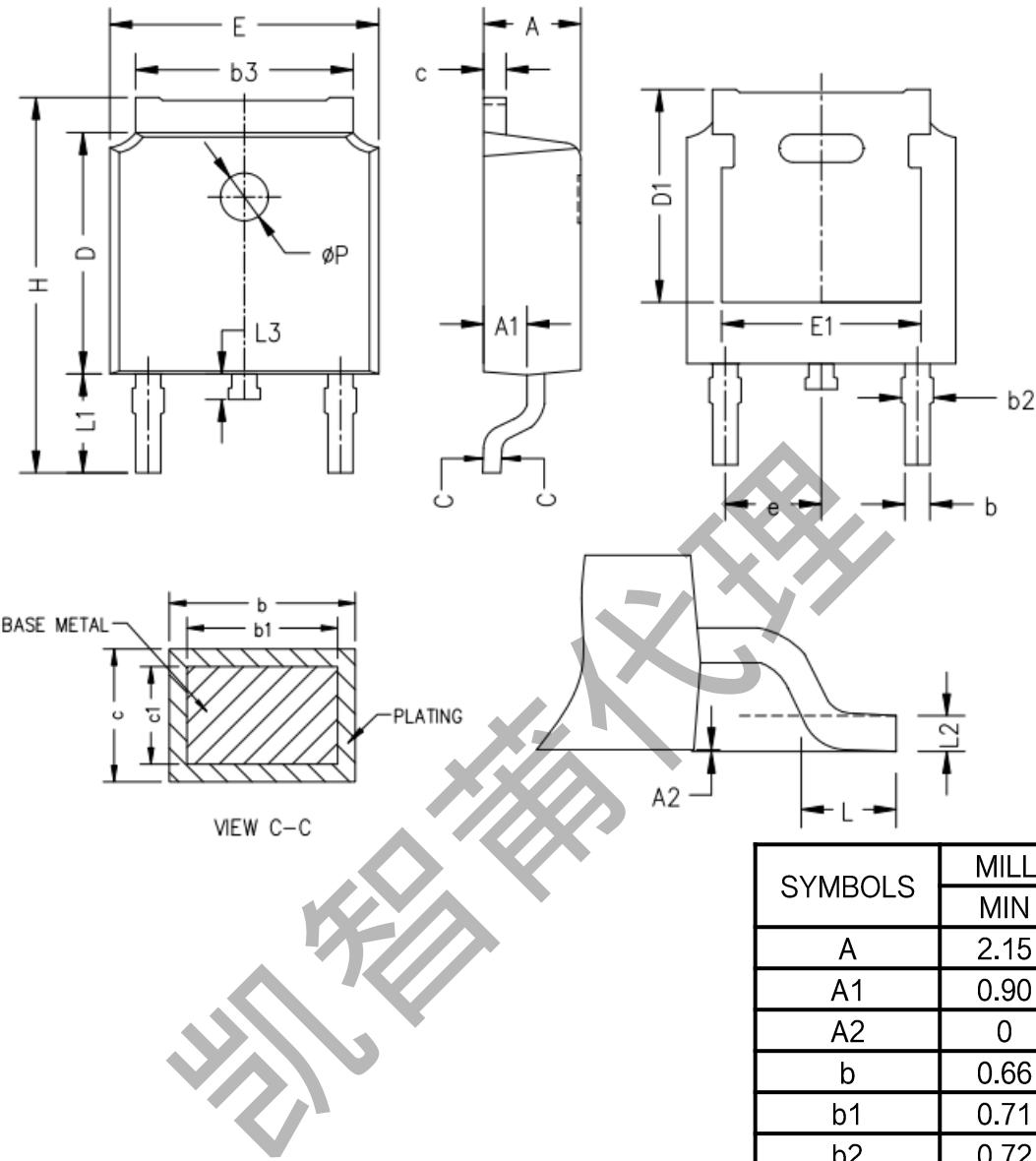


Figure C: Unclamped Inductive Switching Test Circuit and Waveform



TO252-2



SYMBOLS	MILLIMETERS	
	MIN	MAX
A	2.15	2.45
A1	0.90	1.12
A2	0	0.20
b	0.66	0.87
b1	0.71	0.81
b2	0.72	1.23
b3	5.12	5.52
c	0.40	0.61
c1	0.46	0.56
D	5.95	6.25
D1	5.25	6.25
e	2.286BSC	
E	6.45	6.75
E1	4.70	--
H	9.77	10.40
L	1.40	1.70
L1	2.90REF	
L2	0.508REF	
L3	0.60	1.00
ØP	1.10	1.40

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