

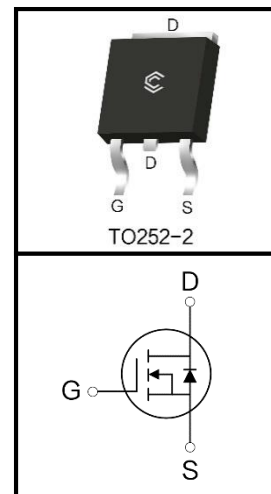
## 650V Super-Junction Power MOSFET

### FEATURES

- Very low FOM  $R_{DS(on)} \times Q_g$
- 100% avalanche tested
- RoHS compliant

### APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply (UPS)
- Power Factor Correction (PFC)



### Device Marking and Package Information

Device	Package	Marking
CLD65R280R	TO252-2	CLD65R280R

### Absolute Maximum Ratings at $T_c = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-Source Voltage ( $V_{GS} = 0V$ )	$V_{DSS}$	650	V
Continuous Drain Current	$I_D$	15	A
Continuous Drain Current $T_c = 100^\circ\text{C}$		9	
Pulsed Drain Current (note1)	$I_{DM}$	45	A
Gate-Source Voltage	$V_{GSS}$	$\pm 30$	V
Single Pulse Avalanche Energy (note2)	$E_{AS}$	80	mJ
Avalanche Current (note1)	$I_{AS}$	4	A
Repetitive Avalanche Energy (note1)	$E_{AR}$	0.32	mJ
Power Dissipation	$P_D$	132	W
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	$-55 \sim +150$	$^\circ\text{C}$

### Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-Case	$R_{\theta JC}$	0.93	$^\circ\text{C/W}$
Thermal Resistance, Junction-Ambient	$R_{\theta JA}$	106	

Electrical Characteristics T <sub>J</sub> = 25°C unless otherwise specified						
Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	650	--	--	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 650V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 25°C	--	--	1	uA
		V <sub>DS</sub> = 650V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 150°C	--	--	100	
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 30V	--	--	± 100	nA
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	2.5	--	4.0	V
Drain-Source On-Resistance (note3)	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 7.5A	--	0.24	0.28	Ω
Dynamic						
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 100V, f = 100kHz	--	1126	--	pF
Output Capacitance	C <sub>oss</sub>		--	41	--	
Reverse Transfer Capacitance	C <sub>rss</sub>		--	0.79	--	
Gate Resistance	R <sub>g</sub>	V <sub>GS</sub> = 0V, f = 1.0MHz	--	3.9	--	Ω
Total Gate Charge	Q <sub>g</sub>	V <sub>DD</sub> = 520V, I <sub>D</sub> = 7.5A, V <sub>GS</sub> = 10V	--	26	--	nC
Gate-Source Charge	Q <sub>gs</sub>		--	3.6	--	
Gate-Drain Charge	Q <sub>gd</sub>		--	10.5	--	
Gate Plateau Voltage	V <sub>GS(pl)</sub>		--	5.5	--	V
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 400V, I <sub>D</sub> = 7.5A, R <sub>G</sub> = 25Ω	--	20	--	ns
Turn-on Rise Time	t <sub>r</sub>		--	40	--	
Turn-off Delay Time	t <sub>d(off)</sub>		--	95	--	
Turn-off Fall Time	t <sub>f</sub>		--	43	--	
Body Diode Characteristics						
Continuous Body Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25°C	--	--	15	A
Pulsed Diode Forward Current	I <sub>SM</sub>		--	--	45	
Body Diode Voltage	V <sub>SD</sub>	T <sub>J</sub> = 25°C, I <sub>SD</sub> = 7.5A, V <sub>GS</sub> = 0V	--	0.85	1.2	V
Reverse Recovery Time	t <sub>rr</sub>	V <sub>R</sub> = 300V, I <sub>F</sub> =7.5A, di <sub>F</sub> /dt = 100A/ μ s	--	260	--	ns
Reverse Recovery Charge	Q <sub>rr</sub>		--	2.95	--	μC
Peak Reverse Recovery Current	I <sub>rrm</sub>		--	21	--	A

#### Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2.  $I_{AS} = 4A, V_{DD} = 50V, R_G = 25\Omega, L = 10mH$ , Starting  $T_J = 25^\circ\text{C}$
3. Pulse Test: Pulse width  $\leq 300\mu s$ , Duty Cycle  $\leq 1\%$

Typical Characteristics  $T_J = 25^\circ\text{C}$ , unless otherwise noted

Figure 1. Output Characteristics

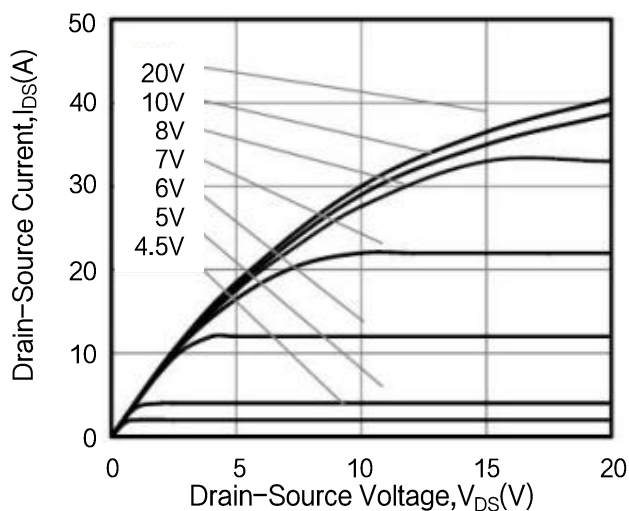


Figure 2. Transfer Characteristics

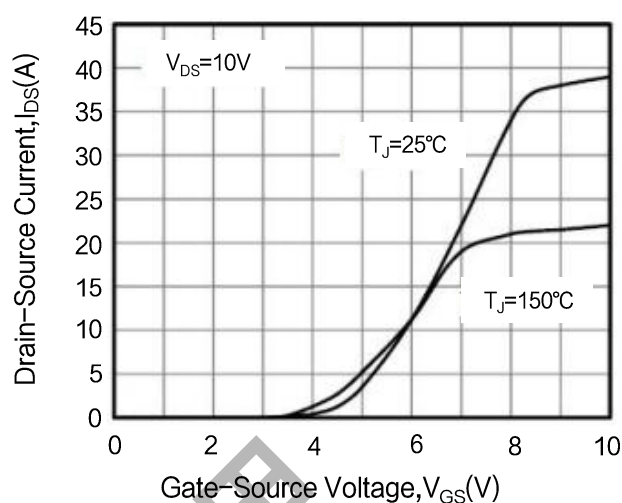


Figure 3. On-Resistance vs. Drain Current

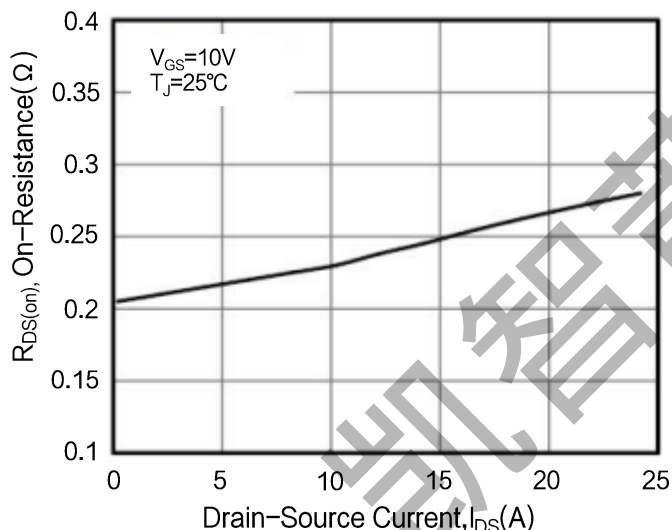


Figure 4. Capacitance

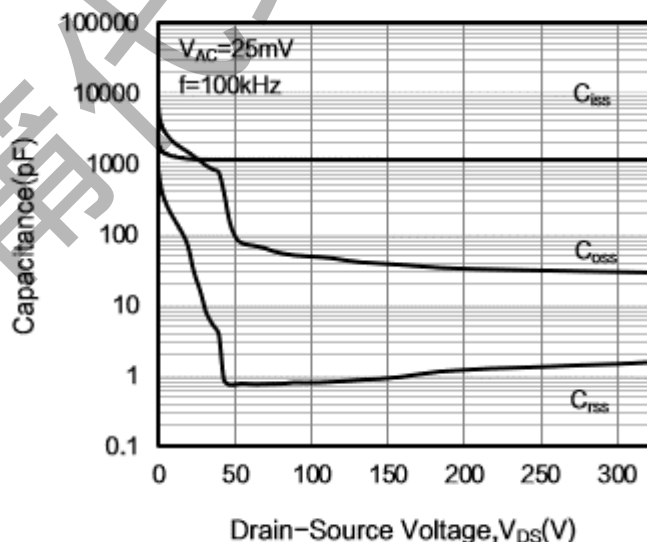


Figure 5. Gate Charge Characteristics

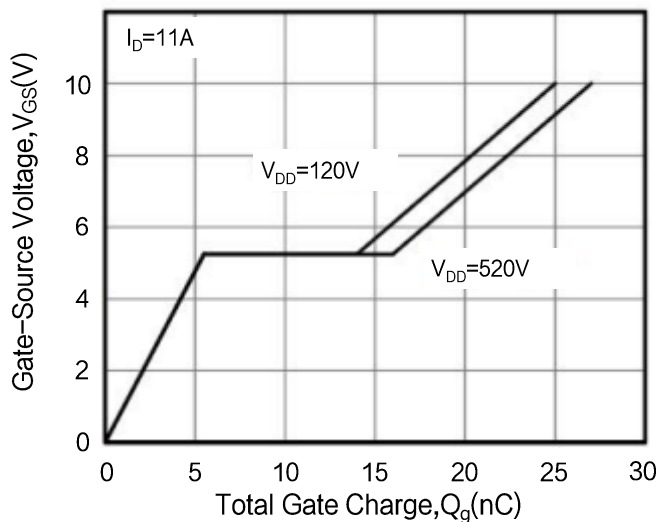
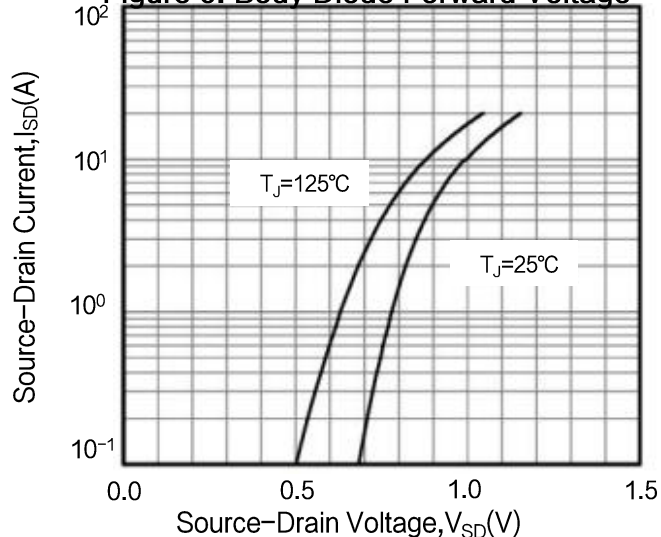


Figure 6. Body Diode Forward Voltage



Typical Characteristics  $T_J = 25^\circ\text{C}$ , unless otherwise noted

Fig.7 Normalized On-Resistance vs. Temperature

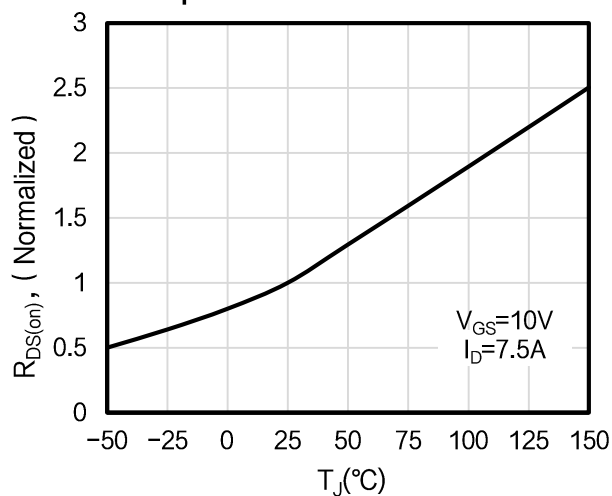


Fig.8 Normalized Threshold Voltage vs. Temperature

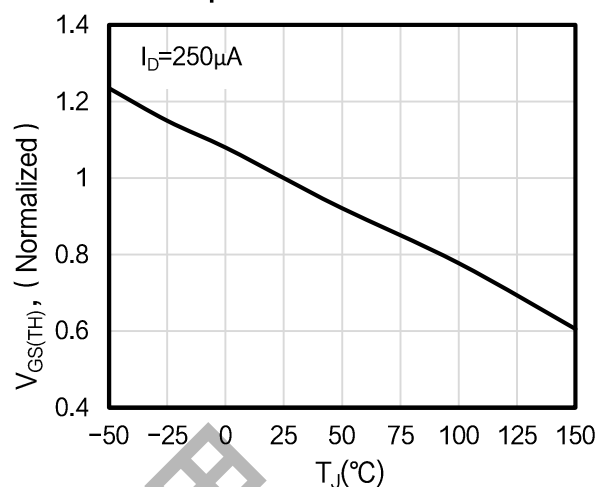


Figure 9. Transient Thermal Impedance

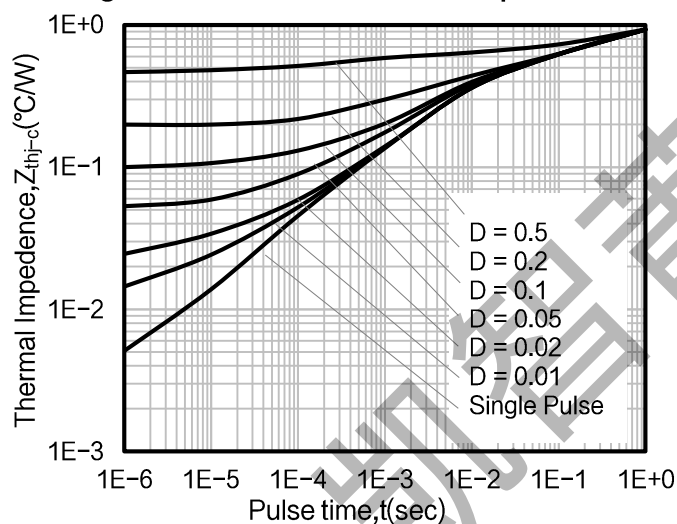


Figure 10. Safe Operation Area

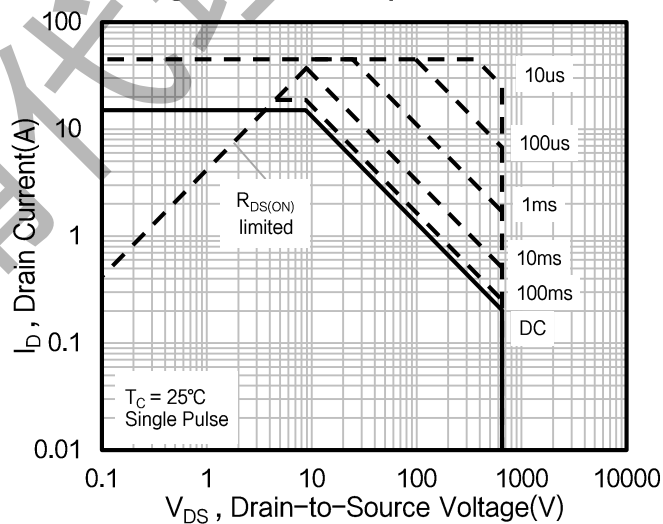


Figure A: Gate Charge Test Circuit and Waveform

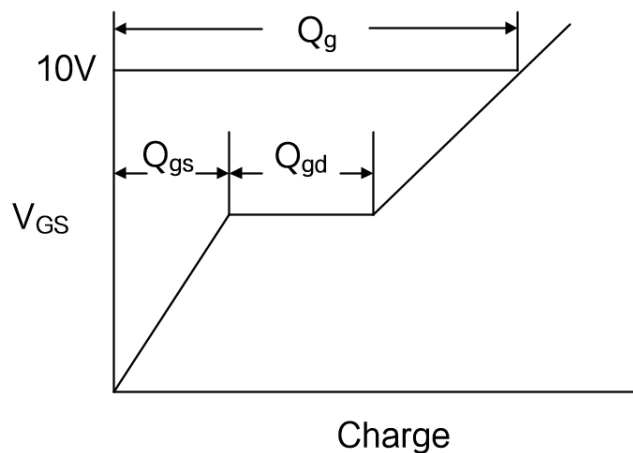
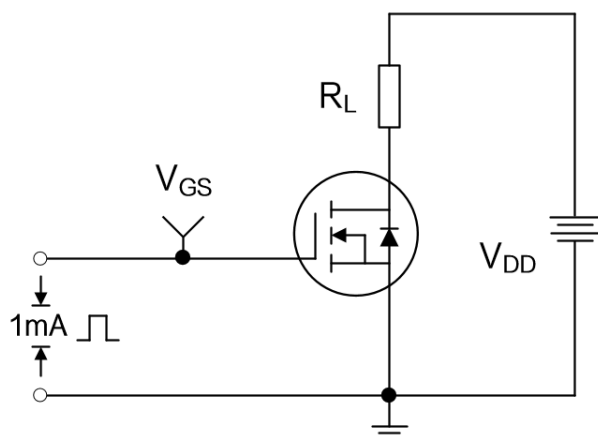


Figure B: Resistive Switching Test Circuit and Waveform

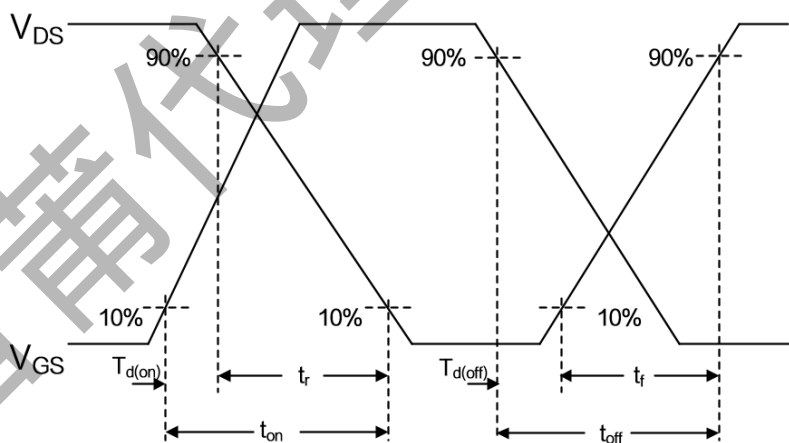
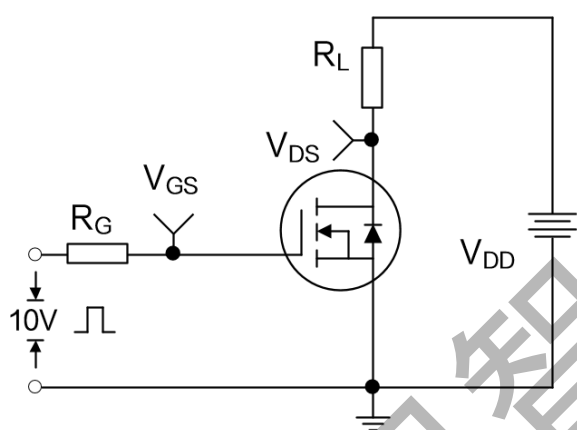
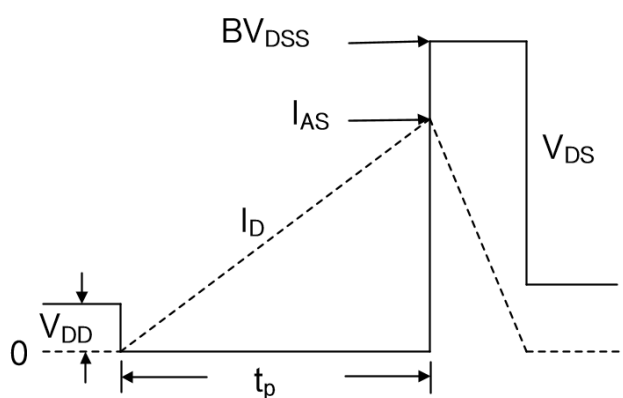
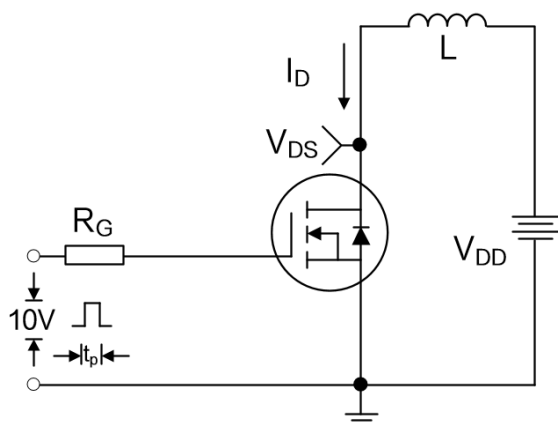
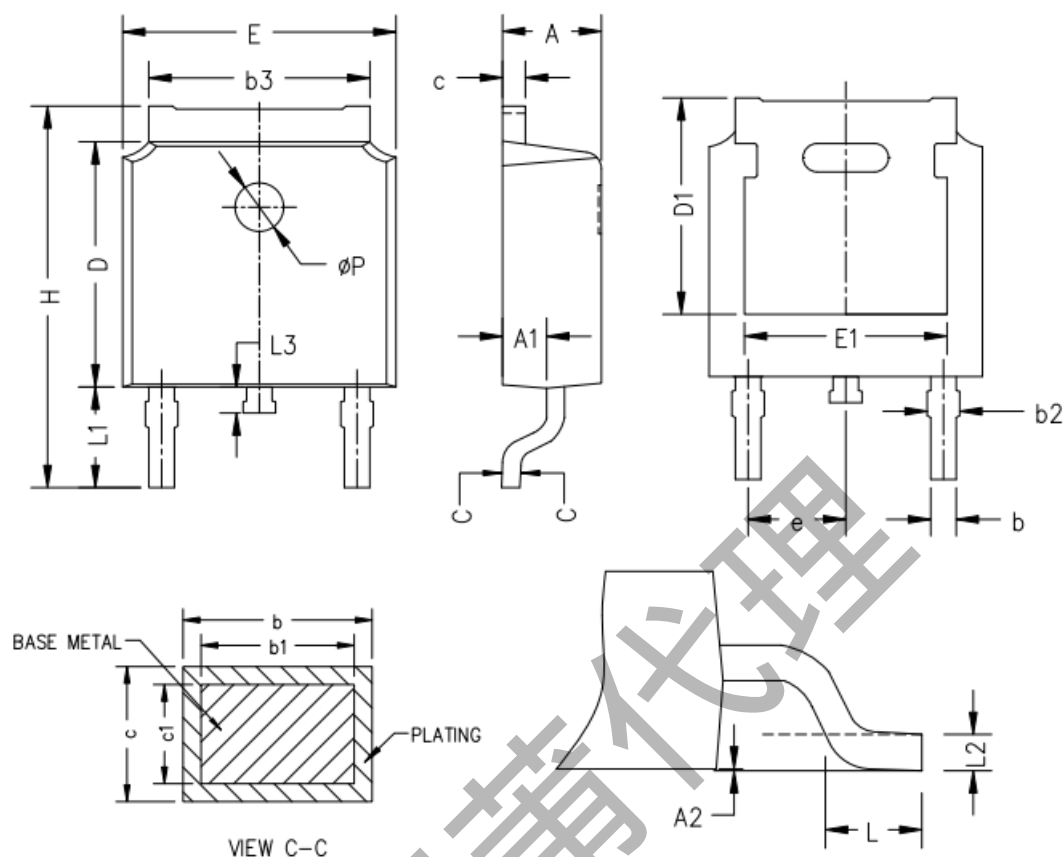


Figure C: Unclamped Inductive Switching Test Circuit and Waveform



## TO252-2



SYMBOLS	MILLIMETERS	
	MIN	MAX
A	2.15	2.45
A1	0.90	1.12
A2	0	0.20
b	0.66	0.87
b1	0.71	0.81
b2	0.72	1.23
b3	5.12	5.52
c	0.40	0.61
c1	0.46	0.56
D	5.95	6.25
D1	5.25	6.25
e	2.286BSC	
E	6.45	6.75
E1	4.70	--
H	9.77	10.40
L	1.40	1.70
L1	2.90REF	
L2	0.508REF	
L3	0.60	1.00
$\phi P$	1.10	1.40

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