ZHCSRR8B – OCTOBER 2023 – REVISED APRIL 2024

OPAx323 20MHz 高带宽、114dB CMRR、低压（1.7V 至 5.5V）RRIO 零交叉运算放大器

1 特性

- 适用于 1.7V 至 5.5V 应用的零交叉放大器
- 高轨到轨 CMRR：114dB（典型值）
- 高增益带宽积：20MHz
- 快速压摆率：33V/μs（典型值）
- 快速稳定 (0.01%)：在 2V 阶跃下的典型值为 200ns
- 低输入失调电压：±150μV（典型值）
- 低本底噪声：10kHz 时的典型值为 5.5nV/$\sqrt{Hz}$
- 高输出电流：5.5V 时 I_{SC} 典型值为 ±110mA
- 静态电流：1.6mA/通道（典型值）
- 轨至轨输入和输出
- 单位增益稳定
- 驱动高达 150pF 的电容，而不会出现持续振荡
- 内置 RFI 和 EMI 滤波输入引脚
- 工作温度范围：–40°C 至 125°C

2 应用

- 用于 ADC 的放大器驱动器
- 高侧电流检测
- 电机旋转编码器
- 跨阻光电二极管放大器
- 音频麦克风前置放大器
- 超声波传感器

3 说明

OPAx323 系列运算放大器包括单通道 (OPA323)、双通道 (OPA2323) 和四通道 (OPA4323) 的低压（1.7V 至 5.5V）、高带宽 (20MHz) 运算放大器，具有零交叉输入级和轨至轨输出级。对于具有 ADC 驱动器应用中典型轨至轨摆幅的输入信号，OPAx323 零交叉输入级可实现高线性和低失真。在 0.5MSPS 至 5MSPS 之间的 ADC 采样速度下，20MHz 增益带宽可提供快速稳定响应，具体取决于所需的稳定性能。OPAx323 经良好优化可实现节能，因为该器件仅消耗 1.6mA 的典型静态电流。

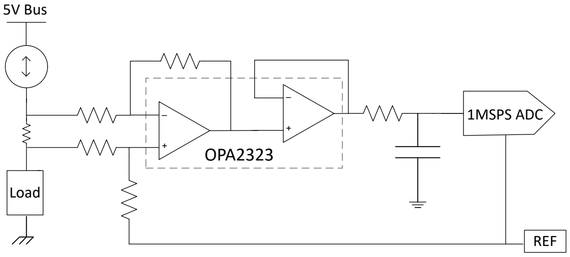
OPAx323 具有 2μV/°C 的最大温漂、5.5nV/rt-Hz 热本底噪声以及最小 100dB 的 CMRR，因此可在惠斯通电桥等高增益电压检测应用中轻松提供精密性能。这种更高精度（低失调电压、漂移、噪声、失真和 CMRR）和更高增益带宽（快速稳定和转换）的独特组合支持此类器件用于多种应用，例如电机旋转编码器、麦克风音频前置放大器和超声波传感器。

OPAx323 实现了 33V/μs 的高压摆率，可在电机电流检测应用中快速检测故障。与传统放大器不同，零交叉输入级可在低侧和高侧检测应用中提供相同的精度性能，因此 OPAx323 成为各种终端设备（例如太阳能串式逆变器、电力输送、电网和电动汽车基础设施）中用于电流检测的理想选择。OPAx323S 器件提供关断功能，可进一步降低功耗，并有助于在空闲时禁用放大器。该系列的所有通道型号均采用标准和小尺寸的引线和 QFN 封装。

器件信息

器件型号(1)	通道数	封装(4)	封装尺寸(5)
OPA323	单通道	DBV（SOT-23，5）(3)	2.9mm x 2.8mm
		DCK（SC70，5）	2mm x 1.25mm
		DRL（SOT-5X3，5）(3)	1.6mm x 1.6mm
OPA323S (2)	单通道，关断	DBV（SOT-23，6）(3)	2.9mm x 2.8mm
		DCK（SC70，6）(3)	2mm x 1.25mm
OPA2323	双通道	D（SOIC，8）	4.9mm × 6mm
		DDF（SOT-23，8）	2.9mm × 2.8mm
		DSG（WSON，8）(3)	2mm × 2mm
		DGK（VSSOP，8）	3mm × 4.9mm
		PW（TSSOP，8）(3)	3mm × 6.4mm
OPA2323S (2)	双通道，关断	RUG（X2QFN，10）(3)	1.5mm x 2mm
OPA4323	四通道	D（SOIC，14）(3)	8.65mm × 6mm
		PW（TSSOP，14）	5mm × 6.4mm
		RUC（X2QFN，14）(3)	2mm × 2mm
		DYY（SOT-23，14）	4.2mm × 3.26mm
OPA4323S (2)	四通道，关断	RTE（WQFN，16）(3)	3mm × 3mm

(1) 请参阅节 4。
(2) 器件型号仅为预发布状态。
(3) 封装仅为预发布状态。
(4) 有关更多信息，请参阅节 11。
(5) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



双向高侧电流检测放大器和 ADC 驱动器

English Data Sheet: SBOSAE8

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4 Device Comparison Table

DEVICE	NO. OF CHANNELS	SHDN	PACKAGE LEADS										
			SC70 DCK	SOIC D	SOT-23 DBV(2)	SOT-23 DDF	SOT-553 DRL(2)	SOT-23 DYY	TSSOP PW	VSSOP DGK	WQFN RTE (2)	WSON DSG(2)	X2QFN RUG(2)
OPA323	1	NO	5	—	5	—	5	—	—	—	—	—	—
OPA323S(1)	1	YES	6	—	6	—	—	—	—	—	—	—	—
OPA2323	2	NO	—	8	—	8	—	—	8	8	—	8	—
OPA2323S(1)	2	YES	—	—	—	—	—	—	—	—	—	—	10
OPA4323	4	NO	—	14	—	—	—	14	14	—	—	—	—
OPA4323S	4	YES	—	—	—	—	—	—	—	—	16	—	—

(1) Devices are preview only.
(2) Packages are preview only.

5 Pin Configuration and Functions

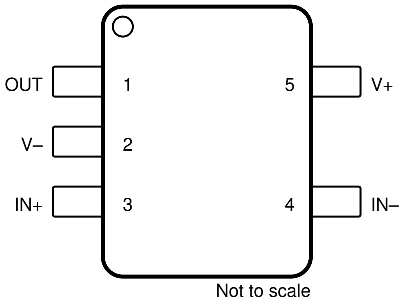

图 5-1. OPA323 DBV Package, 5-Pin SOT-23 (Top View)

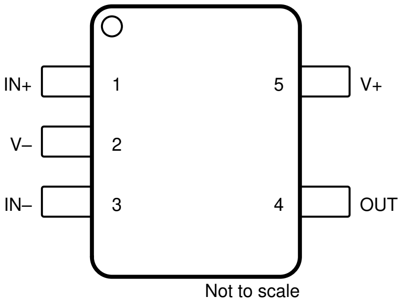

图 5-2. OPA323 DCK and DRL Package, 5-Pin SC70 and 5-Pin SOT-5X3 (Top View)

表 5-1. Pin Functions: OPA323

PIN			TYPE[1]	DESCRIPTION
NAME	SOT-23	SC70, SOT-5X3		
IN –	4	3	I	Inverting input
IN+	3	1	I	Noninverting input
OUT	1	4	O	Output
V –	2	2	I	Negative (low) supply or ground (for single-supply operation)
V+	5	5	I	Positive (high) supply

(1) I = input, O = output

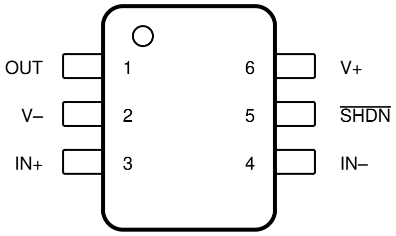

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图 5-3. OPA323S DBV Package, 6-Pin SOT-23 (Top View)

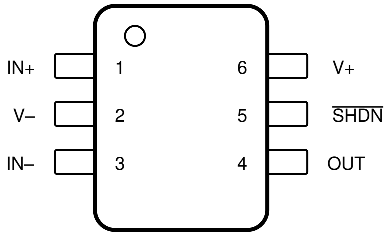

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图 5-4. OPA323S DCK Package, 6-Pin SC70 (Top View)

表 5-2. Pin Functions: OPA323S

PIN			TYPE[1]	DESCRIPTION
NAME	SOT-23	SC70		
IN –	4	3	I	Inverting input
IN+	3	1	I	Noninverting input
OUT	1	4	O	Output
$\overline{\text{SHDN}}$	5	5	I	Shutdown: low = amp disabled, high = amp enabled See *Shutdown Function* for more information
V –	2	2	I	Negative (low) supply or ground (for single-supply operation)
V+	6	6	I	Positive (high) supply

(1) I = input, O = output

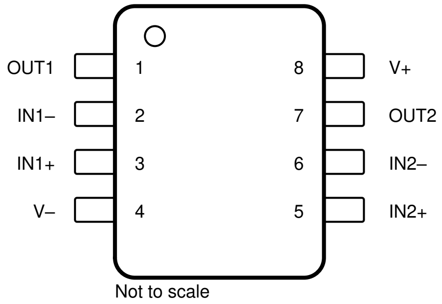
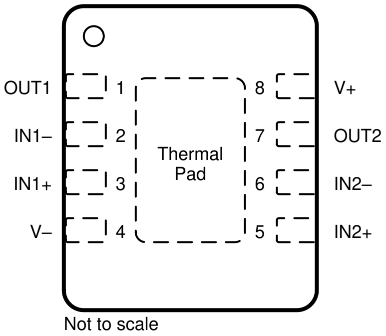


图 5-5. OPA2323 D, PW, DGK, and DDF Package, SOIC, TSSOP, VSSOP, and SOT-23-THIN (Top View)



Connect exposed thermal pad to V – . For more information, see *Packages with an Exposed Thermal Pad*.

图 5-6. OPA2323 DSG Package, 8-Pin WSON with Exposed Thermal Pad (Top View)

表 5-3. Pin Functions: OPA2323

PIN		TYPE[1]	DESCRIPTION
NAME	SOIC, TSSOP, VSSOP, SOT-23-THIN, WSON		
IN1 –	2	I	Inverting input, channel 1
IN1+	3	I	Noninverting input, channel 1
IN2 –	6	I	Inverting input, channel 2
IN2+	5	I	Noninverting input, channel 2
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
V –	4	I	Negative (low) supply or ground (for single-supply operation)
V+	8	I	Positive (high) supply

(1) I = input, O = output

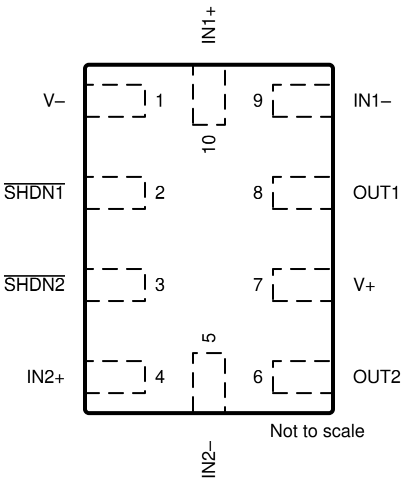


图 5-7. OPA2323S RUG Package
10-Pin X2QFN
(Top View)

表 5-4. Pin Functions: OPA2323S

PIN		TYPE[1]	DESCRIPTION
NAME	X2QFN		
IN1 –	9	I	Inverting input, channel 1
IN1+	10	I	Noninverting input, channel 1
IN2 –	5	I	Inverting input, channel 2
IN2+	4	I	Noninverting input, channel 2
OUT1	8	O	Output, channel 1
OUT2	6	O	Output, channel 2
SHDN1	2	I	Shutdown: low = amp disabled, high = amp enabled, channel 1. For more information, see *Shutdown Function*.
SHDN2	3	I	Shutdown: low = amp disabled, high = amp enabled, channel 2 For more information, see *Shutdown Function*.
V –	1	I	Negative (low) supply or ground (for single-supply operation)
V+	7	I	Positive (high) supply

(1) I = input, O = output

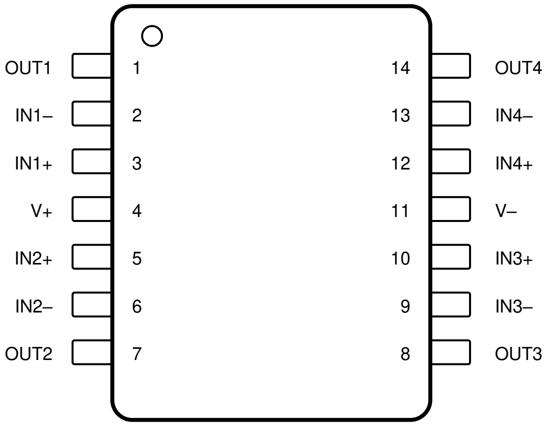


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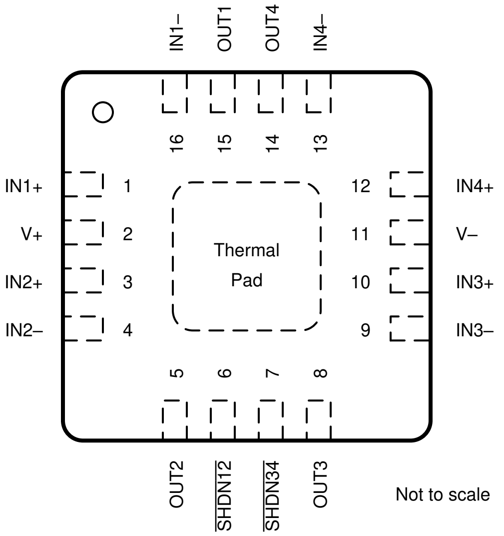
图 5-8. OPA4323 D, PW and DYY Package, 14-Pin SOIC, TSSOP, SOT-23-THN (Top View)

表 5-5. Pin Functions: OPA4323

PIN		TYPE[(1)]	DESCRIPTION
NAME	SOIC, TSSOP		
IN1 –	2	I	Inverting input, channel 1
IN1+	3	I	Noninverting input, channel 1
IN2 –	6	I	Inverting input, channel 2
IN2+	5	I	Noninverting input, channel 2
IN3 –	9	I	Inverting input, channel 3
IN3+	10	I	Noninverting input, channel 3
IN4 –	13	I	Inverting input, channel 4
IN4+	12	I	Noninverting input, channel 4
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
OUT3	8	O	Output, channel 3
OUT4	14	O	Output, channel 4
V –	11	I	Negative (low) supply or ground (for single-supply operation)
V+	4	I	Positive (high) supply

(1) I = input, O = output



A. Connect thermal pad to V – .

图 5-9. OPA4323S RTE Package,
16-Pin WQFN With Exposed Thermal Pad
(Top View)

表 5-6. Pin Functions: OPA4323S

PIN		TYPE[1]	DESCRIPTION
NAME	WQFN		
IN1+	1	I	Noninverting input, channel 1
IN1 –	16	I	Inverting input, channel 1
IN2+	3	I	Noninverting input, channel 2
IN2 –	4	I	Inverting input, channel 2
IN3+	10	I	Noninverting input, channel 3
IN3 –	9	I	Inverting input, channel 3
IN4+	12	I	Noninverting input, channel 4
IN4 –	13	I	Inverting input, channel 4
$\overline{\text{SHDN12}}$	6	I	Shutdown: low = amp disabled, high = amp enabled, channel 1 and 2. For more information, see *Shutdown Function*.
$\overline{\text{SHDN34}}$	7	I	Shutdown: low = amp disabled, high = amp enabled, channel 3 and 4. For more information, see *Shutdown Function*.
OUT1	15	O	Output, channel 1
OUT2	5	O	Output, channel 2
OUT3	8	O	Output, channel 3
OUT4	14	O	Output, channel 4
V –	11	I	Negative (low) supply or ground (for single-supply operation)
V+	2	I	Positive (high) supply

(1) I = input, O = output

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)	Supply voltage, V_S = (V+) – (V–)	0	7.0	V
Signal input pins	Common-mode voltage (2) (3)	–0.5	6.0	V
	Differential voltage (2) (3)		±6.0	V
	Current (3)	–10	10	mA
Output short-circuit (4)		Continuous		
Operating ambient temperature, T_A		–55	150	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Input pins can swing beyond (V+) as long as they stay with in 6V. No diode structure from input pins to (V+).
(3) Input pins are diode-clamped to (V–). Input signals that 0.3V below (V–) must be current-limited to 10mA or less.
(4) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)		±4000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	OPA4323	±500	V
			OPA323, OPA2323	±250	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage, (V+) – (V–)	1.7	5.5	V
C_{BYP}	Bypass capacitor on the power supply pins (1)	0.1		µF
T_A	Specified temperature	–40	125	°C

(1) For C_{BYP}, use low-ESR ceramic capacitors between each supply pin and ground. Only one C_{BYP} is sufficient for single supply operation. Ensure that C_{BYP} is placed as close to the device as possible and the supply trace routes through C_{BYP} before reaching the supply pin.

6.4 Thermal Information for Single Channel

THERMAL METRIC (1)		OPA323			OPA323S		UNIT
		DBV (2) (SOT-23)	DCK (SC70)	DRL (2) (SOT-5X3)	DBV (2) (SOT-23)	DCK (2) (SC70)	
		5 PINS	5 PINS	5 PINS	6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	189.3	196.7	TBD	168.8	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	86.9	104.5	TBD	87.8	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	55.9	44.8	TBD	49.3	TBD	°C/W
ψ_{JT}	Junction-to-top characterization parameter	23.7	18.7	TBD	25.6	TBD	°C/W
ψ_{JB}	Junction-to-board characterization parameter	55.5	44.5	TBD	49.0	TBD	°C/W

THERMAL METRIC (1)		OPA323			OPA323S		UNIT
		DBV (2) (SOT-23)	DCK (SC70)	DRL (2) (SOT-5X3)	DBV (2) (SOT-23)	DCK (2) (SC70)	
		5 PINS	5 PINS	5 PINS	6 PINS	6 PINS	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	TBD	n/a	TBD	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) This package option is preview.

6.5 Thermal Information for Dual Channel

THERMAL METRIC (1)		OPA2323					OPA2323S	UNIT
		D (SOIC	PW (2) (TSSOP)	DGK (VSSOP)	DDF (SOT-23-8)	DSG (2) (WSON)	RUG (2) (X2QFN)	
		8 PINS	8 PINS	8 PINS	8 PINS	8 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	139.0	TBD	173.6	149.6	TBD	144.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	81.2	TBD	65.1	72.9	TBD	47.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	82.4	TBD	95.1	68.4	TBD	76.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	31.3	TBD	10.0	4.0	TBD	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	81.6	TBD	93.5	68.1	TBD	75.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	TBD	n/a	n/a	TBD	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) This package option is preview.

6.6 Thermal Information for Quad Channel

THERMAL METRIC (1)		OPA4323			OPA4323S	UNIT
		D (2) (SOIC)	PW (TSSOP)	DYY (SOT)	RTE (2) (WQFN)	
		14 PINS	14 PINS	14 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	TBD	115.8	113.7	48.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	TBD	44.9	49.1	52.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	TBD	58.7	42.4	23.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	TBD	5.2	1.6	1.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	TBD	58.1	42.2	23.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	TBD	n/a	n/a	8.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) This package option is preview.

6.7 Electrical Characteristics

For V_S = (V+) – (V–) = 1.8V to 5.5V (±0.85V to ±2.75V) at T_A = 25°C, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_S = 1.8V to 5.5V			±0.15	±1.25	mV
		V_S = 1.8V to 5.5V	T_A = –40°C to 125°C			±1.35	
dV_{OS}/dT	Input offset voltage drift (1)	V_S = 1.8V to 5.5V	T_A = –40°C to 125°C		±0.4	±1.8	μV/℃
PSRR	Input offset voltage versus power supply	V_S = 1.8V to 5.5V			±5	±20	μV/V
	Channel separation	f = 10kHz			±1		μV/V
INPUT BIAS CURRENT							
I_B	Input bias current (1)	V_S = 1.8V and V_S = 5V			±0.5	±20	pA
		V_S = 1.8V and V_S = 5V	T_A = –40°C to 125°C			±1600	pA
I_{OS}	Input offset current (1)	V_S = 1.8V and V_S = 5V			±0.25		pA
		V_S = 1.8V and V_S = 5V	T_A = –40°C to 125°C			±120	pA
NOISE							
E_N	Input voltage noise	f = 0.1Hz to 10Hz			2.8		μV_{PP}
e_N	Input voltage noise density	f = 100Hz			24		nV/√Hz
		f = 1kHz			9		
		f = 10kHz			5.5		
i_N	Input current noise (2)	f = 1 kHz			20		fA/√Hz
INPUT VOLTAGE RANGE							
V_I	Input voltage range	V_S = 1.8V to 5.5V		(V–) – 0.2		(V+) + 0.15	V
CMRR	Common-mode rejection ratio	V_S = 5.5V, (V–) – 0.2V ≤ V_{CM} ≤ (V+) + 0.10V		100	114		dB
		V_S = 5.5V, (V–) – 0.2V ≤ V_{CM} ≤ (V+) + 0.15V		90	104		dB
		V_S = 5.5V, (V–) – 0.2V ≤ V_{CM} ≤ (V+) + 0.15V	T_A = –40°C to 125°C	84			dB
		V_S = 1.8V, (V–) – 0.1V ≤ V_{CM} ≤ (V+) + 0.05V		85	103		dB
		V_S = 1.8V, (V–) – 0.1V ≤ V_{CM} ≤ (V+) + 0.05V	T_A = –40°C to 125°C	80			dB
INPUT IMPEDANCE							
Z_{ID}	Differential				80 || 2		GΩ || pF
Z_{ICM}	Common-mode				100 || 1		GΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = 1.8V, (V–) + 0.1V < V_O < (V+) – 0.1V, R_L = 10kΩ to V_S / 2		103	120		dB
		V_S = 1.8V, (V–) + 0.2V < V_O < (V+) – 0.2V, R_L = 2kΩ to V_S / 2		100	115		dB
		V_S = 5.5V, (V–) + 0.1V < V_O < (V+) – 0.1V, R_L = 10kΩ to V_S / 2		112	125		dB
		V_S = 5.5V, (V–) + 0.2V < V_O < (V+) – 0.2V, R_L = 2kΩ to V_S / 2		108	120		dB
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product	V_S = 5.5V, G = +1, R_L = 10kΩ, C_L = 100pF	T_A = 25°C		20		MHz
SR	Slew rate	V_S = 5.5V, G = +1, V_{STEP} = 5V, R_L = 10kΩ, C_L = 100pF			33		V/μs
THD+N	Total harmonic distortion + noise (3)	V_S = 5V, G = +1, V_O = 4V_{P-P}, f = 10kHz, R_L = 600Ω to V_S / 2, C_L = 50pF			0.00125		%

6.7 Electrical Characteristics（续）

For V_S = (V+) – (V–) = 1.8V to 5.5V (±0.85V to ±2.75V) at T_A = 25°C, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_S	Settling time	To 0.1%, V_S = 5.5V, V_{STEP} = 4V, G = +1, C_L = 10pF			200		ns
		To 0.1%, V_S = 5.5V, V_{STEP} = 2V, G = +1, C_L = 10pF			150		
		To 0.01%, V_S = 5.5V, V_{STEP} = 4V, G = +1, C_L = 10pF			250		
		To 0.01%, V_S = 5.5V, V_{STEP} = 2V, G = +1, C_L = 10pF			200		
GM	Gain Margin	V_S = 5.5V, G = +1, R_L = 10kΩ, C_L = 30pF			15		dB
		V_S = 1.8V, G = +1, R_L = 10kΩ, C_L = 30pF			15		dB
PM	Phase Margin	V_S = 5.5V, G = +1, R_L = 10kΩ, C_L = 30pF			50		°
		V_S = 1.8V, G = +1, R_L = 10kΩ, C_L = 30pF			52.5		°
$t_{overload}$	Overload recovery time	V_{IN} × gain > V_S			130		ns
EMIRR	Electro-magnetic interference rejection ratio	f = 1.8GHz, V_{IN_EMIRR} = 100mV			62		dB
OUTPUT							
V_o	Voltage output swing from rail	V_S = 1.8V, R_L = 10kΩ to V_S / 2			15	25	mV
		V_S = 5.5V, R_L = 10kΩ to V_S / 2			25	35	mV
		V_S = 5.5V, R_L = 2kΩ to V_S / 2			45	55	mV
I_{SC}	Short-circuit current (4)	V_S = 1.8V		±20	±40		mA
		V_S = 5.5V		±80	±110		mA
Z_O	Open-loop output impedance	f = 10kHz			80		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	V_S = 5.5V, I_O = 0A			1.6	1.9	mA
			T_A = –40°C to 125°C			2.0	
	Power-on time	V_S = 0V to 5.5V, 90% I_Q Level			25		μs
SHUTDOWN							
I_{QSD}	Shutdown current per amplifier (7)	All amplifiers disabled, $\overline{SHDN}$ = V–			0.5	1	μA
		All amplifiers disabled, $\overline{SHDN}$ = V–, T_A = –40 ℃ to 125 ℃				1.5	μA
Z_{SHDN}	Output impedance during shutdown (7)	Amplifier disabled			43 || 11.5		GΩ || pF
V_{IH}	Logic high threshold voltage (amplifier enabled) (7)			(V–) + 1 V			V
V_{IL}	Logic low threshold voltage (amplifier disabled)					(V–) + 0.2 V	V
t_{ON}	Amplifier enable time (full shutdown) (5) (6) (7)	G = +1, V_{CM} = V_S / 2, V_O = 0.9 × V_S / 2, R_L connected to V–			1		μs
	Amplifier enable time (partial shutdown) (5) (6) (7)	G = +1, V_{CM} = V_S / 2, V_O = 0.9 × V_S / 2, R_L connected to V–			1		
t_{OFF}	Amplifier disable time (5) (7)	G = +1, V_{CM} = V_S / 2, V_O = 0.1 × V_S / 2, R_L connected to V–			1		μs

6.7 Electrical Characteristics （续）

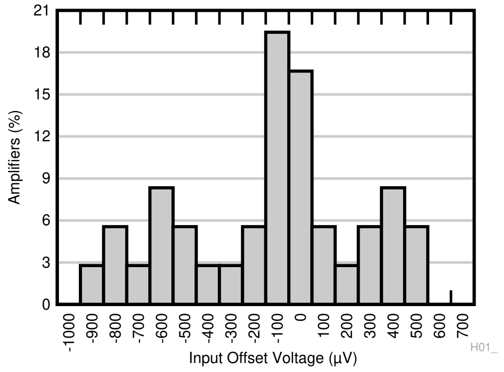
For V_S = (V+) – (V –) = 1.8V to 5.5V (±0.85V to ±2.75V) at T_A = 25°C, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	$\overline{SHDN}$ pin input bias current (per pin) (7)	(V+) ≥ $\overline{SHDN}$ ≥ (V –) + 1V		50		nA
		(V –) ≤ $\overline{SHDN}$ ≤ (V –) + 0.2V		100		

(1) Max or min limit is specified based on characterization results.
(2) Typical input current noise data to be specified based on design simulation results
(3) Third-order filter; bandwidth = 80kHz at – 3dB.
(4) Short circuit current specified here is average of sourcing and sinking short circuit currents
(5) Disable time (t_{OFF}) and enable time (t_{ON}) are defined as the time interval between the 50% point of the signal applied to the $\overline{SHDN}$ pin and the point at which the output voltage reaches the 10% (disable) or 90% (enable) level.
(6) Full shutdown refers to the dual device having both channels 1 and 2 disabled ($\overline{SHDN1}$ = $\overline{SHDN2}$ = V –) and the quad device having all channels 1 to 4 disabled ($\overline{SHDN12}$ = $\overline{SHDN34}$ = V –). For partial shutdown, only one $\overline{SHDN}$ pin is exercised; in this mode, the internal biasing circuitry remains operational and the enable time is shorter.
(7) Shutdown section is on preview

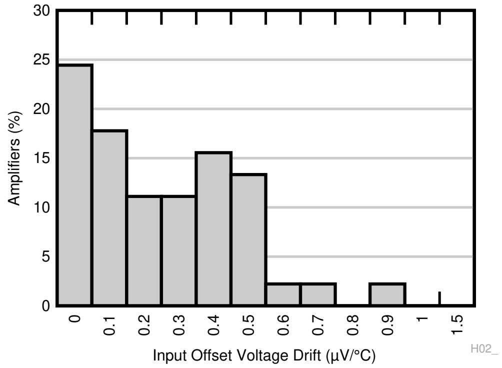
6.8 Typical Characteristics

at T_A = 25°C, V+ = 2.75V, V– = –2.75V, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



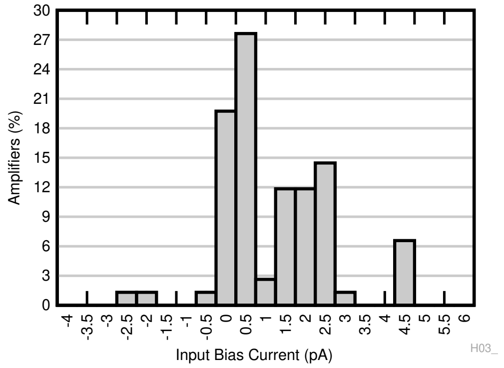
V_S = 5.5V V_{CM} = V_S / 2 T_A = 25°C
No. of devices = 36 Mean = –32µV Sigma = 190µV

图 6-1. Input Offset Voltage Distribution Histogram



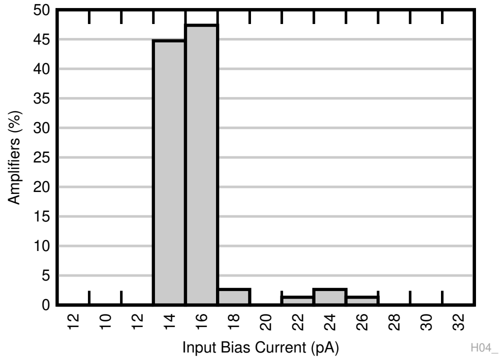
V_S = 5.5V V_{CM} = V_S / 2 T_A = –40°C to +125°C
No. of devices = 36
Mean = 0.28µV/°C Sigma = 0.22µV/°C

图 6-2. Input Offset Voltage Drift Distribution Histogram



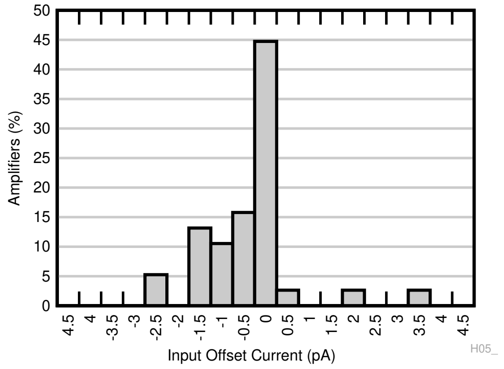
V_S = 5.5V V_{CM} = V_S / 2 T_A = 25°C
No. of devices = 90 Mean = 1pA Sigma = 2pA

图 6-3. Input Bias Current Distribution Histogram



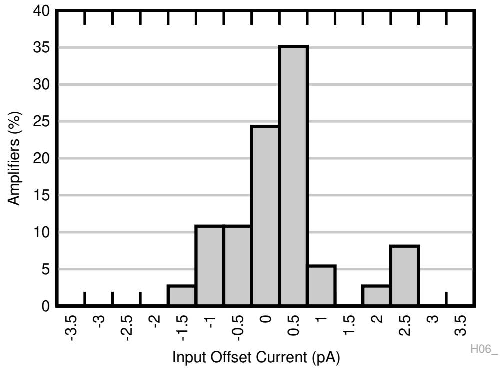
V_S = 5.5V V_{CM} = V_S / 2 T_A = 85°C
No. of devices = 90 Mean = 13pA Sigma = 2pA

图 6-4. Input Bias Current Distribution Histogram



V_S = 5.5V V_{CM} = V_S / 2 T_A = 25°C
No. of devices = 45 Mean = –0.1pA Sigma = 1.7pA

图 6-5. Input Offset Current Distribution Histogram

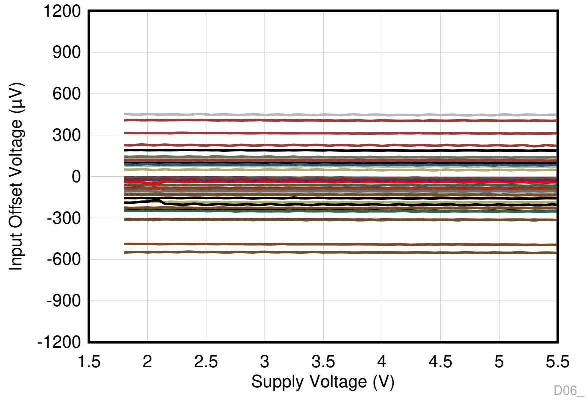


V_S = 5.5V V_{CM} = V_S / 2 T_A = 85°C
No. of devices = 45 Mean = 1.1pA Sigma = 2.1pA

图 6-6. Input Offset Current Distribution Histogram

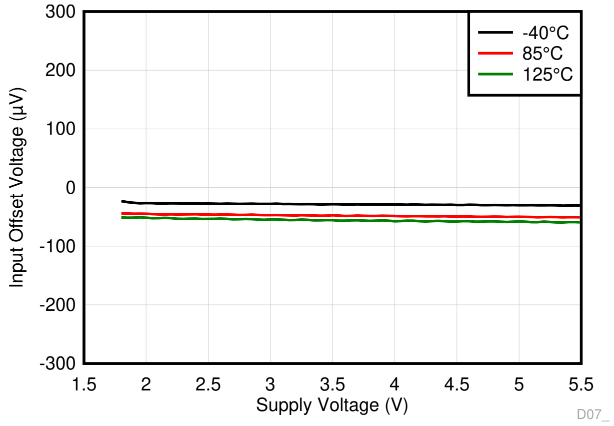
6.8 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75V, V– = –2.75V, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



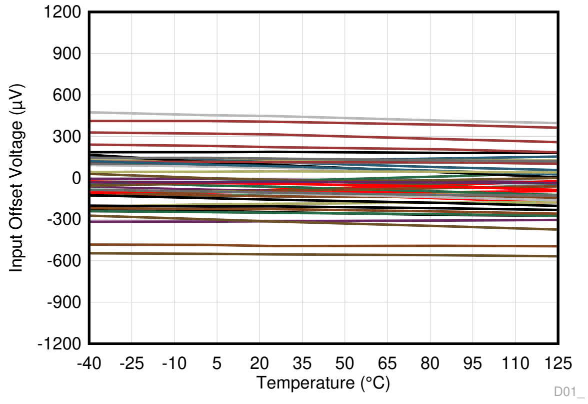
V_{CM} = (V–)   No. of devices = 45

图 6-7. Input Offset Voltage vs Supply Voltage



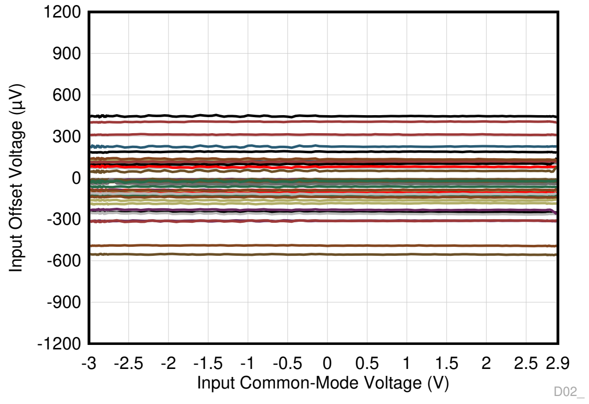
V_{CM} = (V–) T_A = –40°C, 85°C and 125°C

图 6-8. Input Offset Voltage vs Supply Voltage



V_{CM} = V–   No. of devices = 45

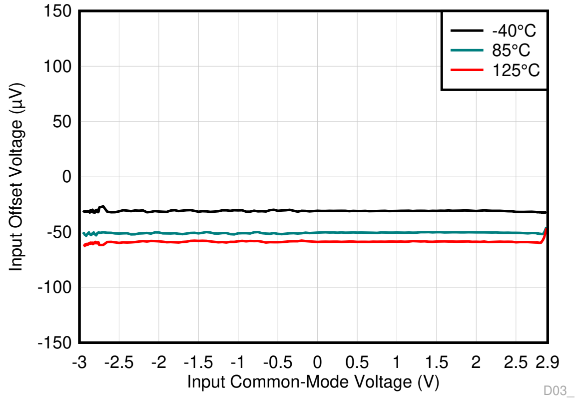
图 6-9. Input Offset Voltage vs Temperature



V+ = 2.75V, V– = –2.75V   No. of devices = 45

(V–) – 0.25V < V_{CM} < (V+) + 0.15V

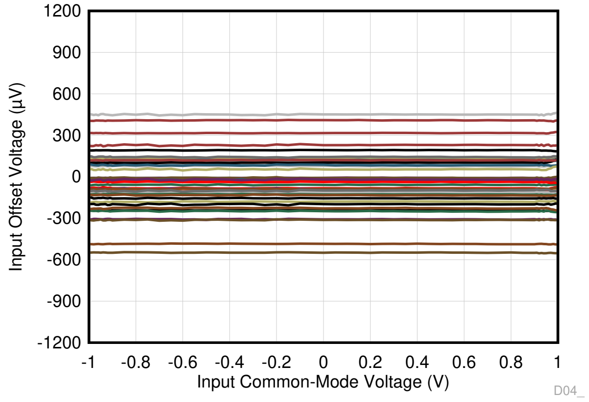
图 6-10. Input Offset Voltage vs Common-Mode



V+ = 2.75V, V– = –2.75V T_A = –40°C, 85°C and 125°C

(V–) – 0.25V < V_{CM} < (V+) + 0.15V

图 6-11. Input Offset Voltage vs Common-Mode



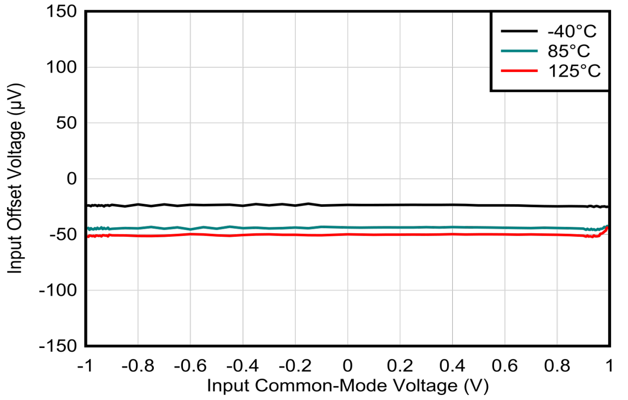
V+ = 0.9V, V– = –0.9V   No. of devices = 45

(V–) – 0.1V < V_{CM} < (V+) + 0.1V

图 6-12. Input Offset Voltage vs Common-Mode

6.8 Typical Characteristics (continued)

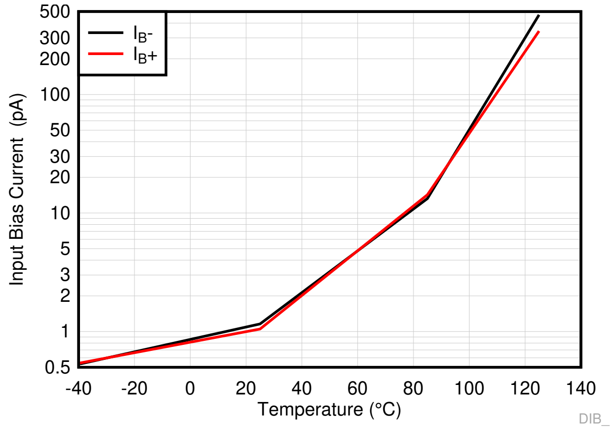
at T_A = 25°C, V+ = 2.75V, V– = –2.75V, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



V+ = 0.9V, V– = –0.9V T_A = –40°C, 85°C and 125°C

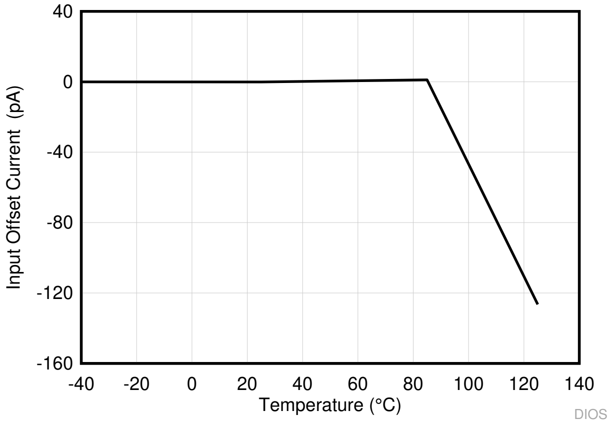
(V–) – 0.1V < V_{CM} < (V+) + 0.1V

图 6-13. Input Offset Voltage vs Common-Mode



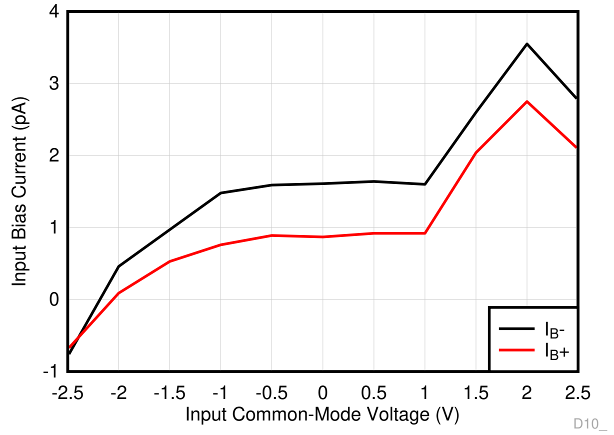
V_S = 5.5V, V_{CM} = V_S/2

图 6-14. I_B vs Temperature



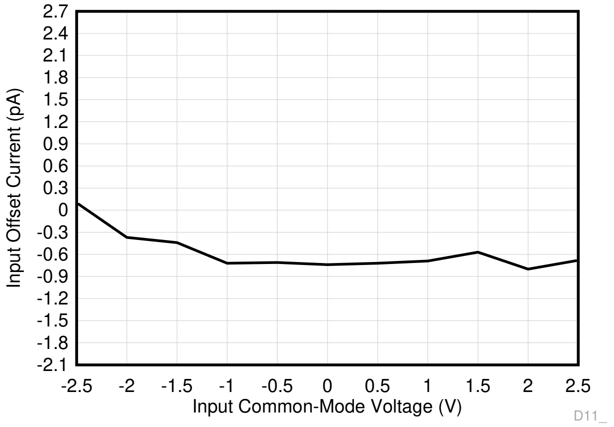
V_S = 5.5V, V_{CM} = V_S/2

图 6-15. I_{OS} vs Temperature



V+ = 2.5V, V– = –2.5V, V_{CM} = V_S/2

图 6-16. I_B vs Common-Mode Voltage



V+ = 2.5V, V– = –2.5V, V_{CM} = V_S/2

图 6-17. I_{OS} vs Common-Mode Voltage

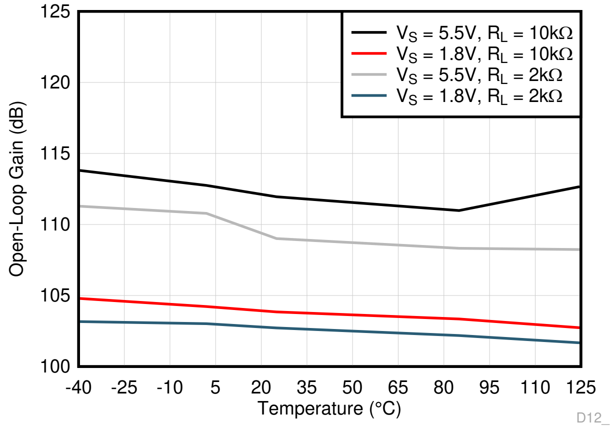
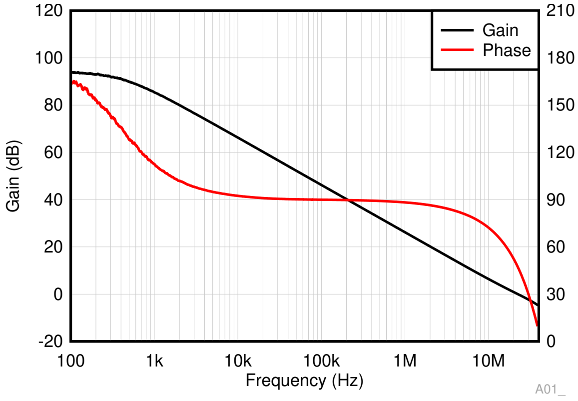


图 6-18. Open-Loop Gain vs Temperature

6.8 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75V, V– = –2.75V, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



C_L = 10pF

图 6-19. Open-Loop Gain and Phase vs Frequency

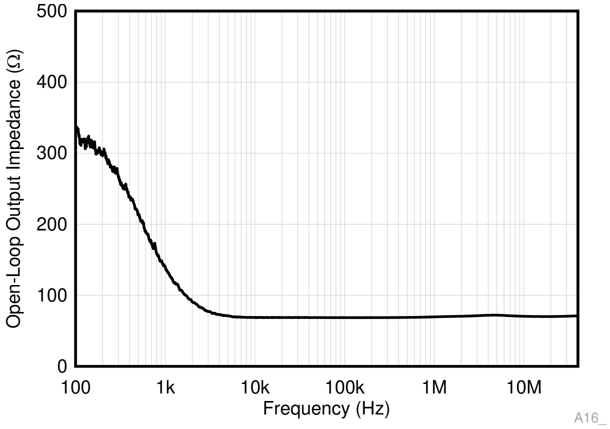
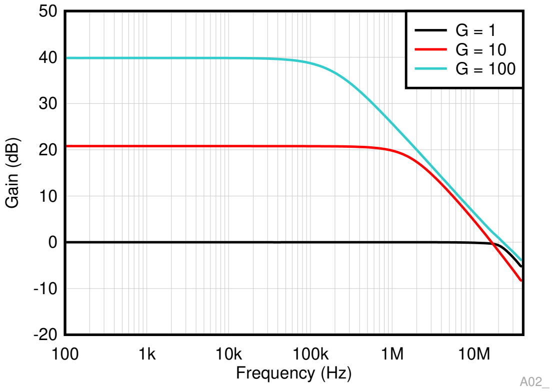
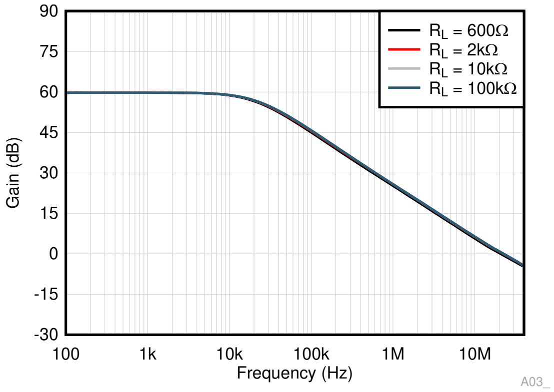


图 6-20. Open-Loop Output Impedance vs Frequency



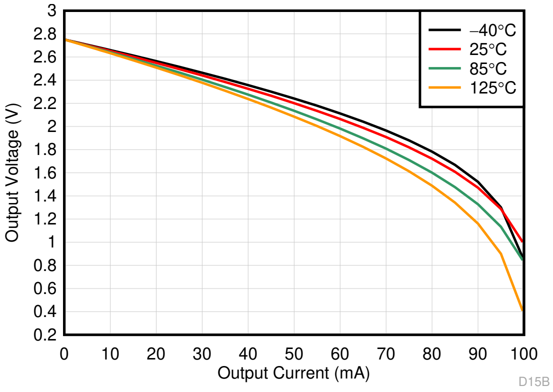
C_L = 10pF

图 6-21. Closed-Loop Gain vs Frequency



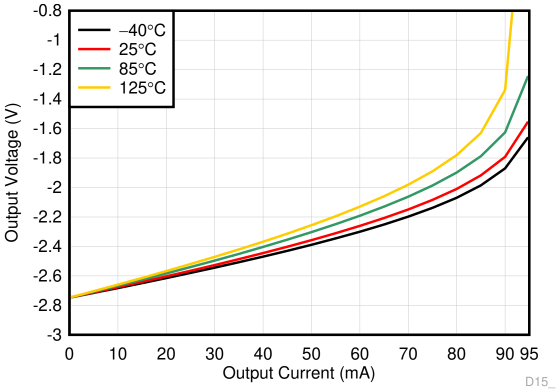
G = 1000 | C_L = 10pF

图 6-22. Closed-Loop Gain vs Frequency



V+ = 2.75V, V– = –2.75V

图 6-23. Output Voltage Swing vs Output Current (Sourcing)

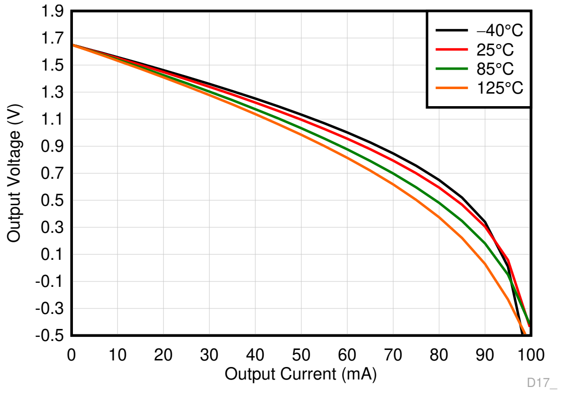


V+ = 2.75V, V– = –2.75V

图 6-24. Output Voltage Swing vs Output Current (Sinking)

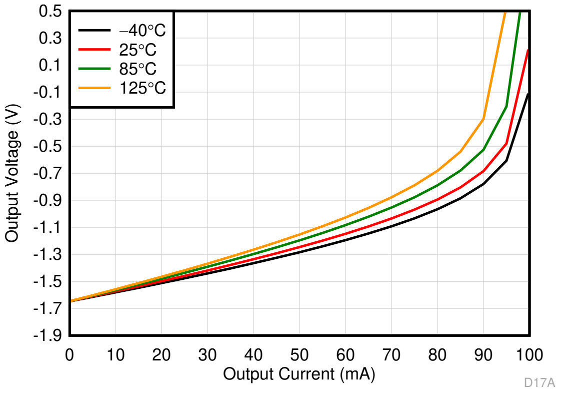
6.8 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75V, V– = –2.75V, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



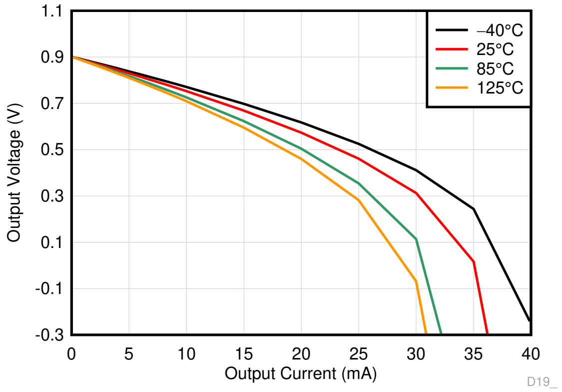
V+ = 1.65V, V– = –1.65V

图 6-25. Output Voltage Swing vs Output Current (Sourcing)



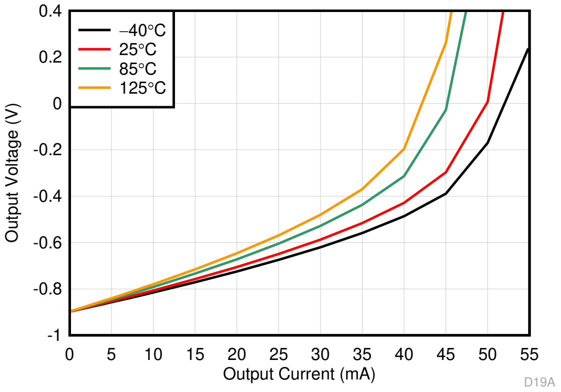
V+ = 1.65V, V– = –1.65V

图 6-26. Output Voltage Swing vs Output Current (Sinking)



V+ = 0.9V, V– = –0.9V

图 6-27. Output Voltage Swing vs Output Current (Sourcing)



V+ = 0.9V, V– = –0.9V

图 6-28. Output Voltage Swing vs Output Current (Sinking)

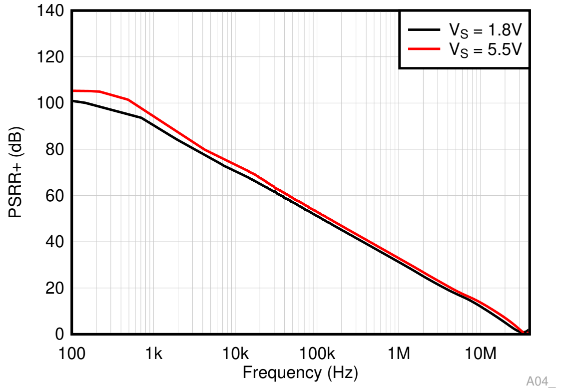


图 6-29. PSRR+ vs Frequency

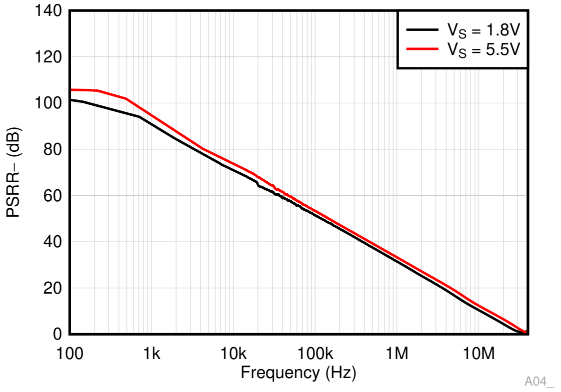
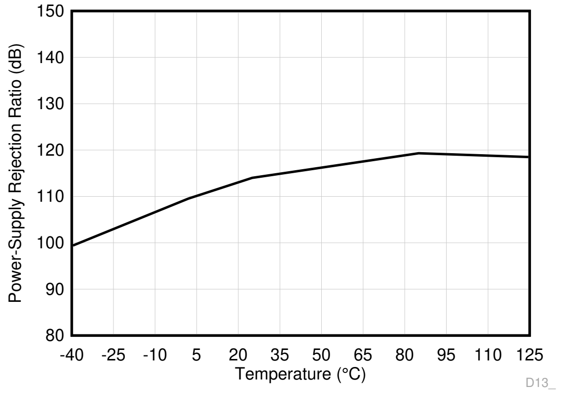


图 6-30. PSRR– vs Frequency

6.8 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75V, V– = –2.75V, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



V_{CM} = (V–) V_S = 1.8V to 5.5V

图 6-31. DC PSRR vs Temperature

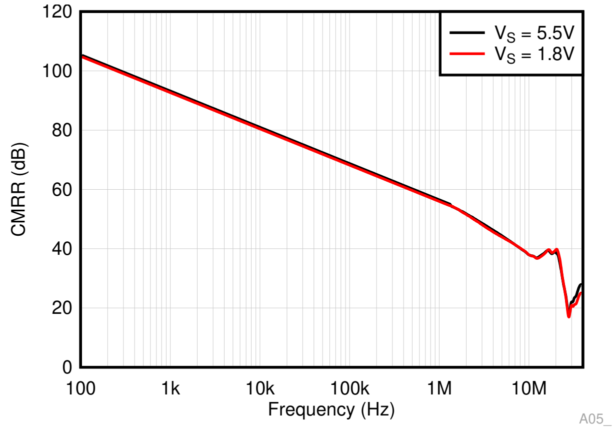
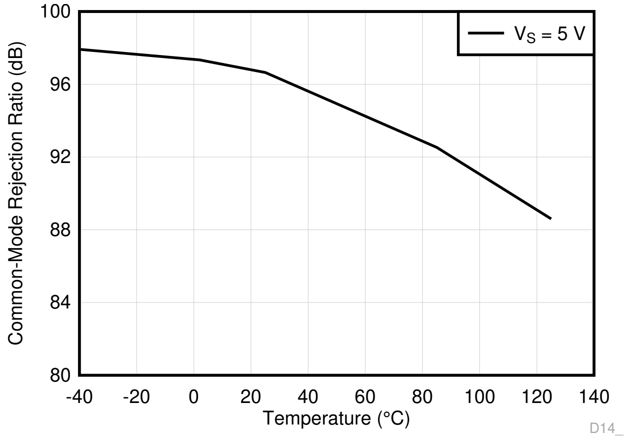


图 6-32. CMRR vs Frequency



V_S = 5V (V–) – 0.2V – < V_{CM} < (V+) + 0.15V

图 6-33. DC CMRR vs Temperature

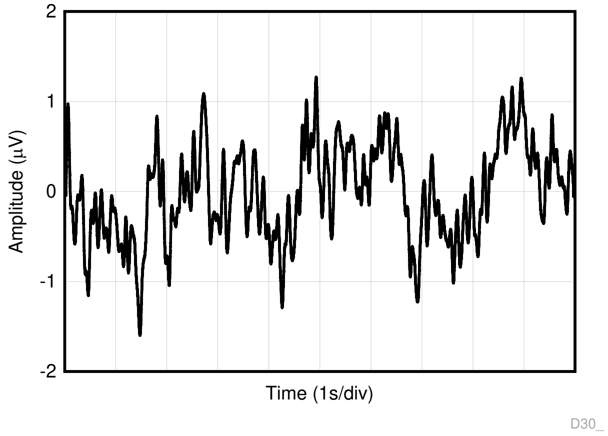


图 6-34. 0.1Hz to 10Hz Voltage Noise in Time Domain

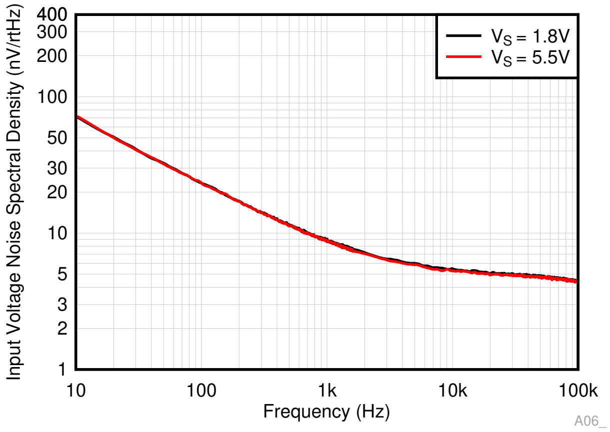
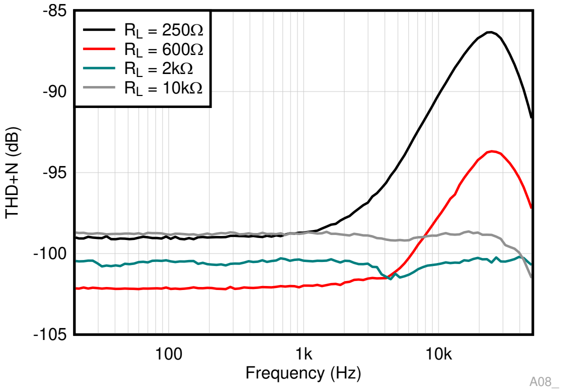


图 6-35. Input Voltage Noise Spectral Density

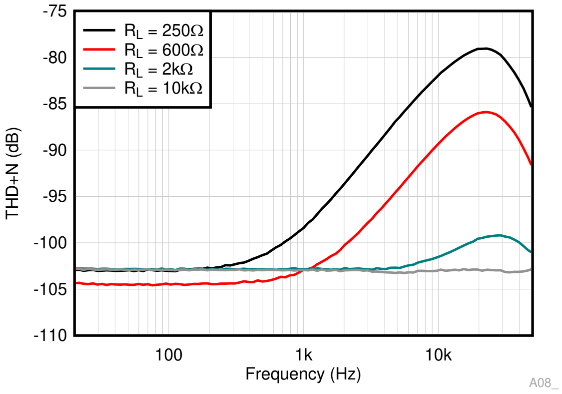


V_S = 5V V_{CM} = 2.5V G = 1
BW = 80kHz V_{OUT} = $2V_{P-P}$

图 6-36. THD + N vs Frequency

6.8 Typical Characteristics (continued)

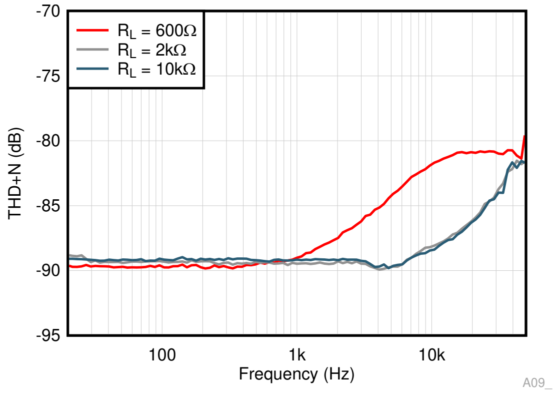
at T_A = 25°C, V+ = 2.75V, V– = –2.75V, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



V_S = 5V V_{CM} = 2.5V G = –1

BW = 80kHz V_{OUT} = $2V_{P-P}$

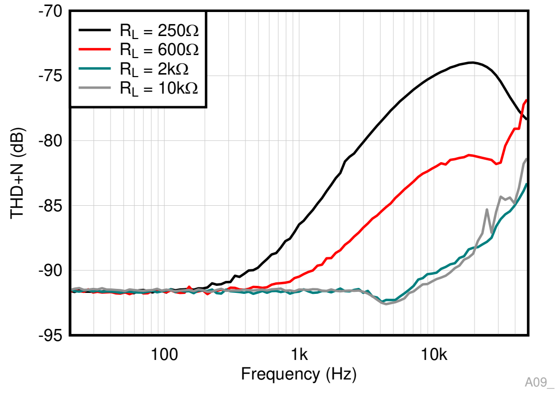
图 6-37. THD + N vs Frequency



V_S = 5V V_{CM} = 2.5V G = 10

BW = 80kHz V_{OUT} = $2V_{P-P}$

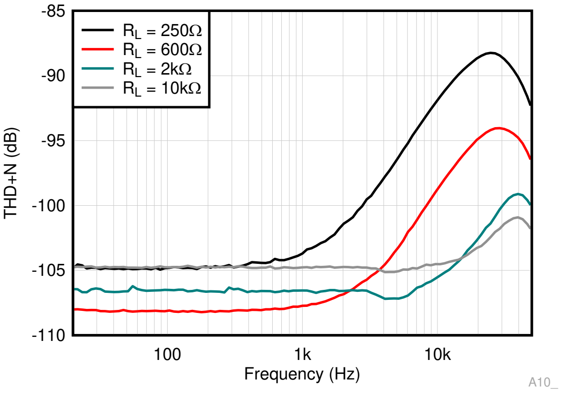
图 6-38. THD + N vs Frequency



V_S = 5V V_{CM} = 2.5V G = –10

BW = 80kHz V_{OUT} = $2V_{P-P}$

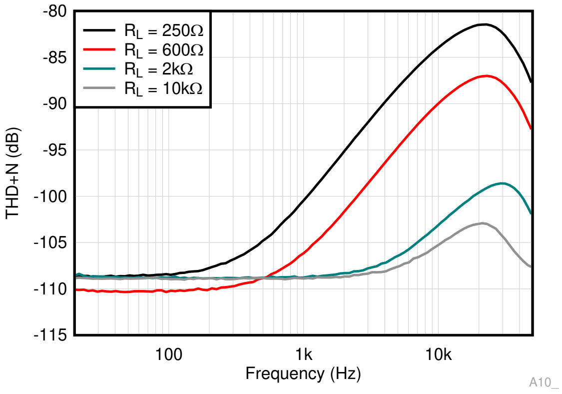
图 6-39. THD + N vs Frequency



V_S = 5V V_{CM} = 2.5V G = 1

BW = 80kHz V_{OUT} = $4V_{P-P}$

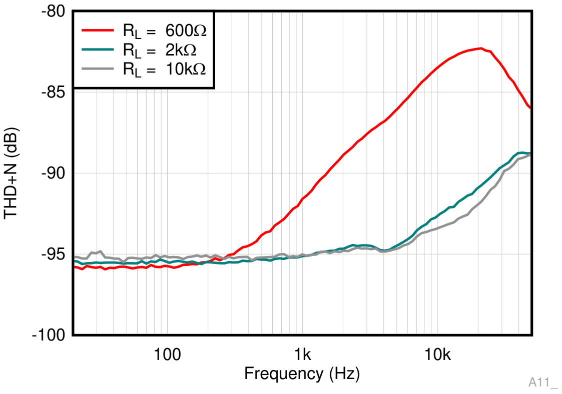
图 6-40. THD + N vs Frequency



V_S = 5V V_{CM} = 2.5V G = –1

BW = 80kHz V_{OUT} = $4V_{P-P}$

图 6-41. THD + N vs Frequency



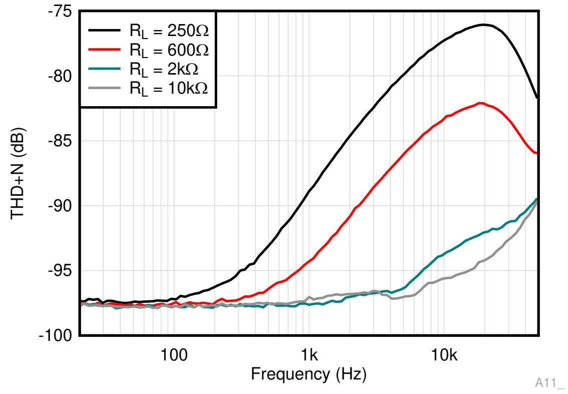
V_S = 5V V_{CM} = 2.5V G = 10

BW = 80kHz V_{OUT} = $4V_{P-P}$

图 6-42. THD + N vs Frequency

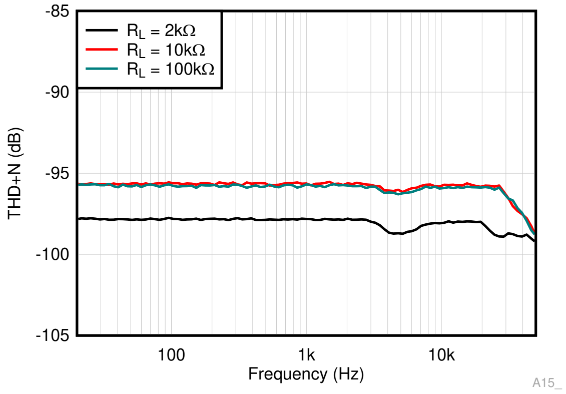
6.8 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75V, V– = –2.75V, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



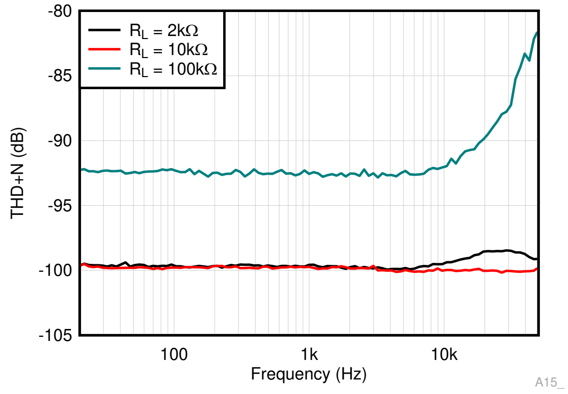
V_S = 5V V_{CM} = 2.5V G = –10
BW = 80kHz V_{OUT} = 4V_{P-P}

图 6-43. THD + N vs Frequency



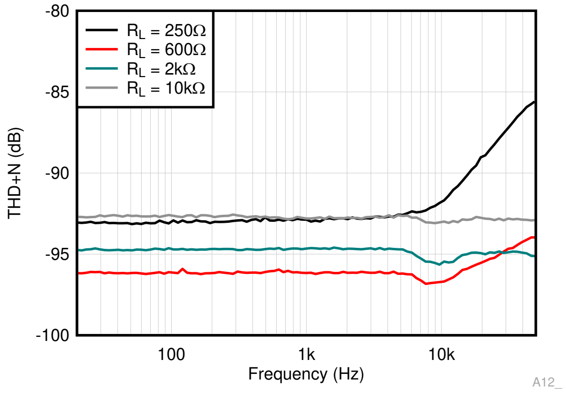
V_S = 5V V_{CM} = 2.5V G = 1
BW = 80kHz V_{OUT} = 1.4V_{P-P}

图 6-44. THD + N vs Frequency



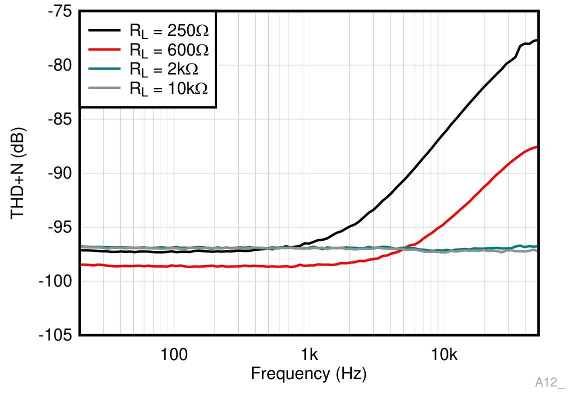
V_S = 5V V_{CM} = 2.5V G = –1
BW = 80kHz V_{OUT} = 1.4V_{P-P}

图 6-45. THD + N vs Frequency



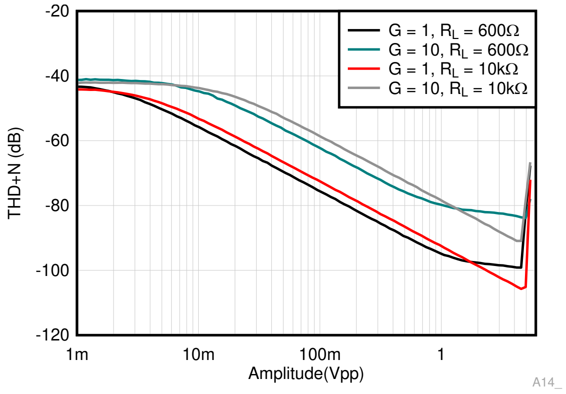
V_S = 3.3V V_{CM} = 1.65V G = 1
BW = 80kHz V_{OUT} = 1V_{P-P}

图 6-46. THD + N vs Frequency



V_S = 3.3V V_{CM} = 1.65V G = –1
BW = 80kHz V_{OUT} = 1V_{P-P}

图 6-47. THD + N vs Frequency

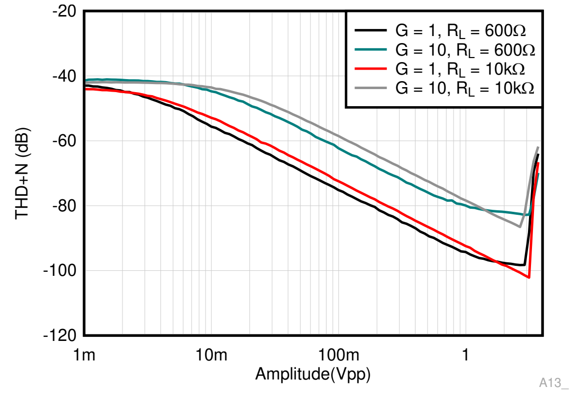


V_S = 5V V_{CM} = 2.5V f = 1kHz
BW = 80kHz

图 6-48. THD + N vs Amplitude

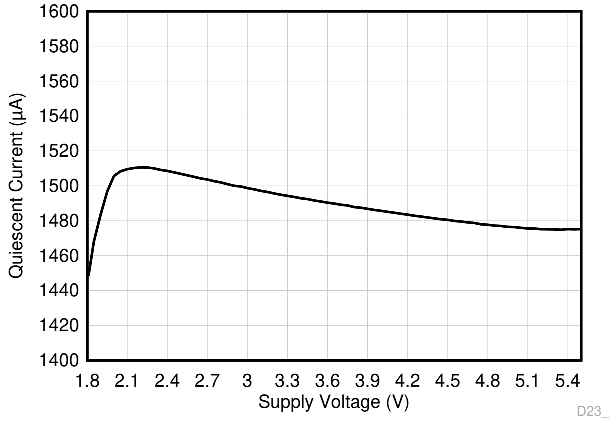
6.8 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75V, V– = –2.75V, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



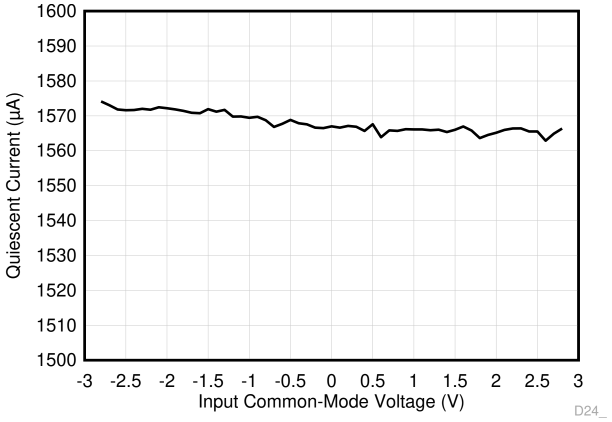
V_S = 3.3V V_{CM} = 1.65V f = 1kHz
BW = 80kHz

图 6-49. THD + N vs Amplitude



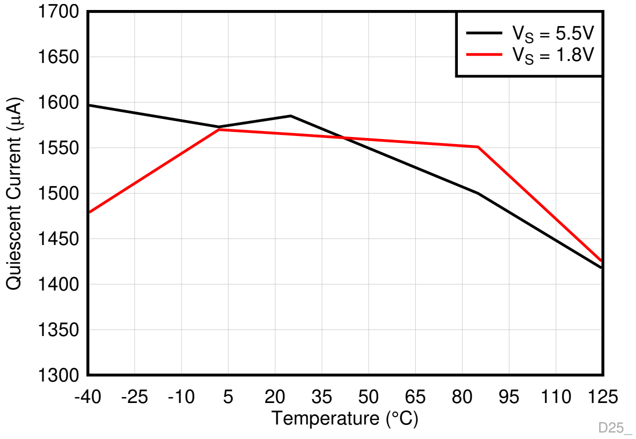
V_{CM} = V_S/2

图 6-50. Quiescent Current vs Supply Voltage



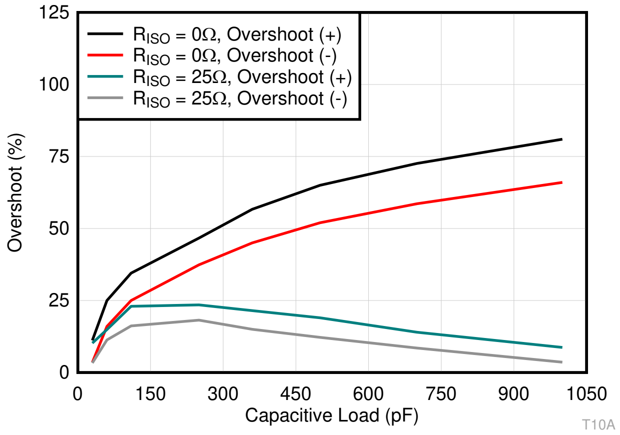
V+ = 2.75V, V– = –2.75V

图 6-51. Quiescent Current vs Common-Mode Voltage



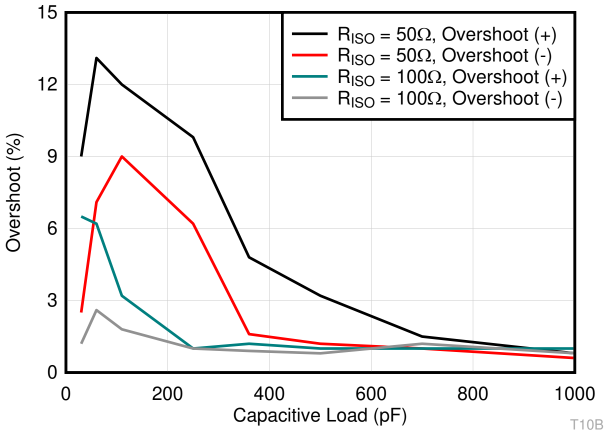
V_{CM} = V_S/2

图 6-52. Quiescent Current vs Temperature



G = 1 V_{IN} = 100mVpp

图 6-53. Small Signal Overshoot vs Capacitive Load



G = 1 V_{IN} = 100mVpp

图 6-54. Small Signal Overshoot vs Capacitive Load

6.8 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75V, V– = –2.75V, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

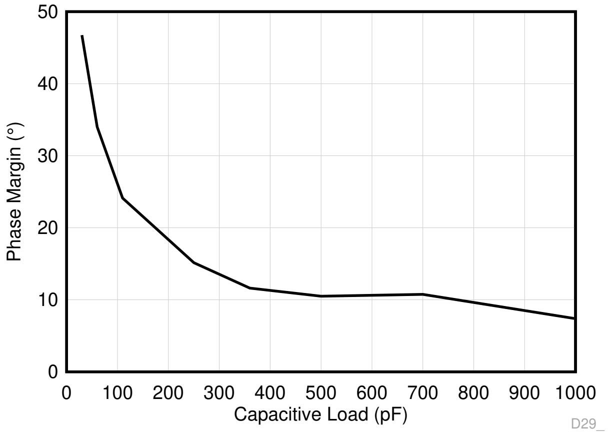
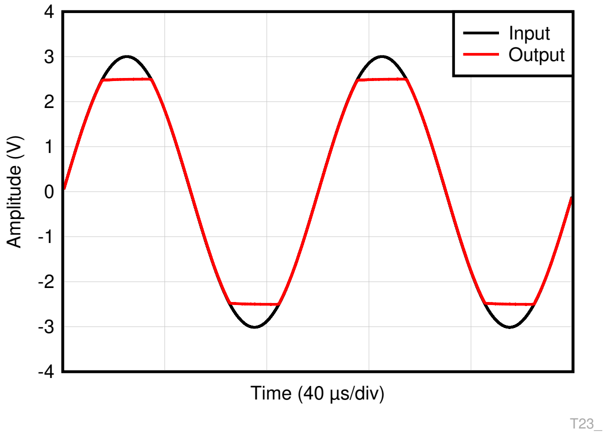
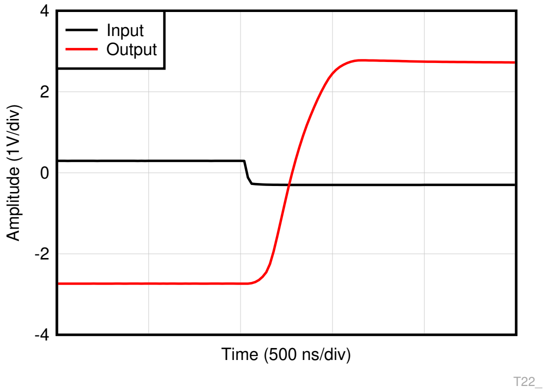


图 6-55. Phase Margin vs Capacitive Load



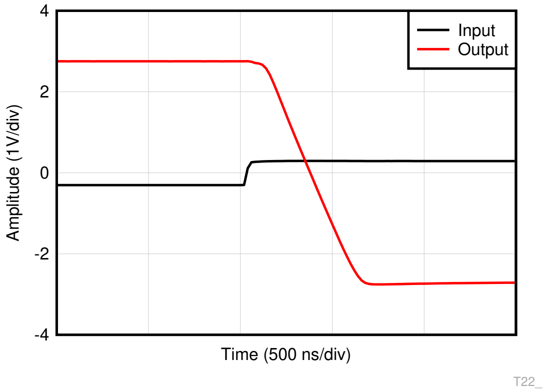
G = 1 V_{IN} = 6V_{PP}

图 6-56. No Phase Reversal



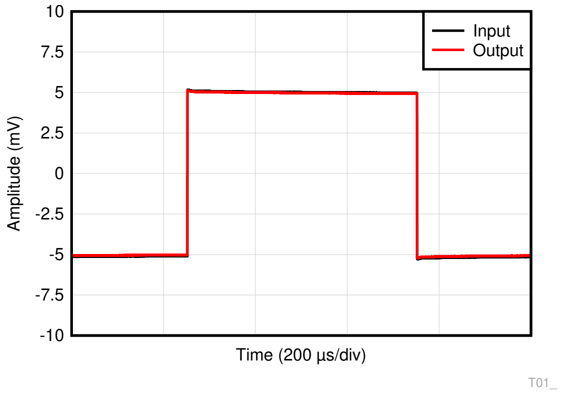
G = –10 V_{IN} = 600mV_{PP}

图 6-57. Overload Recovery



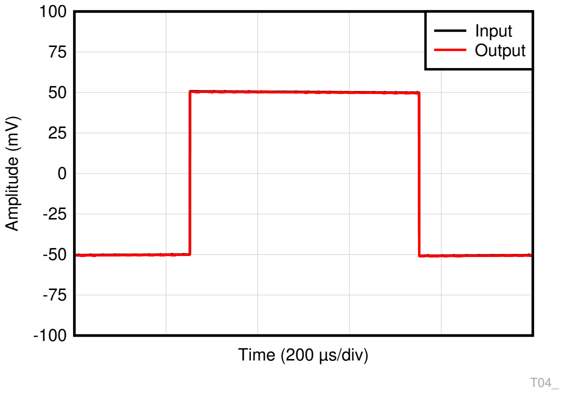
G = –10 V_{IN} = 600mV_{PP}

图 6-58. Overload Recovery



G = 1 V_{IN} = 10mV_{PP} C_L = 10pF

图 6-59. Small-Signal Step Response

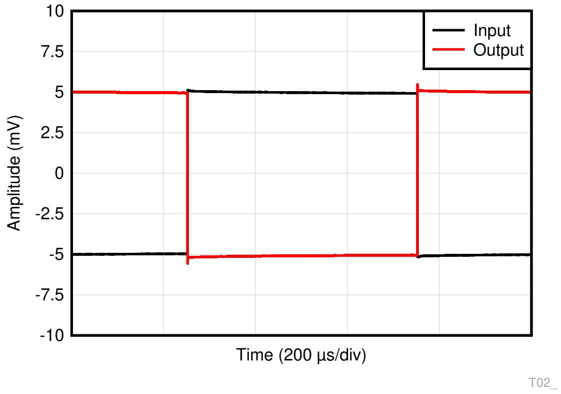


G = 1 V_{IN} = 100mV_{PP} C_L = 10pF

图 6-60. Small-Signal Step Response

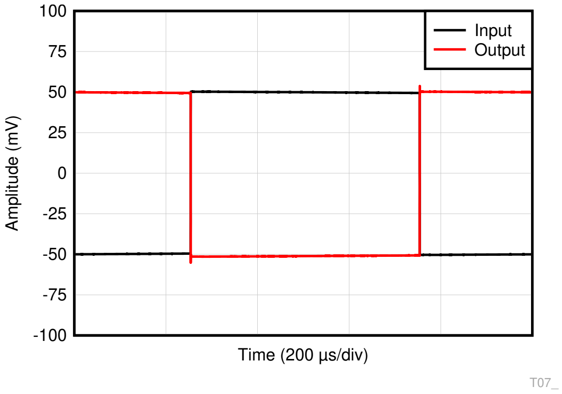
6.8 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75V, V– = –2.75V, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



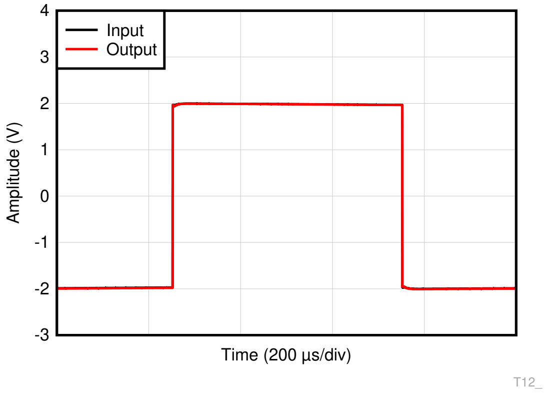
G = –1 V_{IN} = 10mV$_{PP}$ C_L = 10pF

图 6-61. Small-Signal Step Response



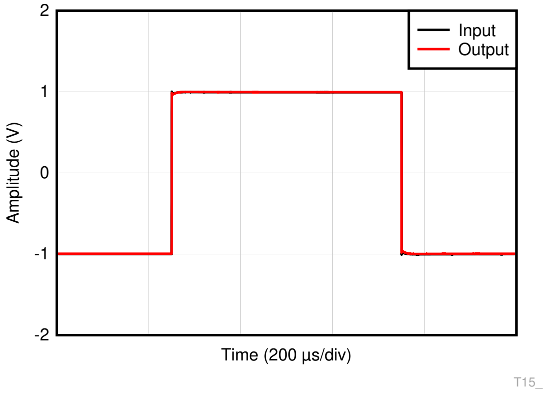
G = –1 V_{IN} = 100mV$_{PP}$ C_L = 10pF

图 6-62. Small-Signal Step Response



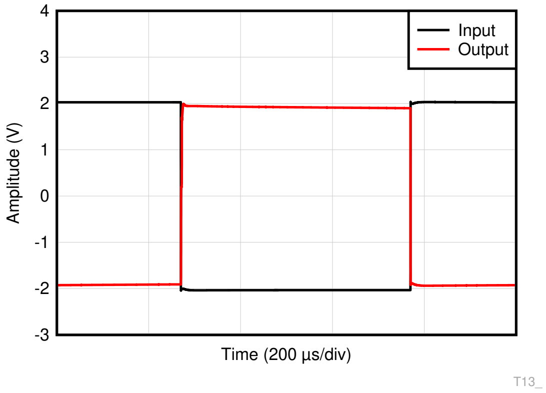
G = 1 V_{IN} = 4V$_{PP}$ C_L = 10pF

图 6-63. Large-Signal Step Response



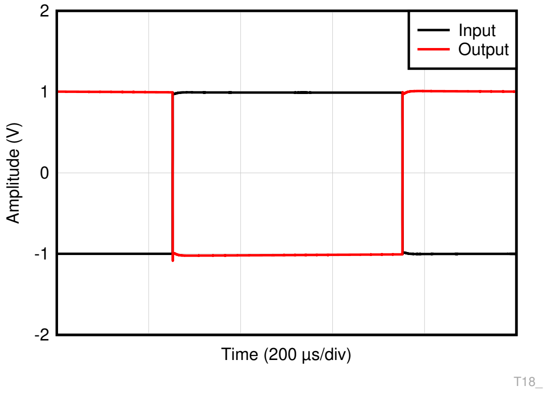
G = 1 V_{IN} = 2V$_{PP}$ C_L = 10pF
R_L = 2kΩ

图 6-64. Large-Signal Step Response



G = –1 V_{IN} = 4V$_{PP}$ C_L = 10pF

图 6-65. Large-Signal Step Response



G = –1 V_{IN} = 2V$_{PP}$ C_L = 10pF
R_L = 2kΩ

图 6-66. Large-Signal Step Response

6.8 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75V, V– = –2.75V, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

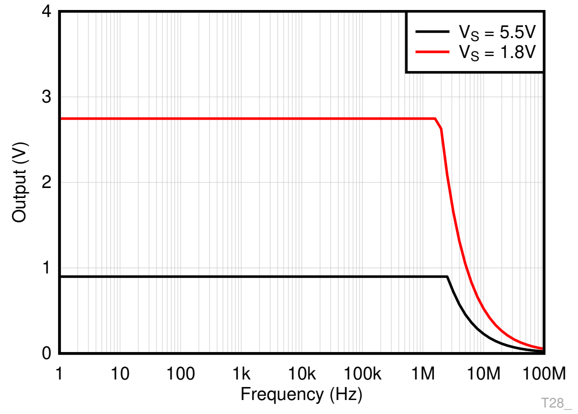
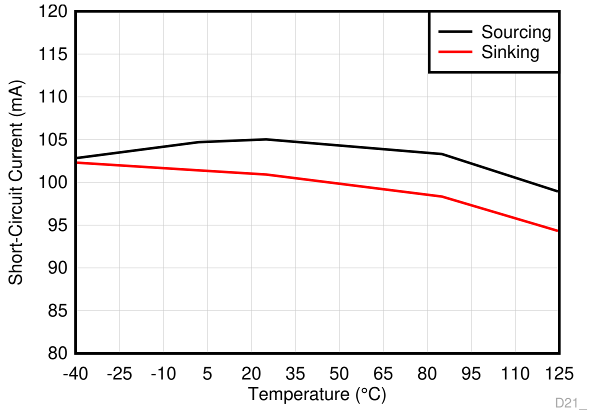
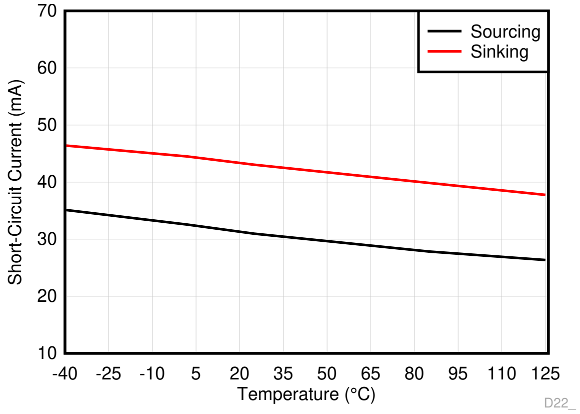


图 6-67. Maximum Output Voltage vs Frequency



V_S = 5.5V

图 6-68. Short-Circuit Current vs Temperature



V_S = 1.8V

图 6-69. Short-Circuit Current vs Temperature

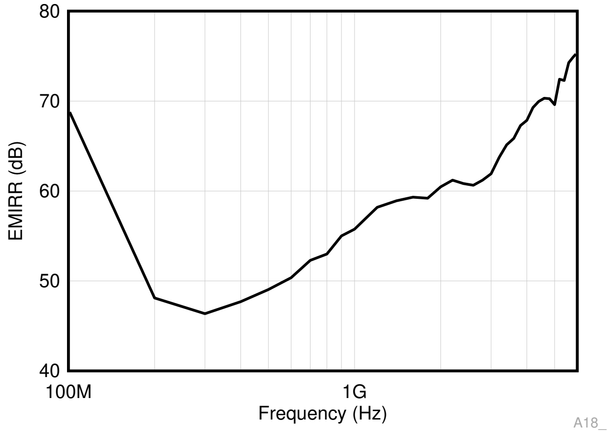


图 6-70. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR+) vs Frequency

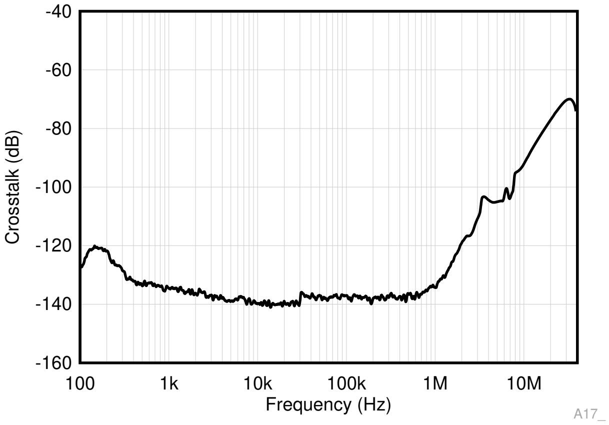


图 6-71. Channel Separation

7 Detailed Description

7.1 Overview

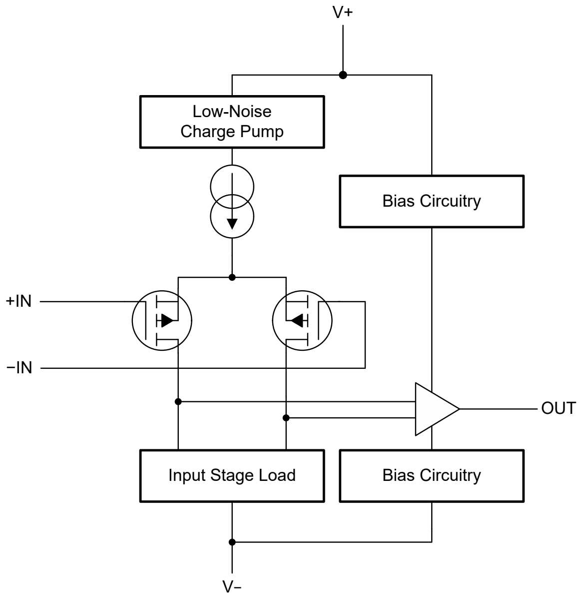
The OPAx323 family of op amps includes single / dual / quad channel (OPA323, OPA2323, OPA4323), ultra low-voltage (1.7V to 5.5V), high-bandwidth (20MHz) amplifiers. This family of amplifiers feature a zero-crossover input stage and a rail-to-rail output stage that can be used for variety of applications across industrial and automotive markets. The input common-mode voltage range includes signal swing beyond the supply rails, and allows the OPAx323 to be used in many single-supply or dual supply configurations. Rail-to-rail output swing significantly increases dynamic range, especially in low-supply applications with the class AB output stage capable of driving smaller resistive loads.

The OPAx323 family of zero-cross input stage amplifiers achieve high linearity for input signals with rail-to-rail swing that are typical in ADC driver applications in comparison to the complementary input stage amplifiers. Gain-bandwidth of 20MHz helps provide a fast settling response for ADC sampling speeds between 0.5 to 5MSPS depending on the settling performance required. The OPAx323 easily supports precision performance in high gain voltage sensing applications (such as the wheatsone bridge), as the device features maximum offset of 1.25mV and drift of 1.8 μ V/°C. This unique combination of high precision and high gain-bandwidth enables use in multiple applications such as the motor rotary encoders, microphone audio pre-amplifiers and ultrasonic transducers.

The OPAx323 family consumes only 1.6mA supply current per channel for 20MHz gain bandwidth, thus providing a good AC performance at a very low power consumption. These devices achieve a high slew-rate of 33V/ μ s allowing for fast detection of faults in motor current sensing applications. The zero-cross over input stage provides identical AC and DC performance for both low and high-side sensing applications, thus making the OPAx323 the best choice for current sensing in a variety of end equipments such as the solar string inverters, power delivery, grid, and EV infrastructure. Precision transimpedance and voltage gain applications are well served with a low input bias current (0.5pA typical, 20pA maximum), a good PSRR (20 μ V/V maximum), CMRR (100dB minimum), and A_{OL} (114dB minimum). The device has 60° of typical phase margin with no load and drives up to 75pF with a phase margin of 35°.

The OPAx323 has an internal current limit that enables additional robustness when operating with high output current while driving smaller output impedance like 68 Ω , 128 Ω , and 256 Ω loads in audio applications. The OPAx323 can swing very close to the rails and has a short circuit current of ±80mA minimum at 5.5V power supply. The OPAx323S devices provide shutdown functionality for additional power savings and help disable the amplifier when idle. These op amps feature an integrated radio frequency immunity (RFI) and electro-magnetic interference (EMI) rejection filter, unity-gain stability, and no-phase reversal in input overdrive conditions.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Voltage

The OPAx323 series of operational amplifiers is fully specified from 1.8V to 5.5V and is designed for amplifier operation from 1.7V to 1.8V. In addition, many specifications apply from –40°C to 125°C. Parameters that vary significantly with operating voltages or temperature are provided in the *Typical Characteristics* section. TI highly recommends to add low-ESR ceramic bypass capacitors (C_{BYP}) between each supply pin and ground. Only one C_{BYP} is sufficient for single supply operation. Make sure that C_{BYP} is placed as close to the device as possible and the power supply trace routes through C_{BYP} before reaching the amplifier power supply terminals.

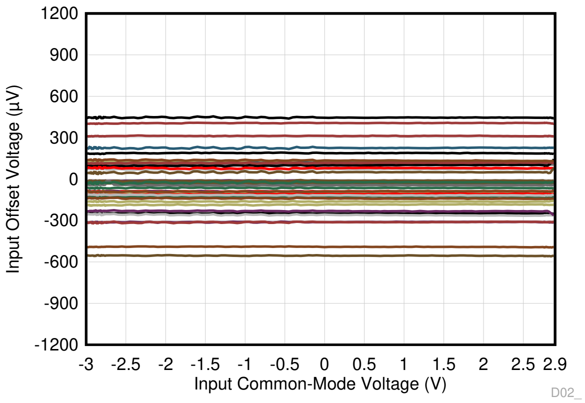
7.3.2 Rail-to-Rail Input

The input common-mode voltage range of the OPAx323 series extends beyond the supply rails with a common-mode rejection ratio (CMRR) of 100dB minimum at 5.5V as specified in *Electrical Characteristics*. The device is designed to have a good performance of 85dB minimum CMRR even when operating at an ultra-low supply voltage of 1.8V. This is made possible by using a zero-cross input stage architecture for the amplifier input pair.

Most commercial amplifiers employ a complementary input stage architecture which often limits the rail-to-rail CMRR to less than 65dB. This is because the offset performance across the rail-to-rail input common-mode range is not linear. One of the input pairs, usually, the P-channel pair with better offset, noise performance is designed to cover the majority of the common-mode range with the N-channel pair slated to slowly take over at a certain threshold voltage from the positive rail. The creates a big jump in the offset voltage across common mode when transitioning across the input pairs as shown in TLV900x Offset Voltage vs Common-Mode. This offset jump not only affects CMRR but also limits linearity / THD for rail-to-rail input signals.

The OPAx323 achieves linear offset performance over the entire rail-to-rail input range by extending the common-mode-range of a single P-channel input pair using an internal charge pump as shown in the *Functional Block Diagram*. This eliminates the need for the N-channel input pair and the resulting offset jump caused by input pair transitions.

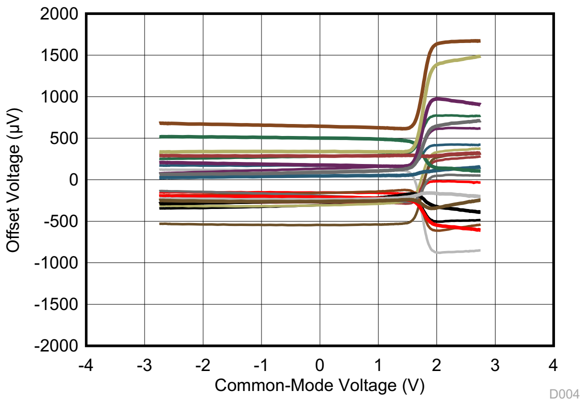
The OPAx323 exhibits near to zero shift in offset voltage across the entire common-mode voltage as shown in 图 7-1. This is crucial to achieving high linearity in ADC driver and audio driver applications.



V+ = 2.75V, V– = –2.75V No. of devices = 45

(V–) – 0.25V < V_{CM} < (V+) + 0.15V

图 7-1. OPAx323 Offset Voltage vs Common-Mode



V+ = 2.75V, V– = –2.75V

图 7-2. TLV900x Offset Voltage vs Common-Mode

7.3.3 Rail-to-Rail Output

The OPAx323 delivers a robust output drive capability. An output stage with common-source transistors is used to achieve full rail-to-rail output swing capability. The device is designed to have a minimum output short circuit current of ±80mA, making the device an excellent choice for audio driver applications at room temperature and at 5.5V. For resistive loads up to 2kΩ and a power supply of 5.5V, the output swings within a maximum of 55mV to either supply rail, thereby using almost the entire input range of an ADC in ADC driver applications.

7.3.4 Common-Mode Rejection Ratio (CMRR)

The OPAx323 achieves excellent DC and AC CMRR performance. The device is designed to have a DC CMRR performance at two supply voltages (5.5V and 1.8V) for the entire operating temperature range (–40°C to 125°C). DC CMRR is specified for common-mode beyond rails over a input voltage range of $(V–) – 0.2V \leqslant V_{CM} \leqslant (V+) + 0.15V$ for 5.5V operation and $(V–) – 0.1V \leqslant V_{CM} \leqslant (V+) + 0.05V$ for 1.8V operation. AC CMRR is shown in *Typical Characteristics* and is subject to the routing of input traces on the PCB board. For good performance, maintain a short and symmetrical input trace for the two amplifier input terminals.

7.3.5 Capacitive Load and Stability

The OPAx323 is designed for use in applications where driving a capacitive load is required. As with all operational amplifiers, there can be specific instances where the device can become unstable. The particular operational amplifier circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether or not an amplifier is stable in operation.

An operational amplifier in the unity-gain (1V/V) buffer configuration that drives a capacitive load exhibits a greater tendency to be unstable than an amplifier operating at a higher noise gain. The capacitive load, in conjunction with the operational amplifier output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases when capacitive loading increases. When operating in the unity-gain configuration, the OPAx323 has a phase margin of 50° with 30pF of capacitive load. The device remains stable with pure capacitive loads up to approximately 75pF with acceptable phase margin of 35° and has no sustained oscillations up to 150pF. The equivalent series resistance (ESR) of some very large capacitors (greater than 1μF) is sometimes sufficient to alter the phase characteristics in the feedback loop such that the amplifier remains stable. Increasing the amplifier closed-loop gain allows the amplifier to drive increasingly larger capacitance. This increased capability is evident when measuring the overshoot response of the amplifier at higher voltage gains.

One technique for increasing the capacitive load drive capability of the amplifier operating in a unity-gain configuration is to insert a small resistor (typically 10Ω to 50Ω) in series with the output, as shown in 图 7-3. This resistor significantly reduces the overshoot and ringing associated with large capacitive loads. This is usually the circuit configuration used in ADC driver application with C_{load} serving as a charge bucket for the ADC sampling capacitor.

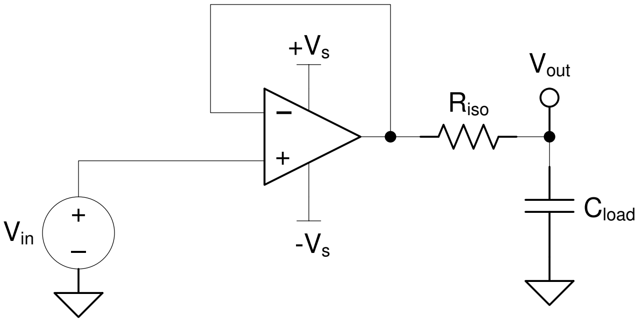


图 7-3. Improving Capacitive Load Drive

7.3.6 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output stage of the operational amplifier enters a saturation region when the output voltage exceeds the rated operating voltage, because of the high input voltage or high gain. After one of the outputs enters the saturation region, the output stage requires additional time to return to the linear operating state which is referred to as overload recovery time. After the output stage returns to linear operating state, the amplifier begins to slew at the specified slew rate. Therefore, the propagation delay (in case of an overload condition) is the sum of the overload recovery time and the slew time.

The overload recovery time for the OPAx323 family is designed to be approximately 130ns typical.

7.3.7 EMI Rejection

The OPAx323 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications (radio frequency interference - RFI) and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPAx323 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10MHz to 6GHz. 图 7-4 shows the results of this testing on the OPAx323. 表 7-1 shows the EMIRR IN+ values for the OPAx323 at particular frequencies commonly encountered in real-world applications. The *EMI Rejection Ratio of Operational Amplifiers* application report contains detailed information on the topic of EMIRR performance relating to op amps and is available for download from www.ti.com.

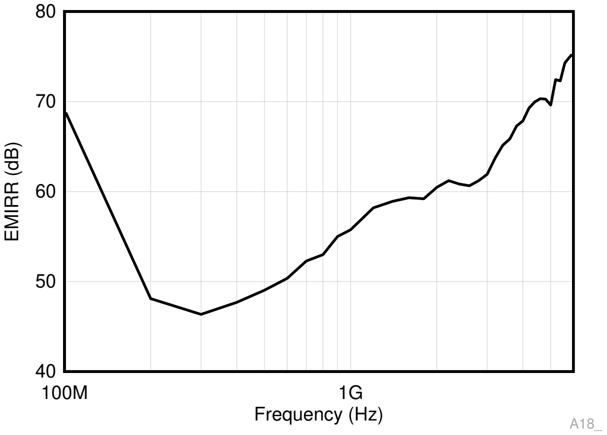


图 7-4. EMIRR Testing

表 7-1. OPAx323 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	48dB
900MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6GHz), GSM, aeronautical mobile, UHF applications	56dB
1.8GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1GHz to 2GHz)	60dB
2.4GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2GHz to 4GHz)	61dB
3.6GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	67dB
5GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4GHz to 8GHz)	70dB

7.3.8 ESD and Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and relevance to an electrical overstress event is helpful. 图 7-5 shows the ESD circuits contained in the OPAx323 devices. The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power supply lines, where the input and output pins meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

Note that the OPAx323 features no current-steering diodes connected between the input and positive power-supply pin.

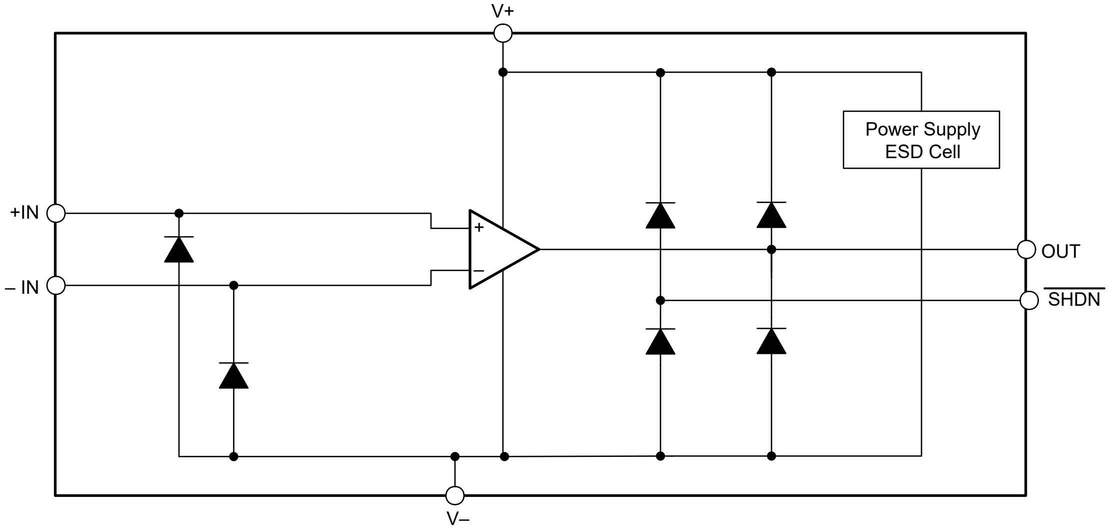


图 7-5. Equivalent Internal ESD Circuitry

7.3.9 Input ESD Protection

The OPAx323 family incorporates internal ESD protection circuits on all pins. For inputs, this protection primarily consists of fail safe ESD input structures which feature no current-steering diodes connected between the input and positive power-supply pin as shown in the 图 7-5. This feature is very useful during power sequencing scenarios where input signal can be present before the positive power supply rail. A fail safe input ESD structure prevents any short between inputs and positive power supply. For further details, refer to *Op Amp ESD Protection Structures* application note.

7.3.10 Shutdown Function

The OPAx323S devices feature $\overline{\text{SHDN}}$ pins that disable the op amp, placing the op amp into a low-power standby mode. In this mode, the op amp typically consumes less than 1000nA at room temperature. The $\overline{\text{SHDN}}$ pins are active low, meaning that shutdown mode is enabled when the input to the $\overline{\text{SHDN}}$ pin is a valid logic low.

The $\overline{\text{SHDN}}$ pins are referenced to the negative supply voltage of the op amp. The threshold of the shutdown feature lies around 500mV (typical) and does not change with respect to the supply voltage. Hysteresis has been included in the switching threshold to provide for smooth switching characteristics. For optimal shutdown behavior, the $\overline{\text{SHDN}}$ pins must be driven with valid logic signals. A valid logic low is defined as a voltage between V– and (V–) + 0.2V. A valid logic high is defined as a voltage between (V–) + 1V and V+. To enable the amplifier, the $\overline{\text{SHDN}}$ pins must be driven to a valid logic high. To disable the amplifier, the $\overline{\text{SHDN}}$ pins must be driven to a valid logic low. TI highly recommends to not leave the shutdown pin floating, but to connect the shutdown pin to a valid high or low voltage. The maximum voltage allowed at the $\overline{\text{SHDN}}$ pins is (V+) + 0.5V. Exceeding this voltage level damages the device.

The $\overline{\text{SHDN}}$ pins are high-impedance CMOS inputs. Dual op amp versions are independently controlled and quad op amp versions are controlled in pairs with logic inputs. For battery-operated applications, this feature can be used to greatly reduce the average current and extend battery life. The enable and disable time is targeted to be under 1µs for full shutdown of all channels. When disabled, the output assumes a high-impedance state. This architecture allows the OPAx323S to operate as a gated amplifier (or to have the device output multiplexed onto a common analog output bus). Shutdown time (t_{OFF}) depends on loading conditions as any charge on the output capacitor needs to be discharged by any external resistive load or the op-amp. To achieve the 1µs shutdown time, the specified 10kΩ load to midsupply (V_S / 2) is required with no capacitive load.

7.3.11 Packages with an Exposed Thermal Pad

The OPAx323 family is available in packages such as the WQFN-16 (RTE) and WSON-8 (DSG), which feature an exposed thermal pad. Inside the package, the die is attached to this thermal pad using an electrically conductive compound. For this reason, when using a package with an exposed thermal pad, the thermal pad must be connected to V–. Attaching the thermal pad to a potential other then V– is not allowed, and the performance of the device may not be consistent with the *Electrical Characteristics* table when doing so.

7.4 Device Functional Modes

The OPAx323 devices have one functional mode. These devices are powered on as long as the power-supply voltage is between 1.7V (±0.85V) and 5.5V (±2.75V).

The OPAx323S devices feature a shutdown pin, which can be used to place the op amp into a low-power mode. For more information, see the *Shutdown Function* section.

8 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The OPAx323 family of rail-to-rail input and output operational amplifiers is specifically designed for variety of high gain and high speed applications. These devices operate from 1.7V to 5.5V, are unity-gain stable, and are also an excellent choice for a wide range of general-purpose applications. The output stage is capable of driving small resistive loads connected to any point between V+ and V– as long as the device is not forced into short circuit mode. The input common-mode voltage range includes beyond the rail signal swing and allows the OPAx323 series to be used in many single-supply or dual supply configurations.

8.2 Typical Application

8.2.1 OPAx323 in Low-Side, Current Sensing Application

图 8-1 shows the OPA323 configured in a low-side current sensing application.

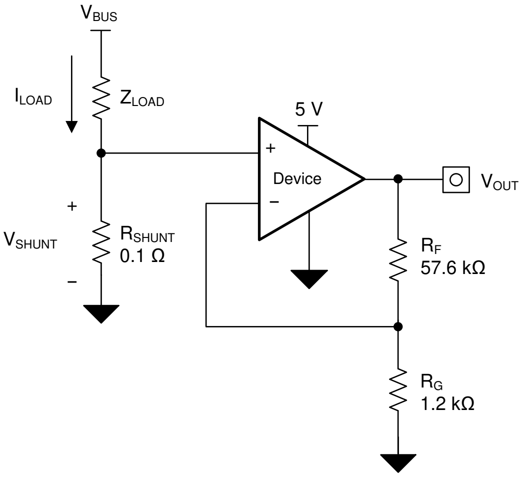


图 8-1. OPA323 in a Low-Side, Current-Sensing Application

8.2.1.1 Design Requirements

The design requirements for this design are:

- Load current: 0A to 1A
- Maximum output voltage: 4.9V
- Maximum shunt voltage: 100mV

8.2.1.2 Detailed Design Procedure

The transfer function of the circuit in 图 8-1 is given in 方程式 1.

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times \text{Gain} \tag{1}$$

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0A to 1A. To keep the shunt voltage below 100 mV at maximum load current, the largest shunt resistor is defined using 方程式 2.

$$R_{SHUNT} = \frac{V_{SHUNT\_MAX}}{I_{LOAD\_MAX}} = \frac{100\ \text{mV}}{1\ \text{A}} = 100\ \text{m}\Omega \tag{2}$$

Using 方程式 2, R_{SHUNT} is calculated to be 100mΩ. The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the OPA323 to produce an output voltage of approximately 0V to 4.9V. The gain needed by the OPA323 to produce the necessary output voltage is calculated using 方程式 3.

$$\text{Gain} = \frac{V_{OUT\_MAX} - V_{OUT\_MIN}}{V_{IN\_MAX} - V_{IN\_MIN}} \tag{3}$$

Using 方程式 3, the required gain is calculated to be 49V/V, which is set with resistors R_F and R_G. 方程式 4 sizes the resistors R_F and R_G, to set the gain of the OPA323 to 49V/V.

$$\text{Gain} = 1 + \frac{R_F}{R_G} \tag{4}$$

Selecting R_F as 57.6kΩ and R_G as 1.2kΩ provides a combination that equals 49V/V. 图 8-2 shows the measured transfer function of the circuit shown in 图 8-1. Notice that the gain is only a function of the feedback and gain resistors. This gain is adjusted by varying the ratio of the resistors and the actual resistors values are determined by the impedance levels that the designer wants to establish. The impedance level determines the current drain, the effect that stray capacitance has, and a few other behaviors. There is no optimal impedance selection that works for every system; choose an impedance that is best for the system parameters.

8.2.1.3 Application Curve

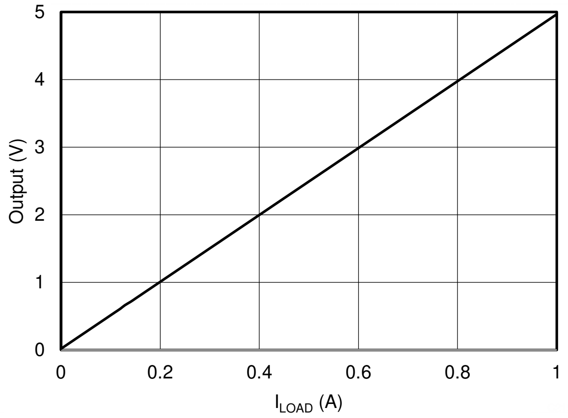


图 8-2. Low-Side, Current-Sense Transfer Function

8.3 Power Supply Recommendations

The OPAx323 is tested for amplifier operation at 1.7V and is fully specified from 1.8V to 5.5V (±0.9V to ±2.75V); many specifications apply from –40°C to 125°C. *Electrical Characteristics* presents parameters that can exhibit significant variance regarding operating voltage or temperature.

> 小心
>
> Supply voltages larger than 7V can permanently damage the device; for more information, see the *Absolute Maximum Ratings* table.

TI highly recommends to add low-ESR ceramic bypass capacitors (C_{BYP}) between each supply pin and ground. Only one C_{BYP} is sufficient for single supply operation. Place the C_{BYP} as close to the device as possible to reduce coupling errors from noisy or high-impedance power supplies. Make sure the power supply trace routes through C_{BYP} before reaching the amplifier power supply terminals. For more information, see *Layout Guidelines*.

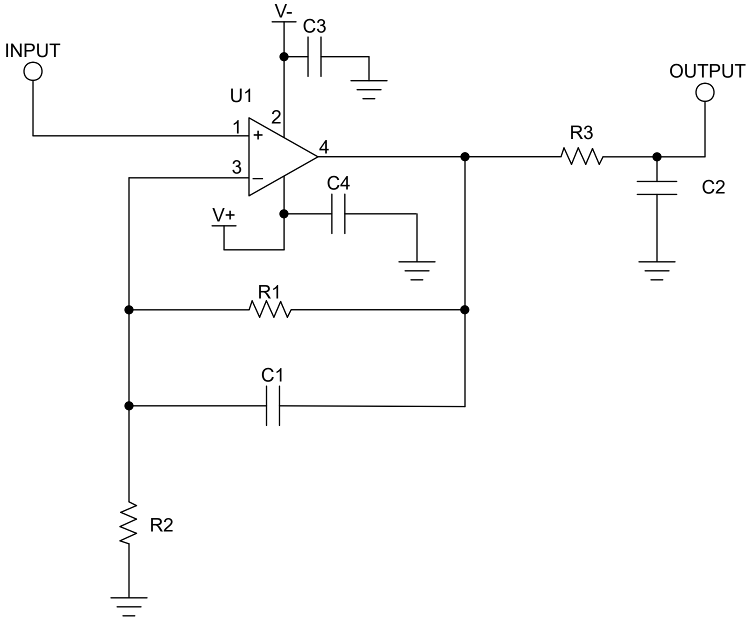
8.4 Layout

8.4.1 Layout Guidelines

For best operational performance, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power connections of the board and propagate to the power pins of the op amp itself. Bypass capacitors are used to reduce the coupled noise by providing a low-impedance path to ground.
  - Connect low-ESR, 0.1μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. One bypass capacitor from V+ to ground is adequate for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, then cross the sensitive trace at a 90 degree angle, which is much better as opposed to running the traces in parallel with the noisy trace.
- Place the external components as close to the device as possible, as shown in *Layout Example*. Keeping R_1 and R_2 close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- TI recommends cleaning the PCB following board assembly for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, TI recommends baking the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

8.4.2 Layout Example



Note: C3 and C4 are C_{BYP} capacitors

图 8-3. Schematic for Noninverting Configuration Layout Example

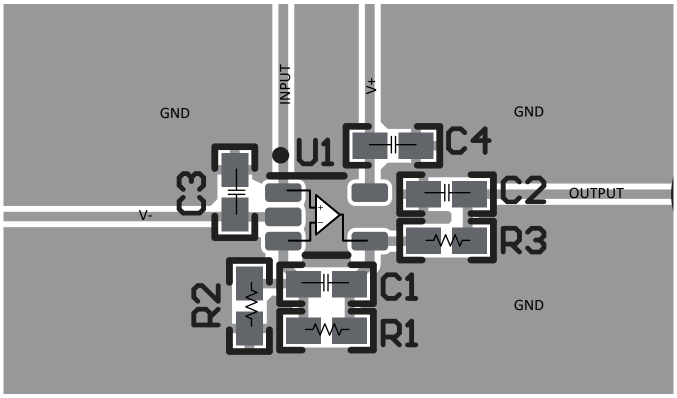


图 8-4. Operational Amplifier Board Layout for Noninverting Configuration - SC70 (DCK) Package

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *QFN/SON PCB Attachment* application note
- Texas Instruments, *Quad Flatpack No-Lead Logic Packages* application note

9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

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Bluetooth® is a registered trademark of Bluetooth SIG, Inc.
所有商标均为其各自所有者的财产。

9.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.5 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (November 2023) to Revision B (April 2024)	Page
将 DGK (VSSOP, 8)、DDF (SOT23-THN) OPA2323 和 DYY (SOT23-THN) OPA4323 的状态从*预发布* 更改为*正在供货*	1
将数据表标题中的 CMRR 值从 m *100dB* 更改为 *114dB*	1
在*器件信息* 表中将 DYY (SOT-23) 封装选项从 *16* 引脚更改为 *14* 引脚，并将封装从 OPA4323S 移至 OPA4323	1
Changed the DYY (SOT-23) package option from *16* to *14* pins and moved the package from OPA4323S to OPA4323 in *Device Comparison* table	2
Removed OPA4310 information from the data sheet	11
Changed the *Typical Characteristics* section to add more plots	14
Changed the *Rail-to-Rail input* section	28
Changed the EMIRR Testing plot in *EMI Rejection* section	30
Changed the EMIRR IN+ values for the 900MHz, 1.8GHz, 2.4GHz, 3.6GHz, and 5GHz frequency options in *OPAx323 EMIRR IN+ for Frequencies of Interest* table	30

Changes from Revision * (October 2023) to Revision A (November 2023) **Page**

- 将 DCK (SC70, 5) OPA323 状态从*预发布*更改为*正在供货* 1
- 将 D (SOIC, 8) OPA2323 状态从*预发布*更改为*正在供货* 1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2323IDDFR	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	23DDF
OPA2323IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2DGK
OPA2323IDR	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2323ID
OPA323IDCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1RG
OPA4323IDYYR	Active	Production	SOT-23-THIN (DYY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	125 to -40	O4323IDYYR
OPA4323IPWR	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	125 to -40	O4323PW

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

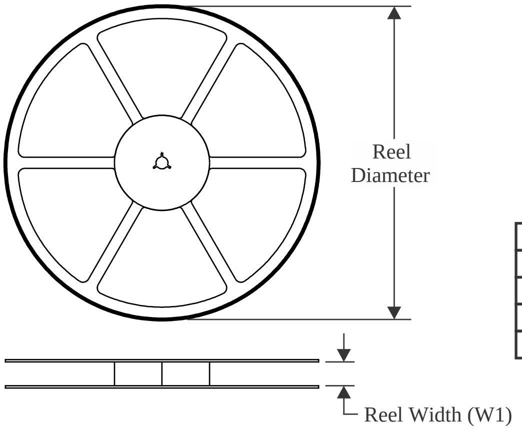
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

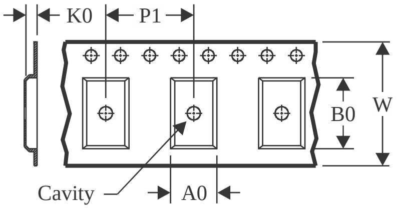
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

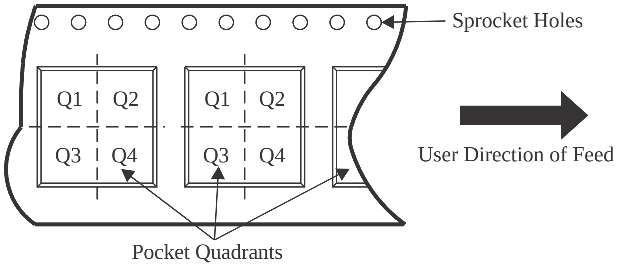


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

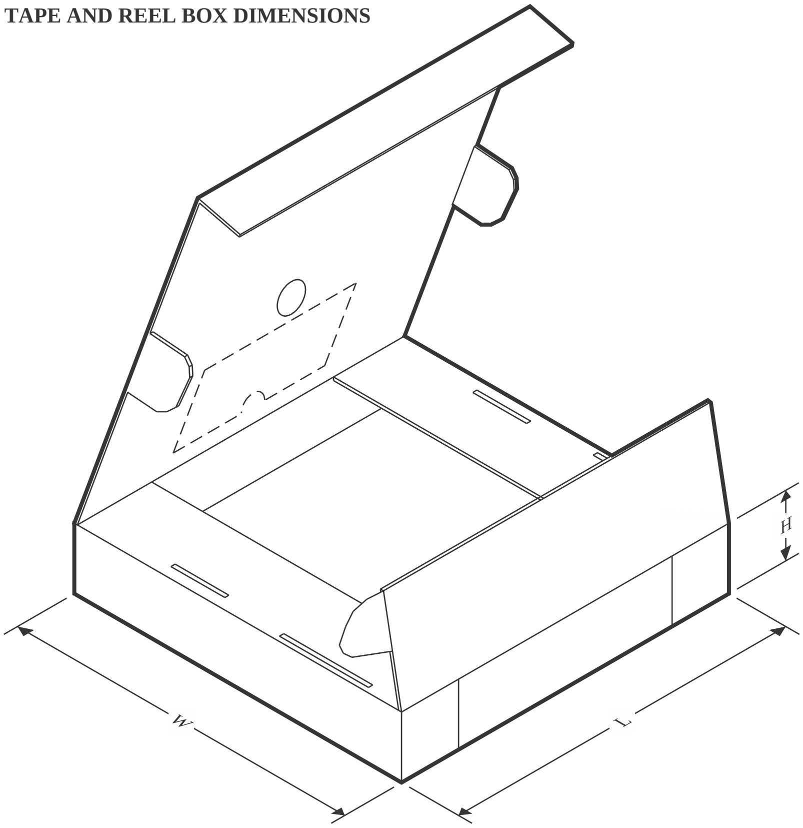
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

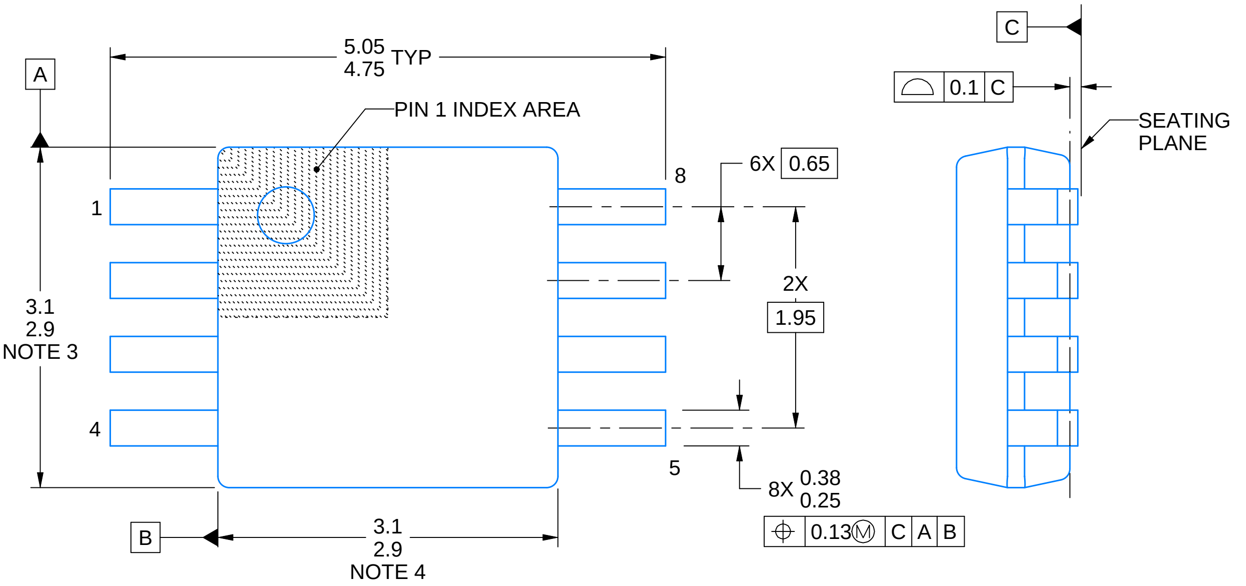
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2323IDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA2323IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2323IDR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA323IDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
OPA4323IDYYR	SOT-23-THIN	DYY	14	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
OPA4323IPWR	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

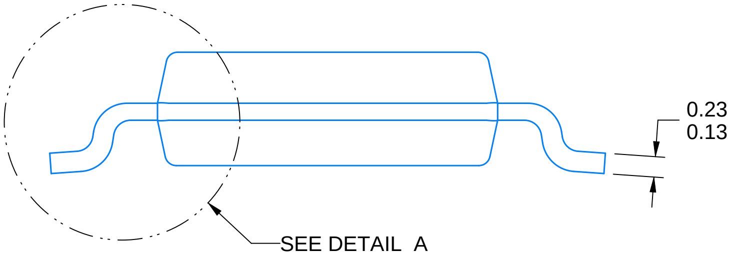
TAPE AND REEL BOX DIMENSIONS

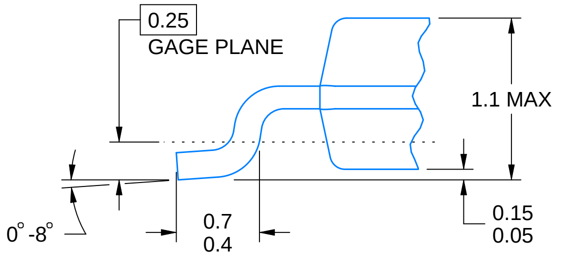


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2323IDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
OPA2323IDGKR	VSSOP	DGK	8	2500	356.0	356.0	35.0
OPA2323IDR	SOIC	D	8	3000	356.0	356.0	35.0
OPA323IDCKR	SC70	DCK	5	3000	190.0	190.0	30.0
OPA4323IDYYR	SOT-23-THIN	DYY	14	3000	336.6	336.6	31.8
OPA4323IPWR	TSSOP	PW	14	3000	356.0	356.0	35.0







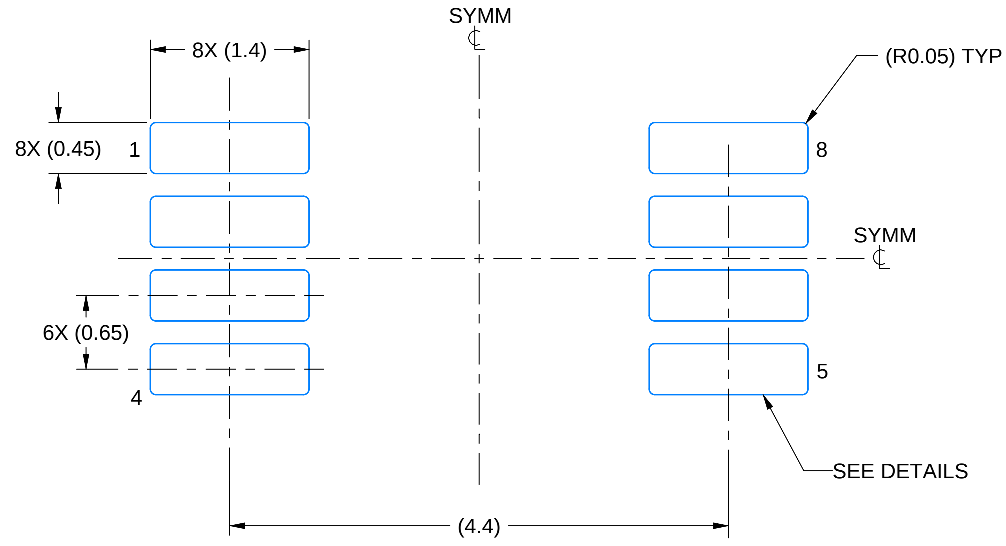
DETAIL A
TYPICAL

4214862/A 04/2023

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

NON-SOLDER MASK
DEFINED
(PREFERRED)

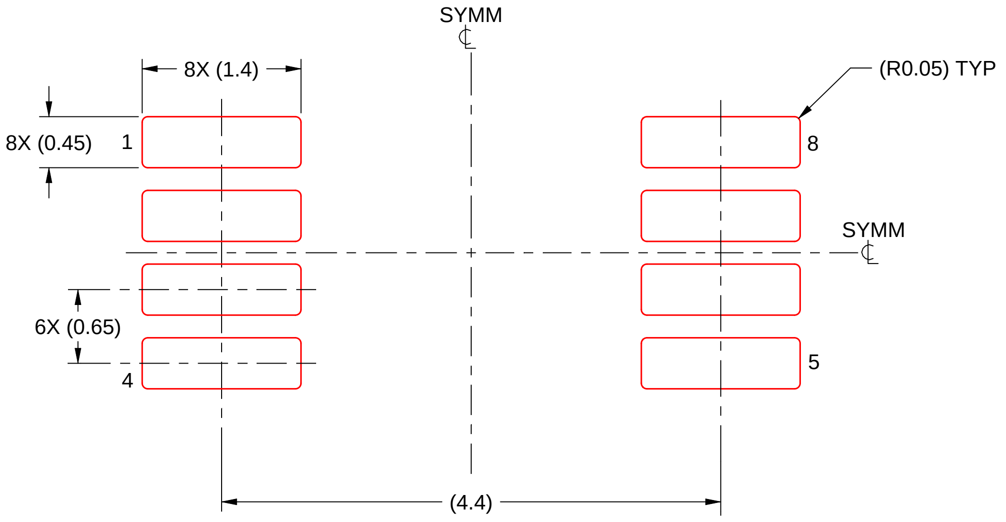
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

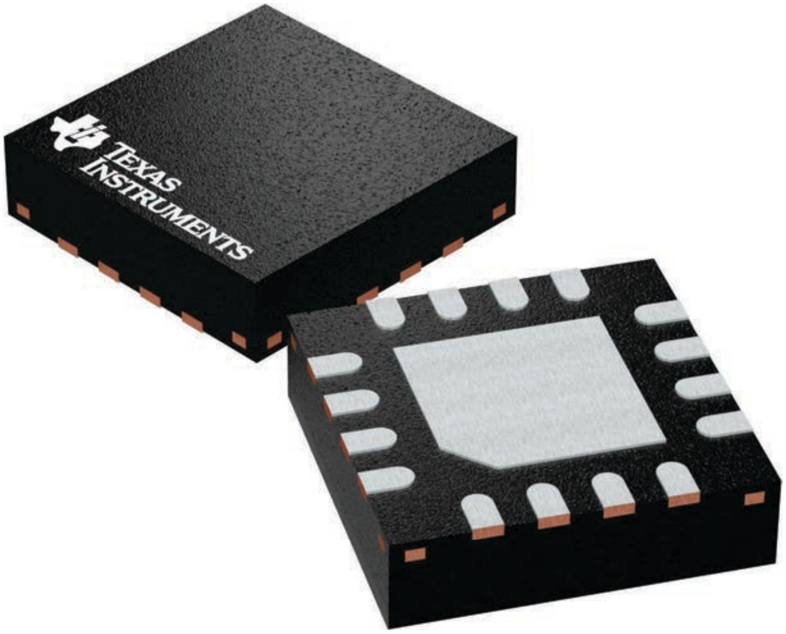
RTE 16

WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

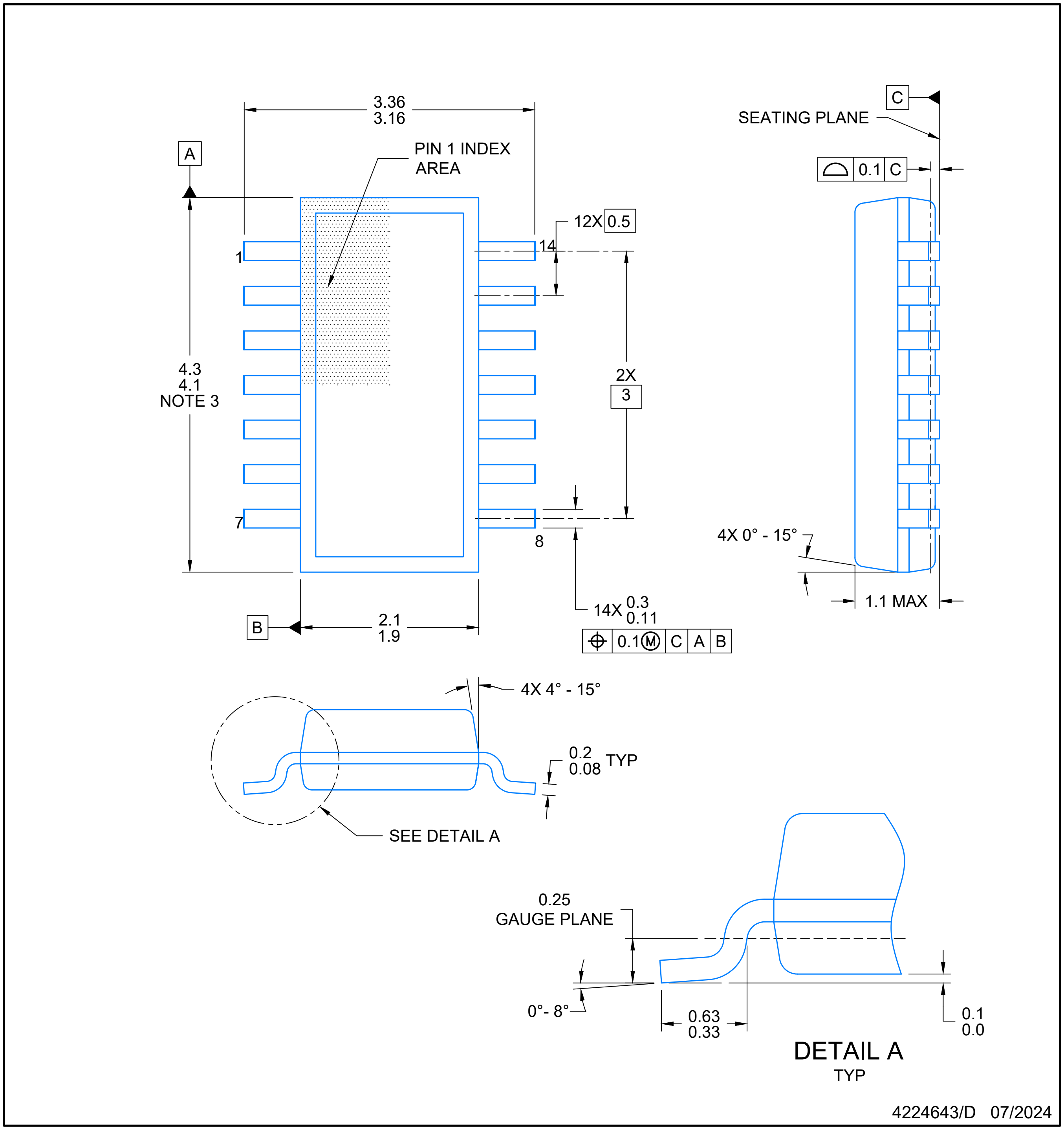


PACKAGE OUTLINE

DYY0014A

SOT-23-THIN - 1.1 mm max height

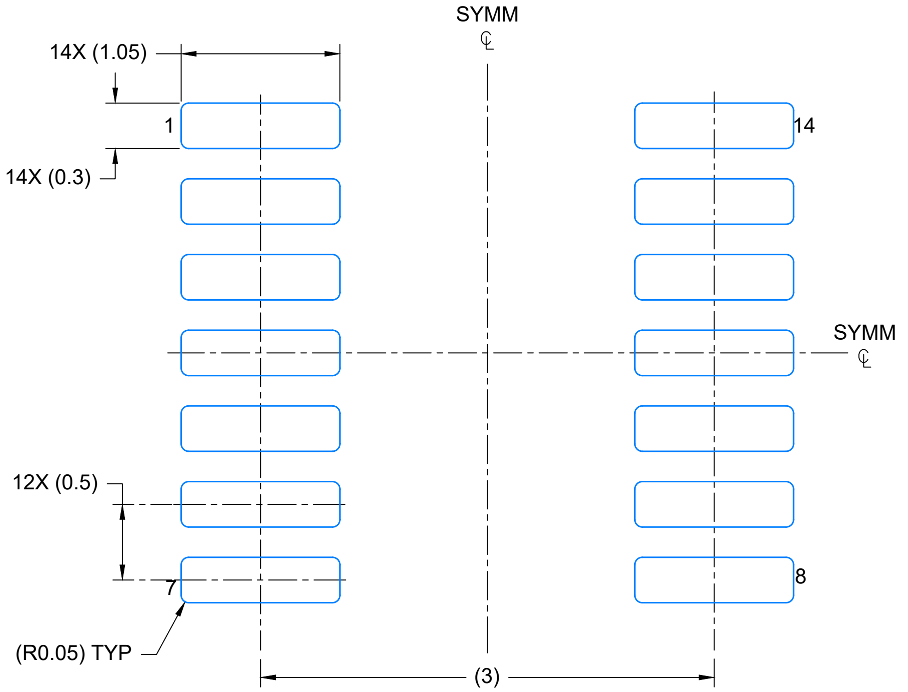
PLASTIC SMALL OUTLINE



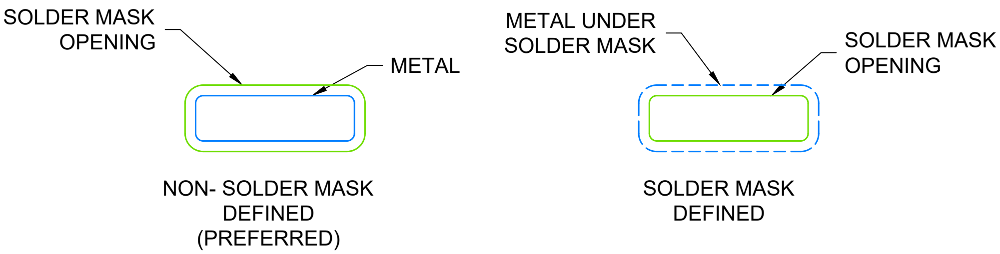
4224643/D 07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4224643/D 07/2024

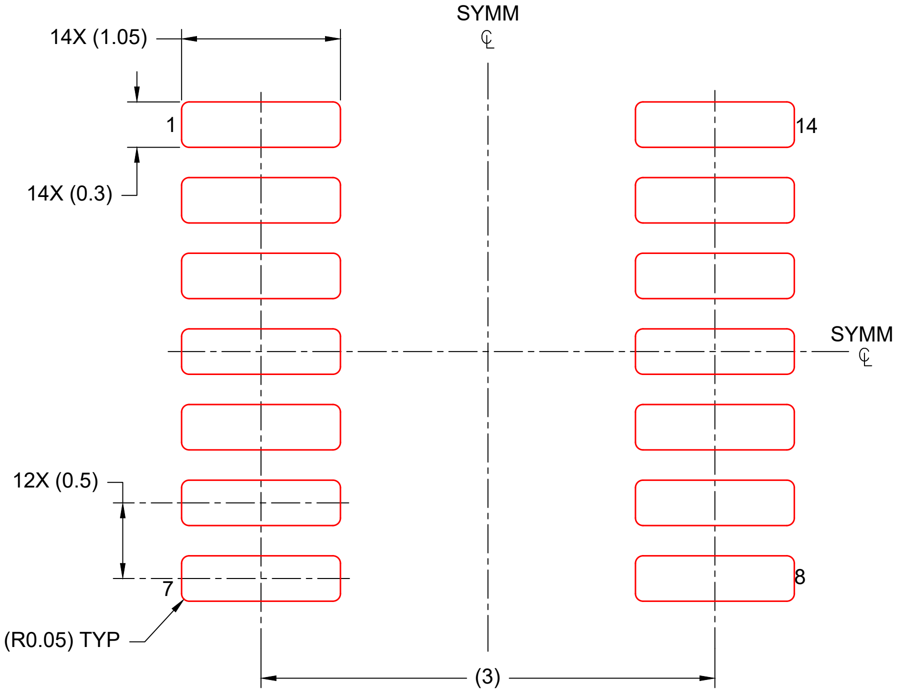
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

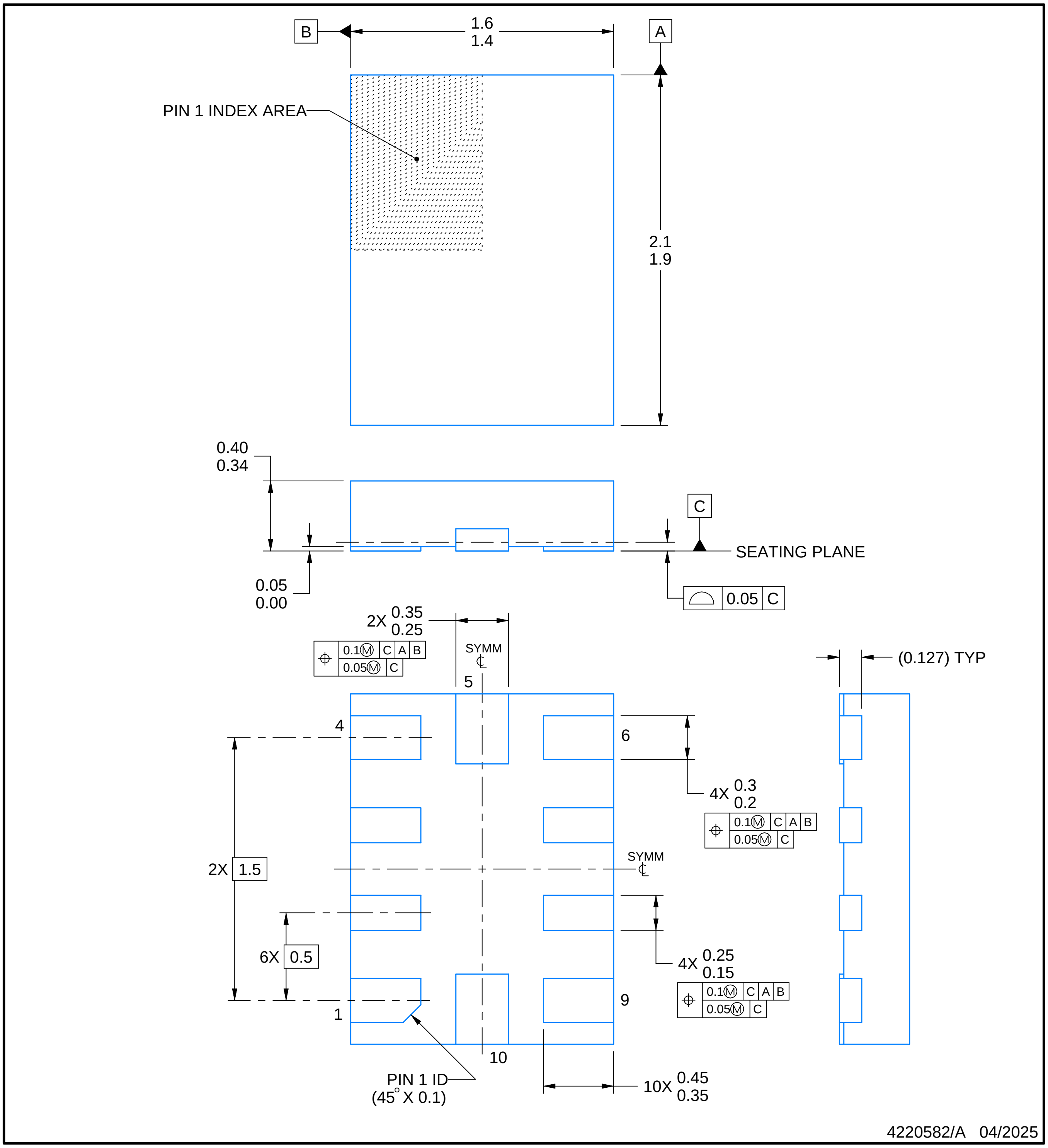


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224643/D 07/2024

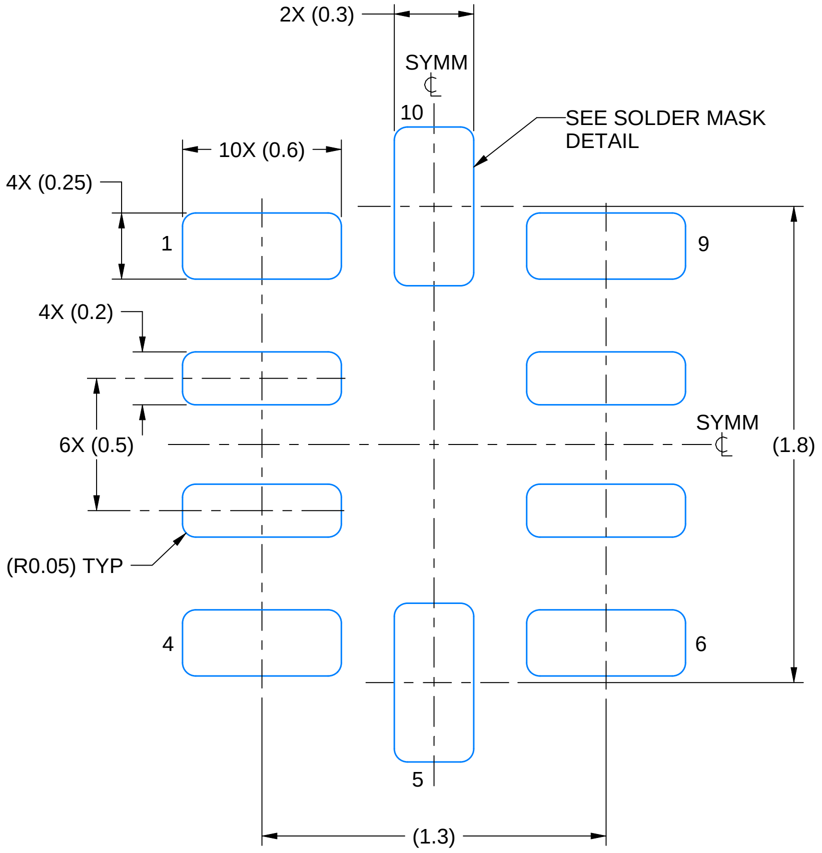
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

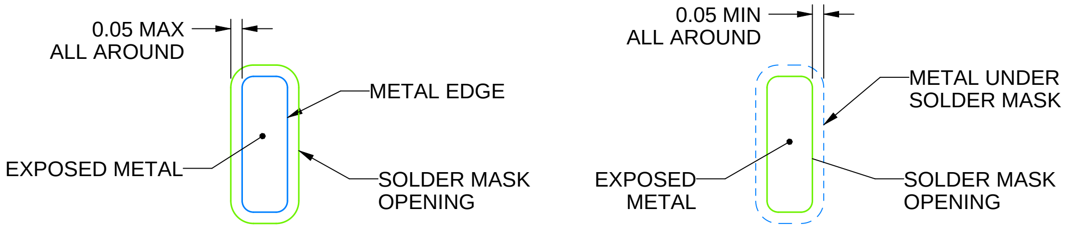


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 35X



NON SOLDER MASK DEFINED
(PREFERRED)

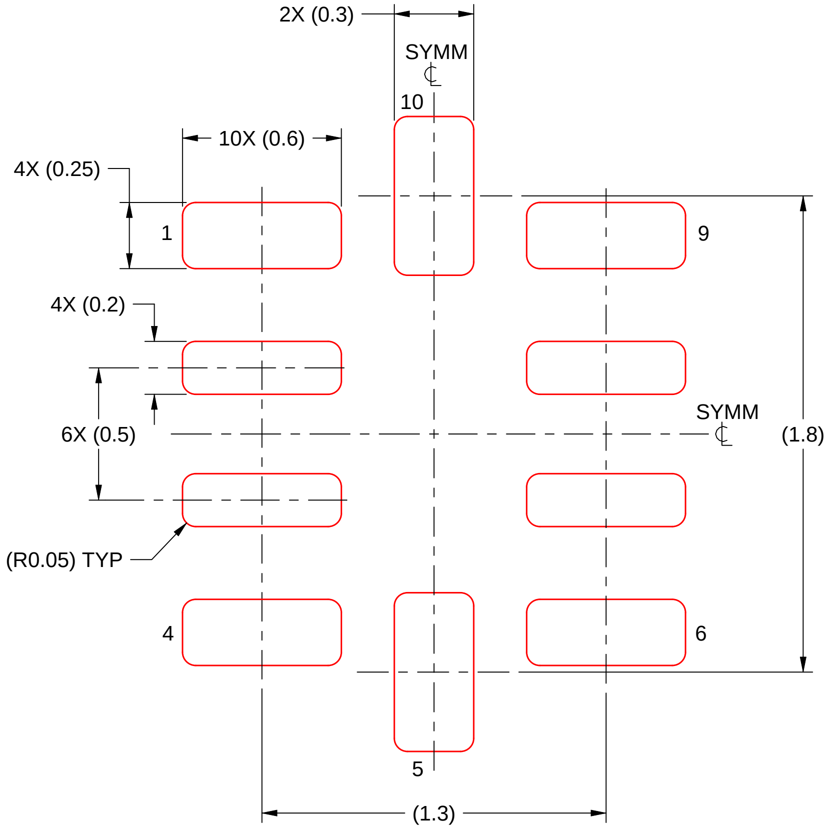
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220582/A 04/2025

NOTES: (continued)

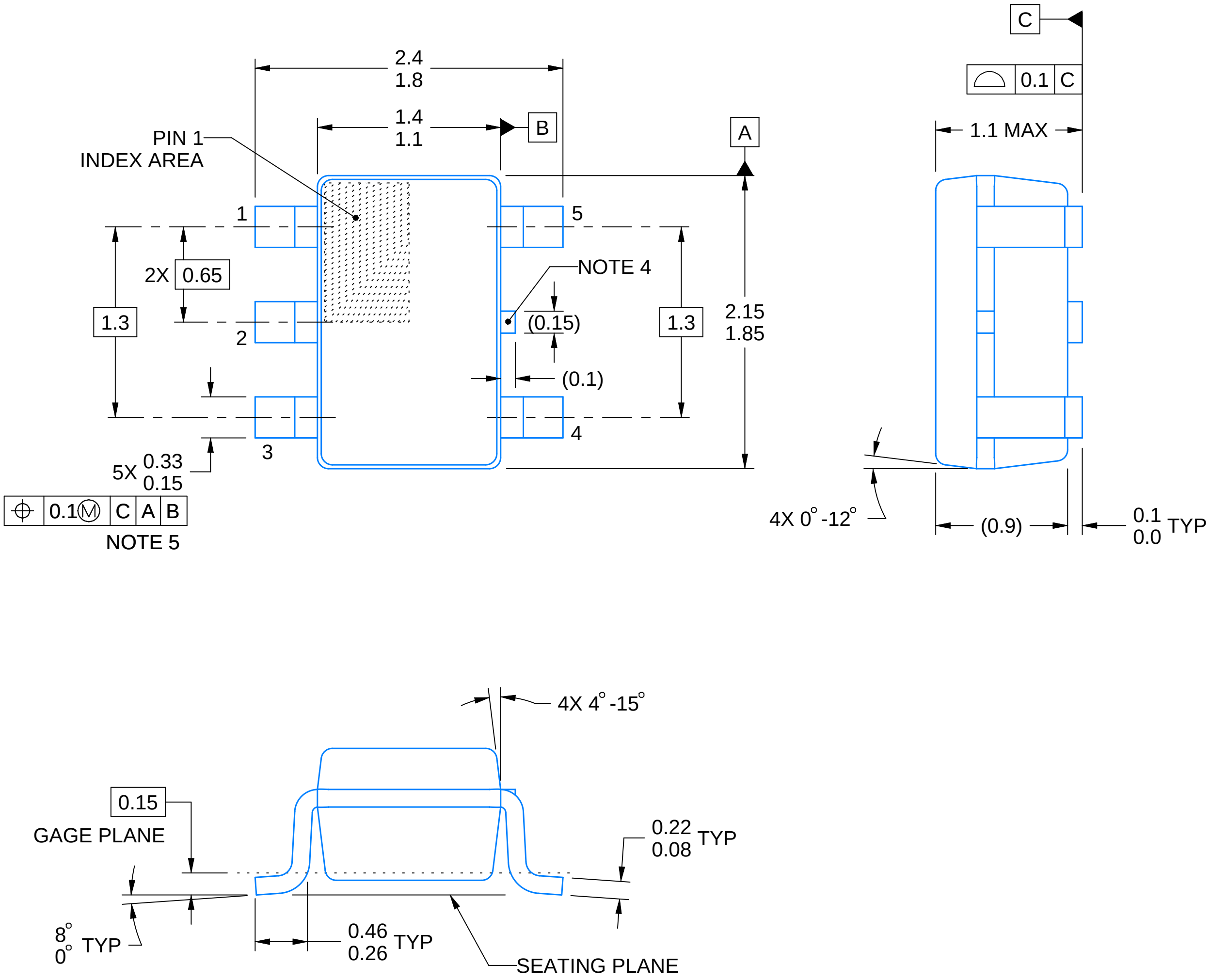
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 35X

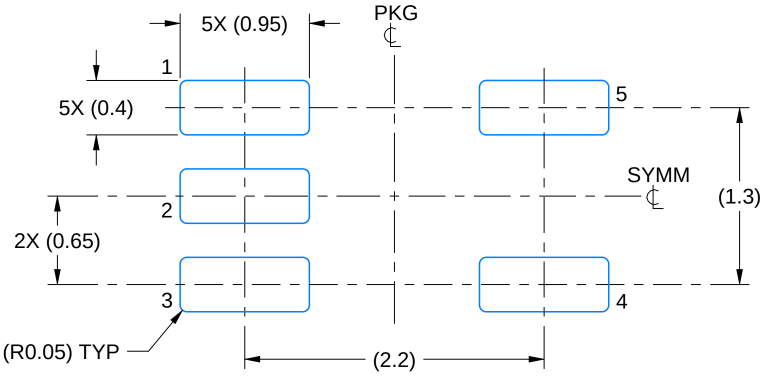
NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

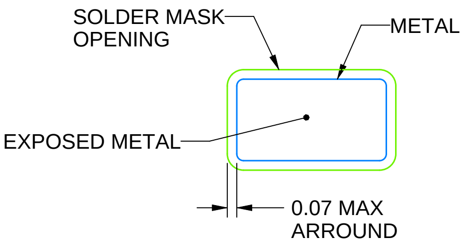


NOTES:

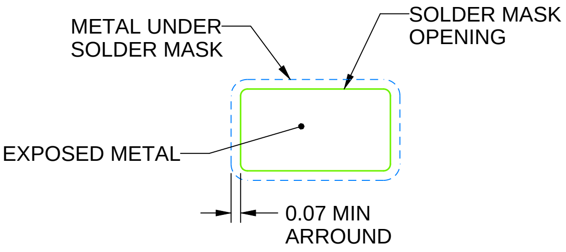
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



NON SOLDER MASK
DEFINED
(PREFERRED)

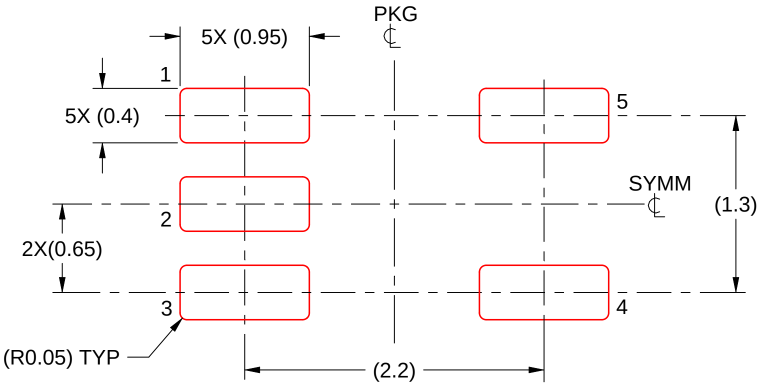


SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

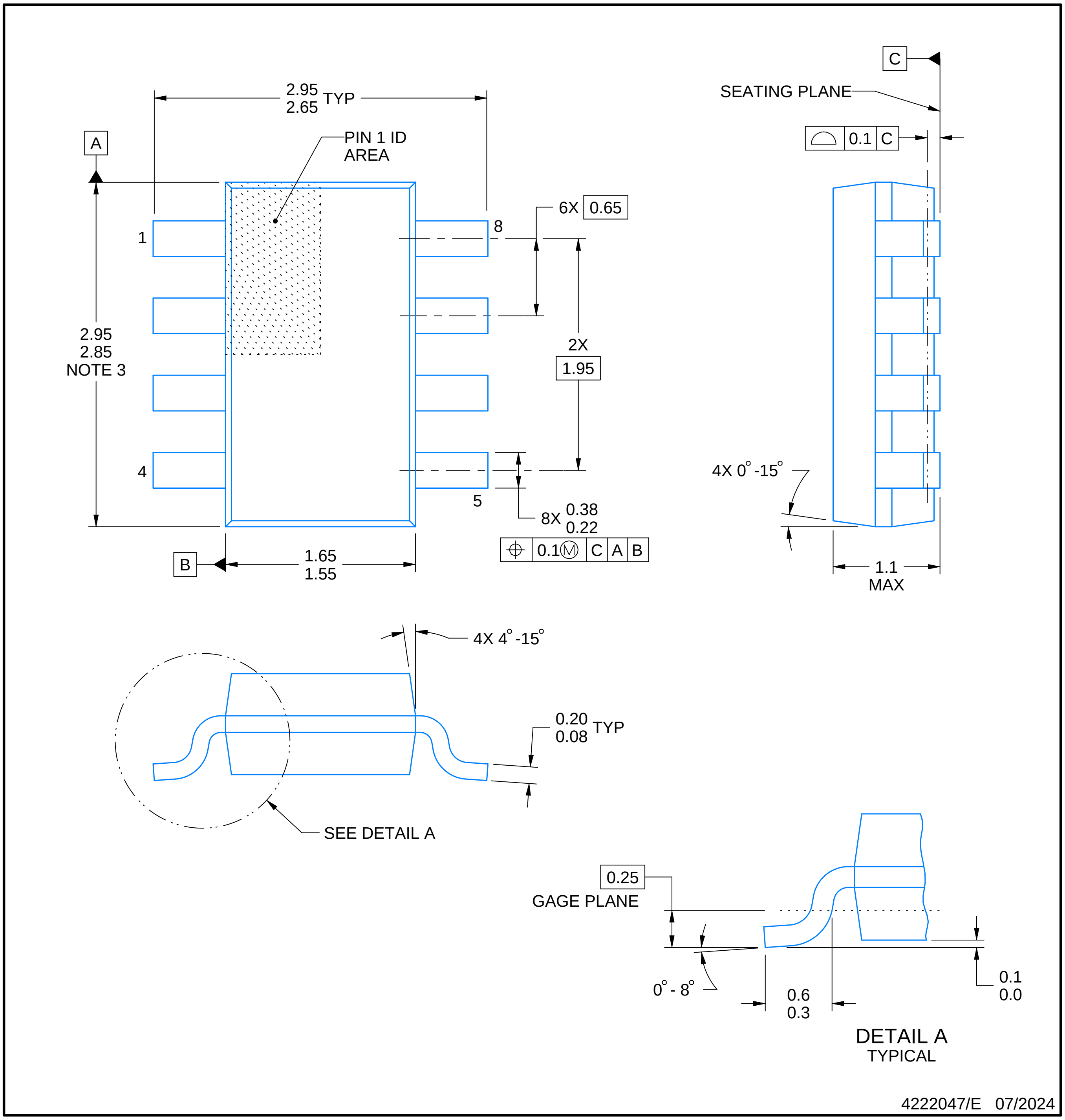


SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

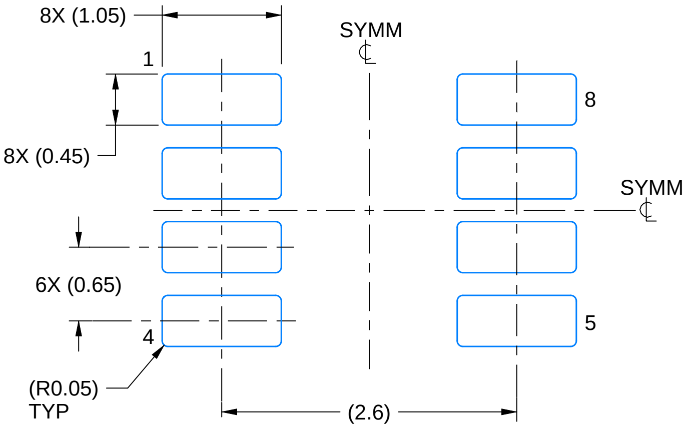
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.



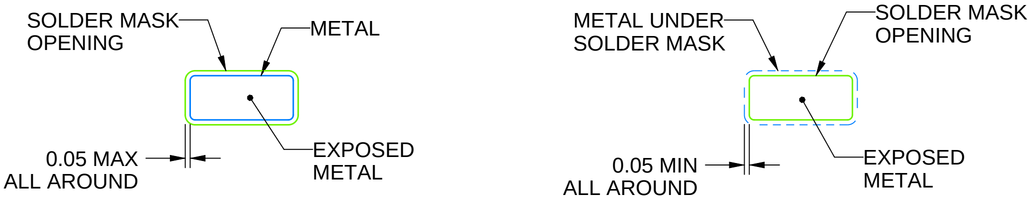
4222047/E 07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



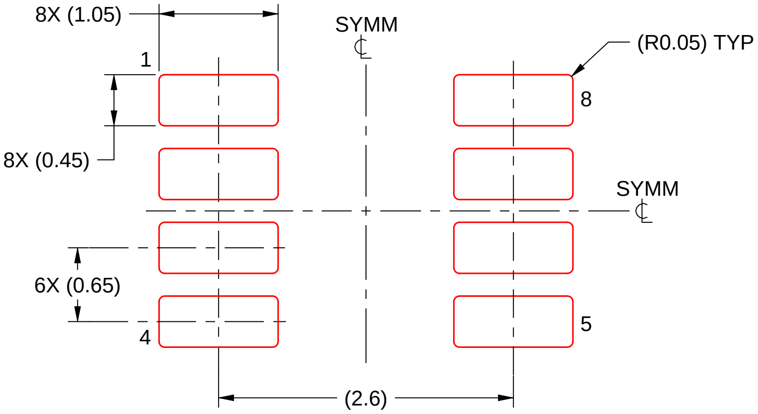
NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

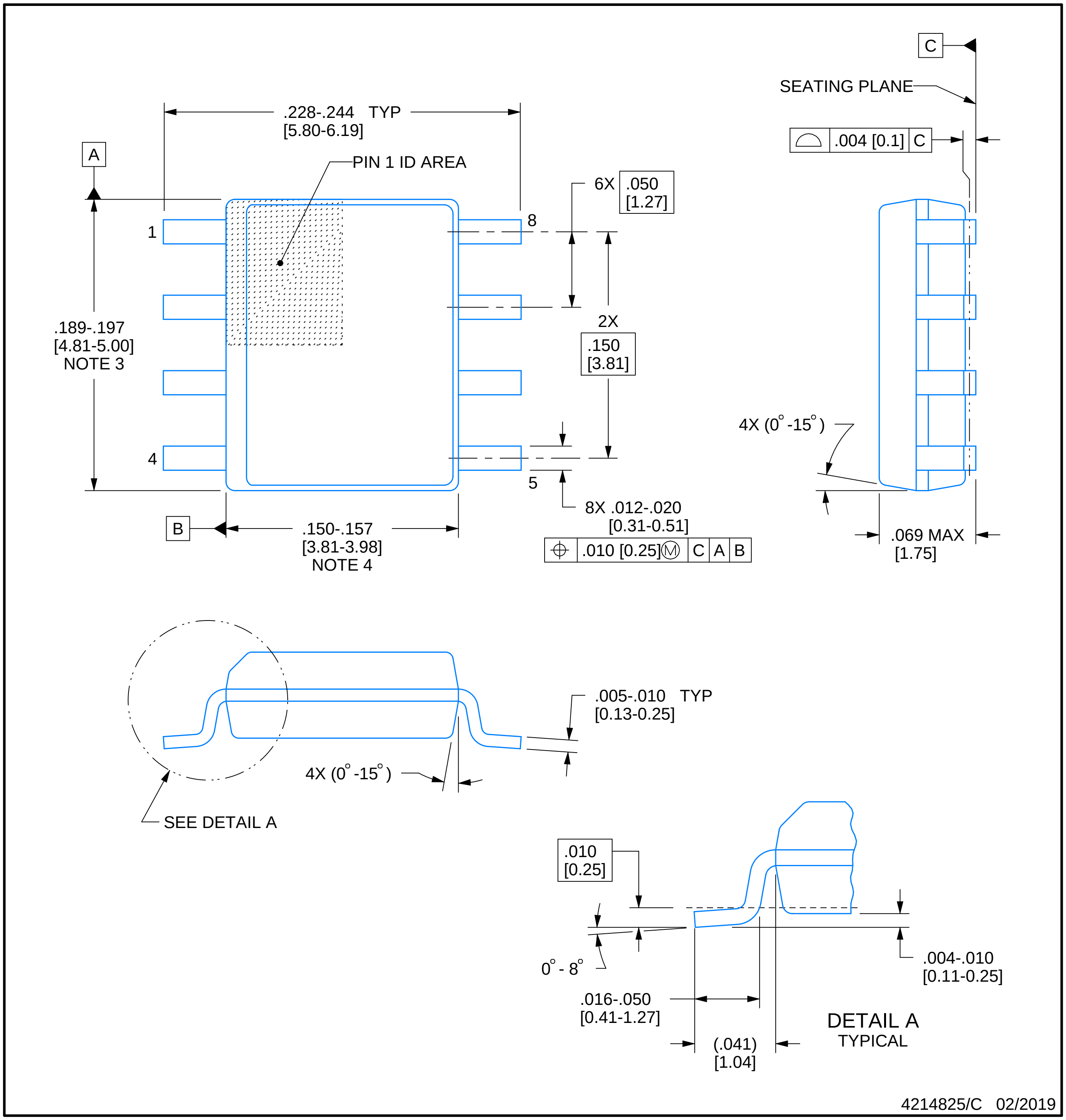
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

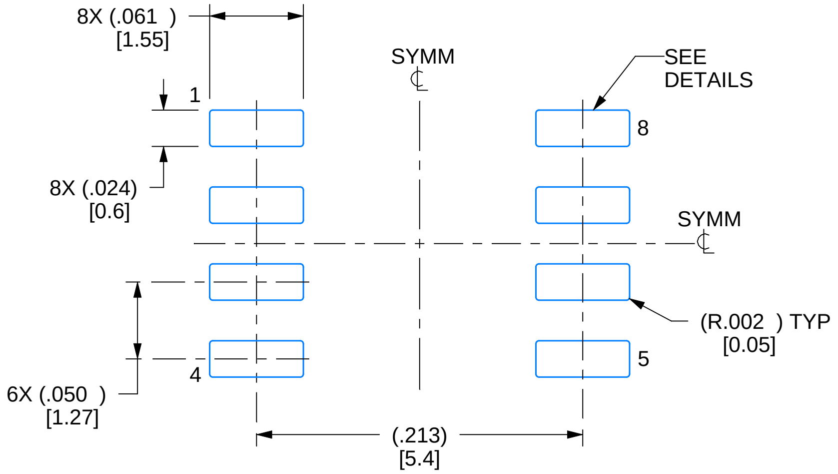
SMALL OUTLINE INTEGRATED CIRCUIT



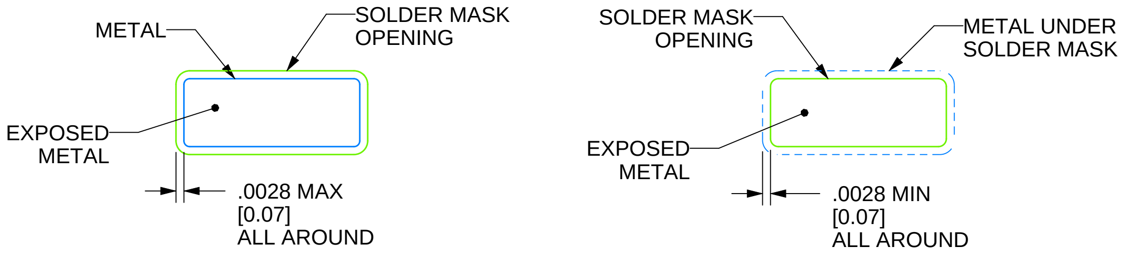
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



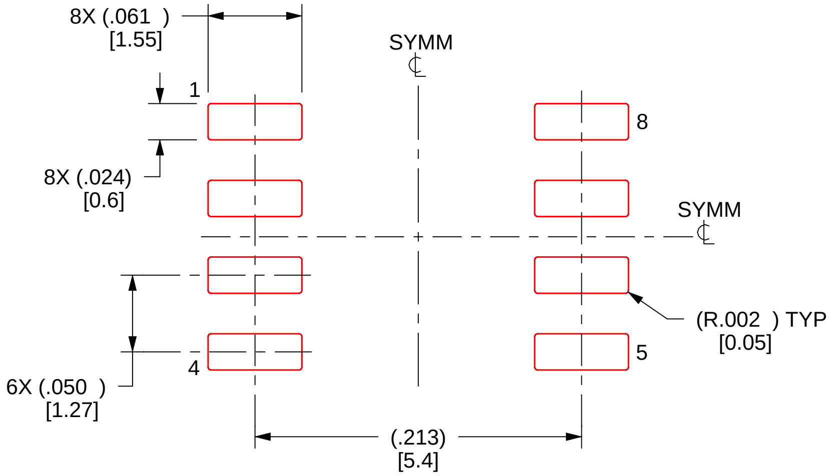
NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

NOTES: (continued)

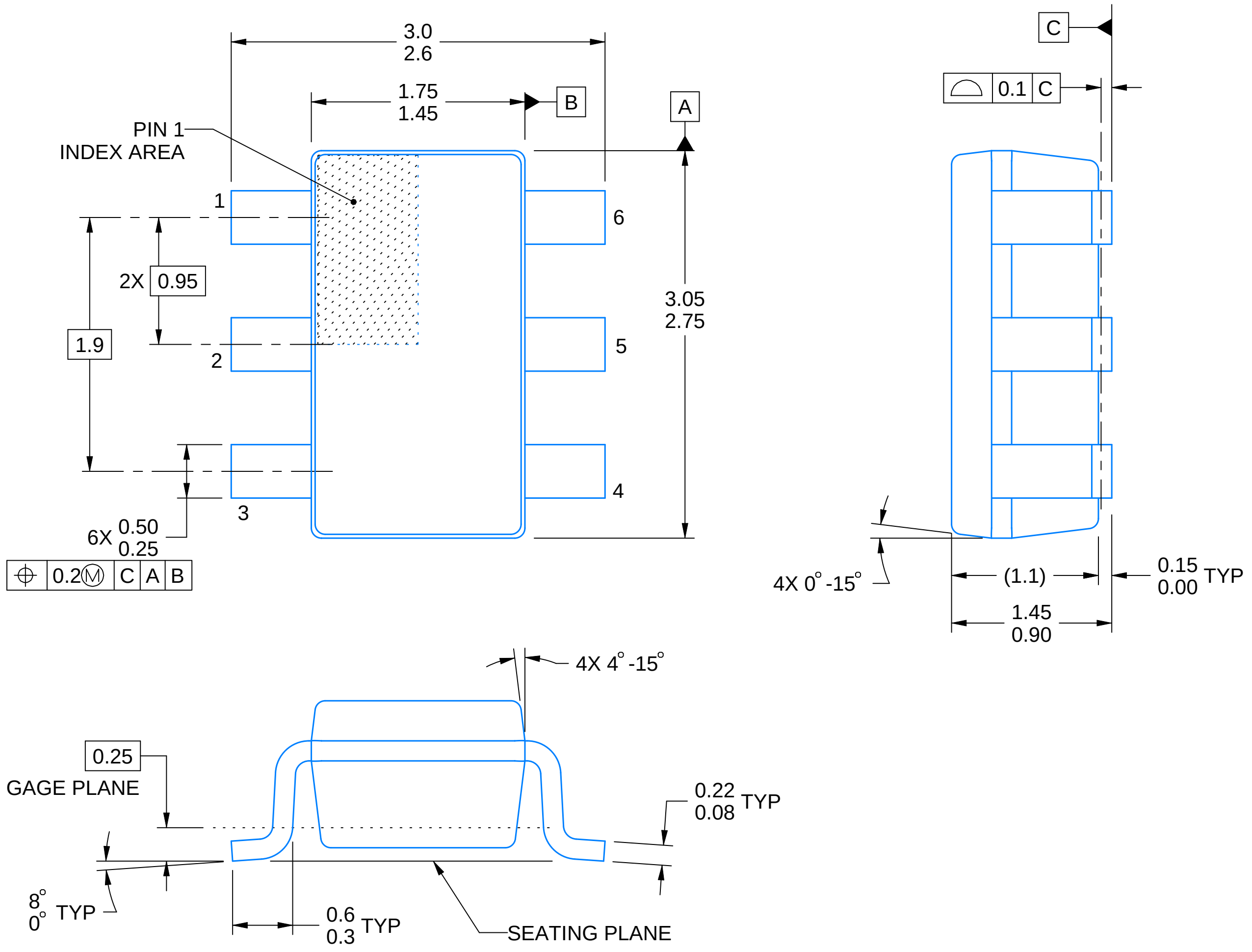
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

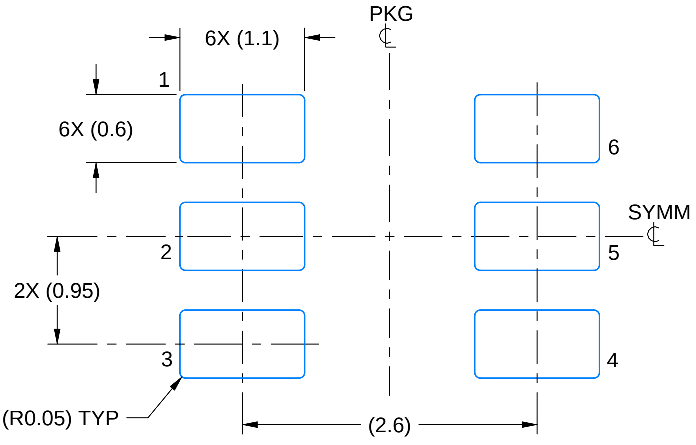
SMALL OUTLINE TRANSISTOR



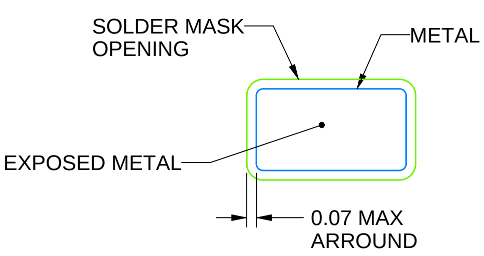
4214840/G 08/2024

NOTES:

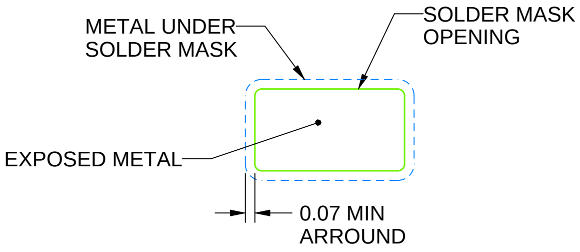
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK
DEFINED
(PREFERRED)

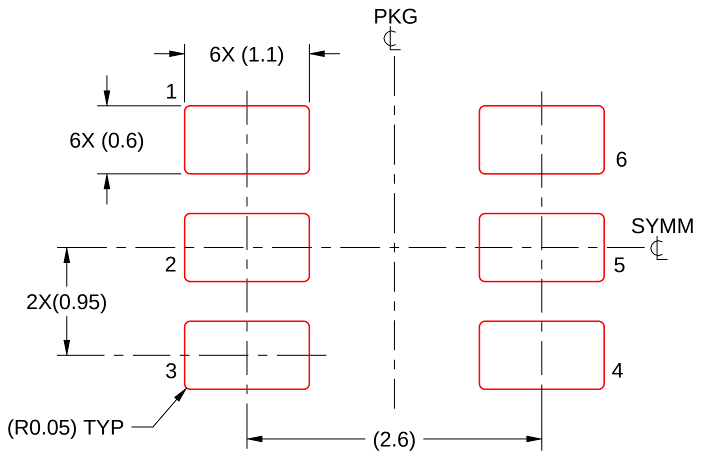


SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

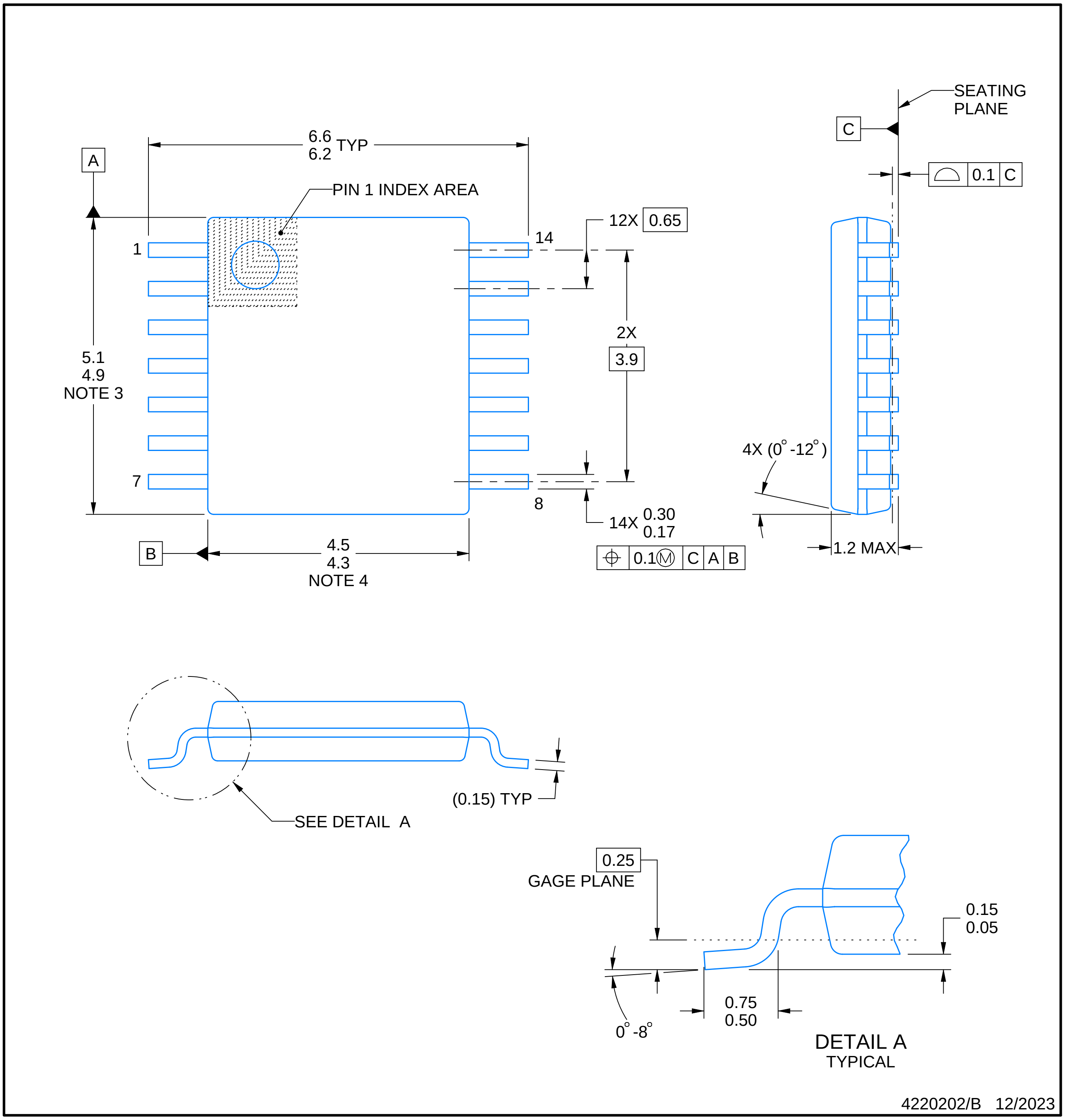
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

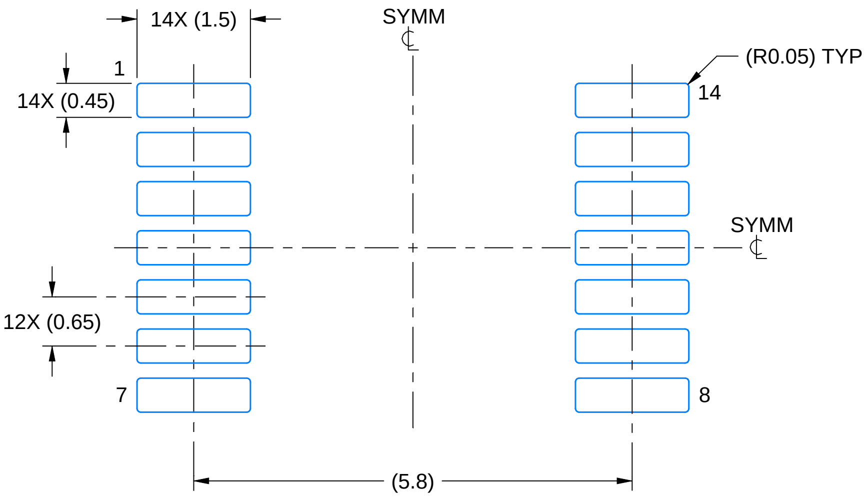
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

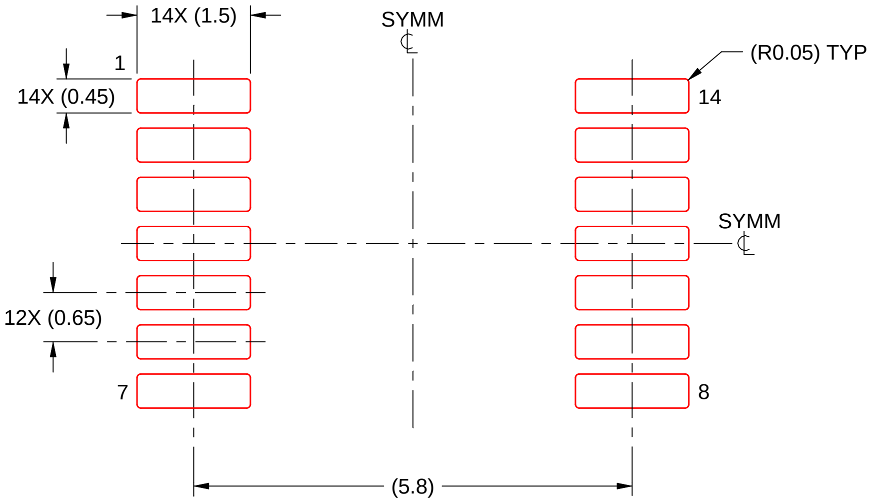
NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要通知和免责声明

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265