

BML60N120UC1

N-Channel Power MOSFET

600 V, 28 A, 120 mΩ

Description

BML60N120UC1 is power MOSFET using bestirpower's advanced super junction technology that can realize very low on resistance and gate charge.

It will provide much high efficiency by using optimized charge coupling technology. These user friendly devices give an advantage of Low EMI to designers as well as low switching loss.

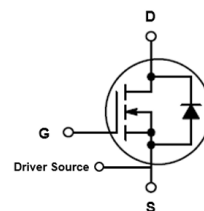
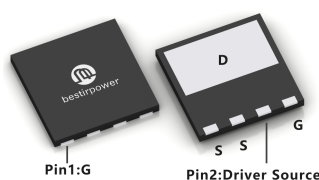
Applications

- AC/DC power supply.
- PC power.
- Telecom/Sever.
- Solar inverter.

Features

$BV_{DSS} @ T_{J,max}$	I_D	$R_{DS(on),max}$	$Q_{g,typ}$
650 V	23A	120 mΩ	53 nC

- Ultra-fast body diode.
- Extremely low losses due to very low FOM $R_{DS(on)} \cdot Q_g$ and E_{oss} .
- Very high commutation ruggedness.
- Qualified for industrial grade applications according to JEDEC.



Absolute Maximum Ratings ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter		Value	Unit
V_{DSS}	Drain to Source Voltage ¹⁾		600	V
V_{GSS}	Gate to Source Voltage ²⁾		± 30	V
I_D	Drain Current	Continuous ($T_C = 25^\circ\text{C}$)	23	A
		Continuous ($T_C = 125^\circ\text{C}$)	10	
I_{DM}	Drain Current	Pulsed ($T_C = 25^\circ\text{C}$)	84	A
E_{AS}	Single Pulsed Avalanche Energy ³⁾		506	mJ
I_{AR}	Repetitive Avalanche Energy		4.5	A
dv/dt	MOSFET dv/dt		50	V/ns
	Peak Diode Recovery dv/dt ⁴⁾		50	
P_{tot}	Power Dissipation	($T_C = 25^\circ\text{C}$)	152	W
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to 150	$^\circ\text{C}$
T_{sold}	Soldering temperature, wavesoldering only allowed at leads		260	$^\circ\text{C}$

1) Limited by T_j max. Maximum duty cycle $D=0.75$.

2) Pulse width t_p limited by $T_{j,max}$.

3) $V_{DD}=50\text{V}$, $R_G=25\Omega$, Starting $T_j=25^\circ\text{C}$.

4) $V_{DClk}=400\text{V}$; $V_{DS,peak} < V(BR)_{DSS}$; identical low side and high side switch with identical R_G .

Thermal Characteristics

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.82	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62	

Package Marking and Ordering Information

Part Number	Top Marking	Package	Packing Method	Quantity
BML60N120UC1	BML60N120UC1	DFN8*8	Tape & Reel	5000 units

Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	600	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}, T_J = 25^\circ\text{C}$	-	-	10	μA
I_{GSS}	Gate-Source Leakage Current	$V_{GS} = \pm 30\text{ V}, V_{DS} = 0\text{ V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	3.0	4.0	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 13\text{ A}, T_J = 25^\circ\text{C}$	-	100	120	mΩ

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V},$ $f = 250\text{ kHz}$	-	2380	-	pF
C_{oss}	Output Capacitance		-	89	-	pF
C_{rss}	Reverse transfer capacitance		-	4	-	pF
$C_{o(er)}$	Energy Related Output Capacitance ¹⁾	$V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$	-	73	-	pF
$C_{o(tr)}$	Time Related Output Capacitance ²⁾		-	379	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10 V	$V_{DD} = 400\text{ V}, I_D = 20\text{ A},$ $V_{GS} = 0\text{ to } 10\text{ V}$	-	53	-	nC
Q_{gs}	Gate to Source Charge		-	15	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	18	-	nC
R_G	Gate Resistance	$V_{DD} = 0\text{ V}, V_{GS} = 0\text{ V}, F = 1\text{ MHz}$	-	4	-	Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 400\text{ V}, I_D = 20\text{ A},$ $V_{GS} = 10\text{ V}$	-	15	-	ns
t_r	Turn-On Rise Time		-	24	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	72	-	ns
t_f	Turn-Off Fall Time		-	6	-	ns

Source-Drain Diode Characteristics

I_S	Maximum Continuous Diode Forward Current	-	-	23	A
V_{SD}	Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_F = 13\text{ A}, T_f = 25^\circ\text{C}$	-	0.85	V
t_{rr}	Reverse Recovery Time	$V_R = 400\text{ V}, I_F = 20\text{ A},$ $di_F/dt = 100\text{ A}/\mu\text{s}$	-	160	ns
Q_{rr}	Reverse Recovery Charge		-	1.03	μC
I_{mm}	Peak reverse recovery current		-	12	A

1) $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V.2) $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V.

Typical Performance Characteristics

Figure 1. Power dissipation

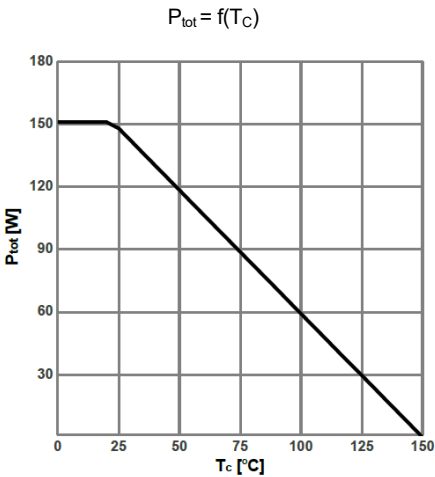


Figure 2. Max. transient thermal impedance

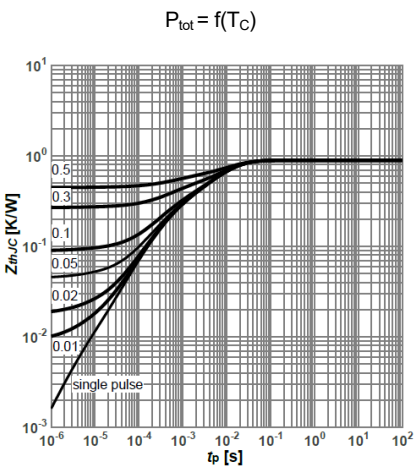


Figure 3. Safe operating area

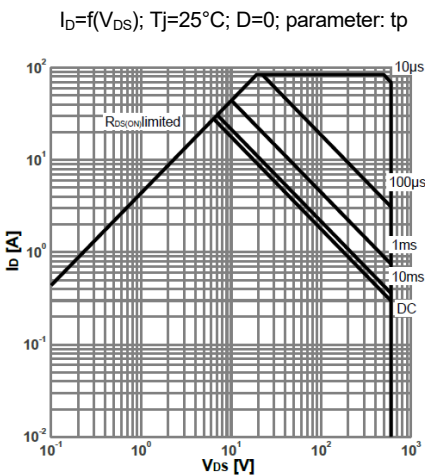


Figure 4. Typ. output characteristics

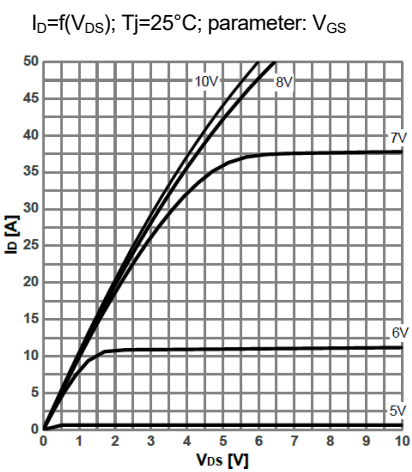


Figure 5. Typ. output Characteristics

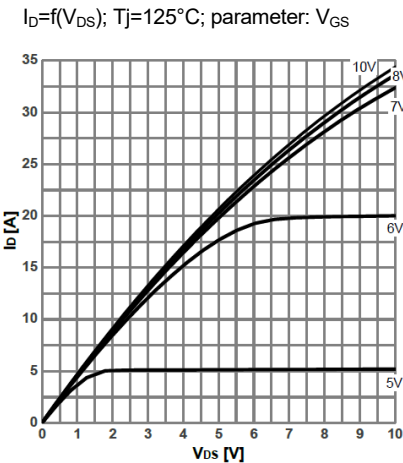
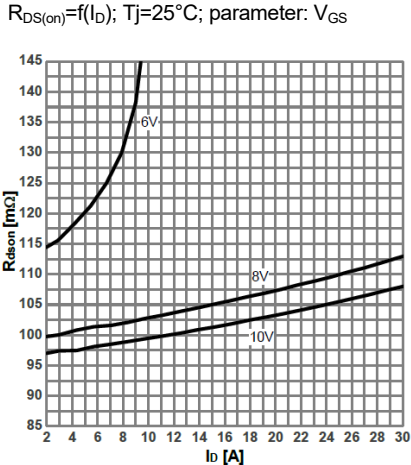


Figure 6. Typ. drain-source on-state resistance



Typical Performance Characteristics

Figure 7. Drain-soucre on-state resistance

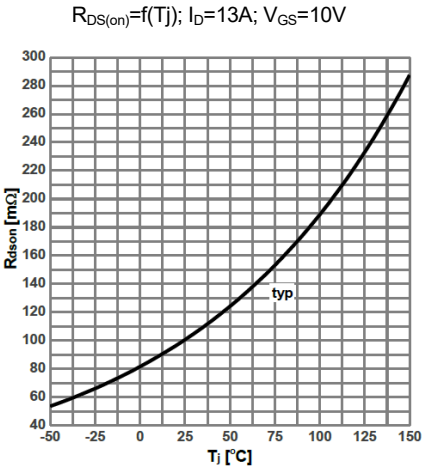


Figure 8. Typ. transfer characteristics

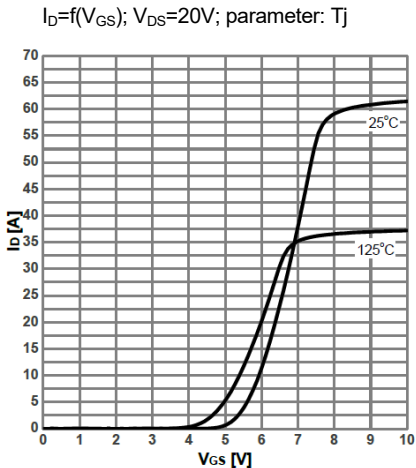


Figure 9. Typ. gate charge

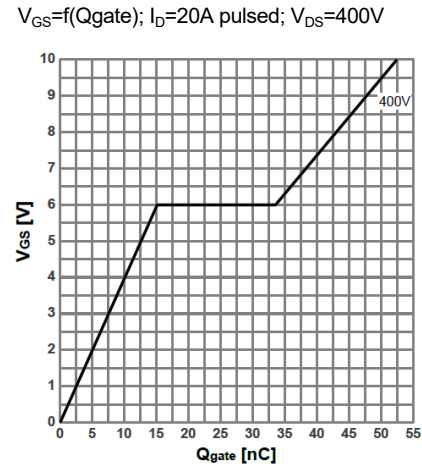


Figure 10. Foward characteristics of reverse diode

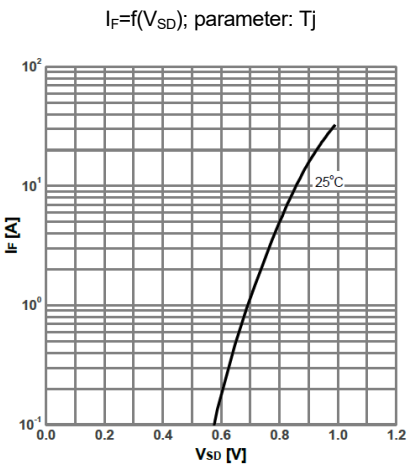


Figure 11. Drain-source breakdown coltage

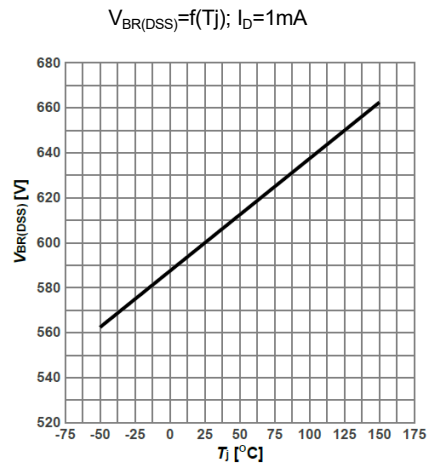


Figure 12. Typ. capacitances

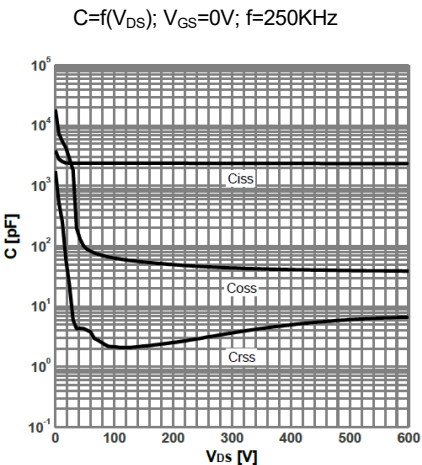
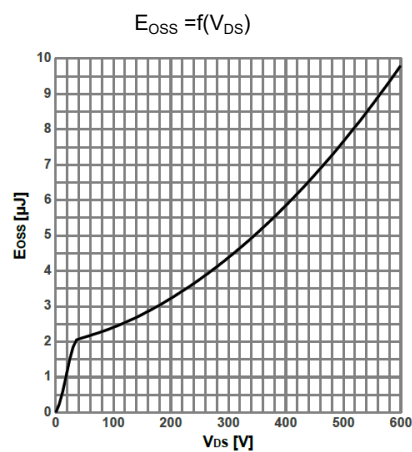


Figure 13. Typ. Coss stored energy



Test Circuits

Figure 14. Diode Characteristics

Test circuit for diode characteristics and Diode recovery waveform

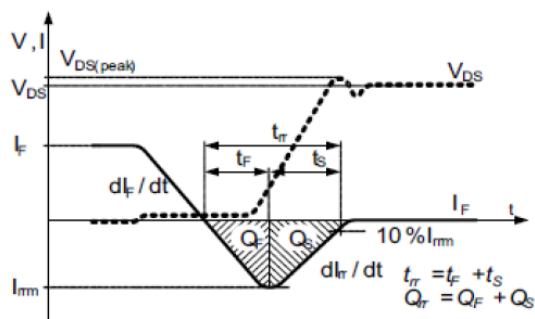


Figure 15. Switching Times

Switching times test circuit for inductive load and Switching times waveform

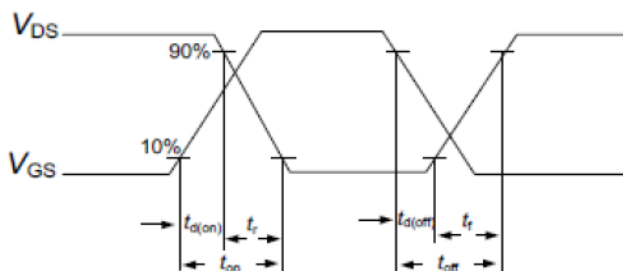
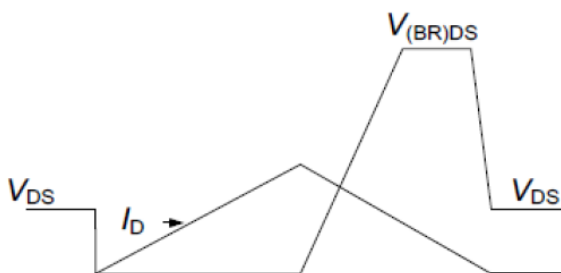


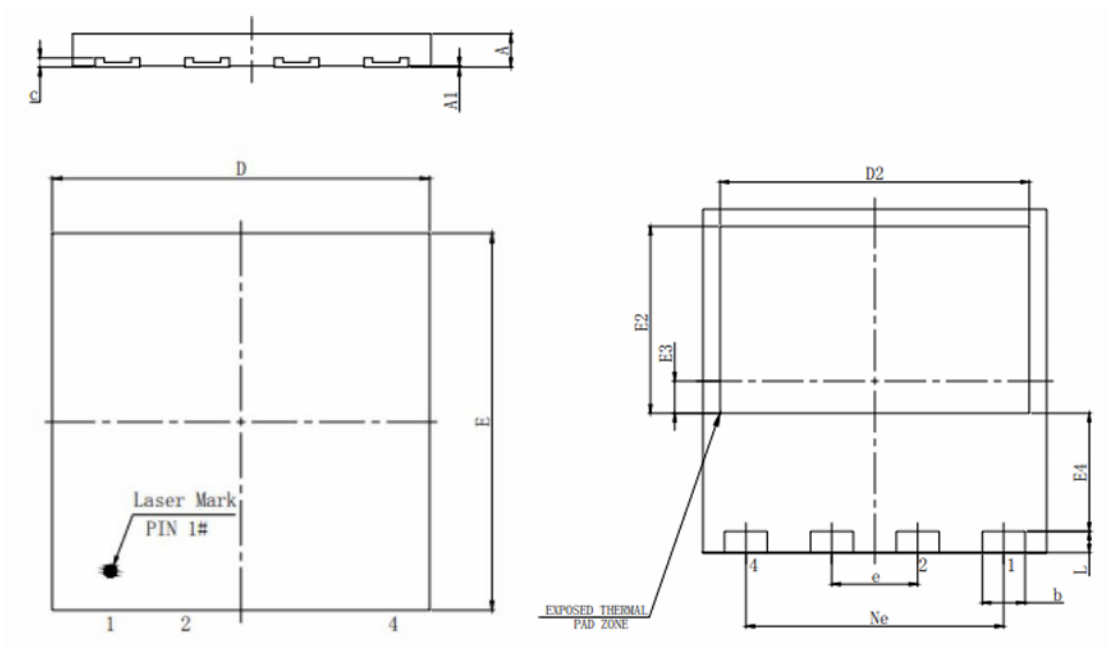
Figure 16. Unclamped Inductive Load

Unclamped inductive load test circuit and Unclamped inductive waveform



Package Outlines

DFN 8*8



Symbol	Dimensions In Millimeters		
	Min	Nom	Max
D	7.90	8.00	8.10
E	7.90	8.00	8.10
D2	7.10	7.20	7.30
E2	4.25	4.35	4.45
e	2.00BSC		
E3	0.75REF		
E4	2.75REF		
Ne	6.00BSC		
b	0.95	1.00	1.05
A	0.70	0.75	0.80
c	0.203REF		
A1	0	/	0.050
L	0.40	0.50	0.55

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