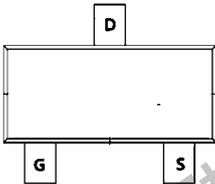
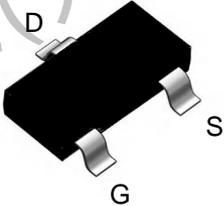
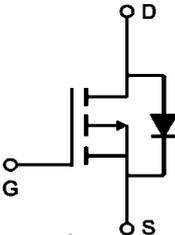


**TM05P03MI**

**P-Channel Enhancement Mosfet**

<p><b>General Description</b></p> <ul style="list-style-type: none"> <li>• Low <math>R_{DS(ON)}</math></li> <li>• RoHS and Halogen-Free Compliant</li> </ul> <p><b>Applications</b></p> <ul style="list-style-type: none"> <li>• Load switch</li> <li>• PWM</li> </ul>	<p><b>General Features</b></p> <p><math>V_{DS} = -30V</math> <math>I_D = -4.8A</math></p> <p><math>R_{DS(ON)} = 38m\Omega(Typ.) @ V_{GS} = -10V</math></p> <p>100% UIS Tested 100% <math>R_g</math> Tested</p> 
--	--

MI: SOT-23-3L

Marking: A19T OR X1

Absolute Maximum Ratings ( $T_C = 25^\circ C$ unless otherwise noted)			
Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	-30	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ -10V^1$	-4.8	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ -10V^1$	-3.2	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	-25	A
$P_D @ T_A = 25^\circ C$	Total Power Dissipation <sup>3</sup>	1.4	W
$T_{STG}$	Storage Temperature Range	-55 to 175	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 175	$^\circ C$

Thermal Data				
Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-ambient <sup>1</sup>	---	170	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	---	---	$^\circ C/W$

## TM05P03MI

## P-Channel Enhancement Mosfet

### Electrical Characteristics (T<sub>J</sub>=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =-250uA	-30	-32	---	V
ΔBVDSS/ΔT <sub>J</sub>	BV <sub>DSS</sub> Temperature Coefficient	Reference to 25°C, I <sub>D</sub> =-1mA	---	-0.014	---	V/°C
RDS(ON)	Static Drain-Source On-Resistance	V <sub>GS</sub> =-10V, I <sub>D</sub> =-3A	---	38	45	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-3A	---	46	56	
VGS(th)	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =-250uA	-1.0	-1.5	-2.0	V
ΔVGS(th)	V <sub>GS(th)</sub> Temperature Coefficient		---	2.6	---	mV/°C
IDSS	Drain-Source Leakage Current	V <sub>DS</sub> =-24V, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C	---	---	-1	uA
		V <sub>DS</sub> =-24V, V <sub>GS</sub> =0V, T <sub>J</sub> =55°C	---	---	-5	
IGSS	Gate-Source Leakage Current	V <sub>GS</sub> =±12V, V <sub>DS</sub> =0V	---	---	±100	nA
gfs	Forward Transconductance	V <sub>DS</sub> =-5V, I <sub>D</sub> =-3A	---	5.6	---	S
Q <sub>g</sub>	Total Gate Charge (-4.5V)	V <sub>DS</sub> =-15V, V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-3A	---	11.9	---	nC
Q <sub>gs</sub>	Gate-Source Charge		---	1.8	---	
Q <sub>gd</sub>	Gate-Drain Charge		---	3	---	
Td(on)	Turn-On Delay Time	V <sub>DD</sub> =-15V, V <sub>GS</sub> =-4.5V, R <sub>G</sub> =3.3Ω, I <sub>D</sub> =-3A	---	6.6	---	ns
T <sub>r</sub>	Rise Time		---	27.8	---	
Td(off)	Turn-Off Delay Time		---	46.2	---	
T <sub>f</sub>	Fall Time		---	20.6	---	
Ciss	Input Capacitance	V <sub>DS</sub> =-15V, V <sub>GS</sub> =0V, f=1MHz	---	290	---	pF
Coss	Output Capacitance		---	73	---	
Crss	Reverse Transfer Capacitance		---	71	---	
IS	Continuous Source Current <sup>1,4</sup>	V <sub>G</sub> =V <sub>D</sub> =0V, Force Current	---	---	-4.8	A
VSD	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V, I <sub>S</sub> =-1A, T <sub>J</sub> =25°C	---	---	-1.2	V

**Note :**

- 1.The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width ≅ 300us , duty cycle ≅ 2%
- 3.The power dissipation is limited by 150°C junction temperature
- 4.The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub> , in real applications , should be limited by total power dissipation.



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P-Channel Enhancement Mosfet

Typical Characteristics

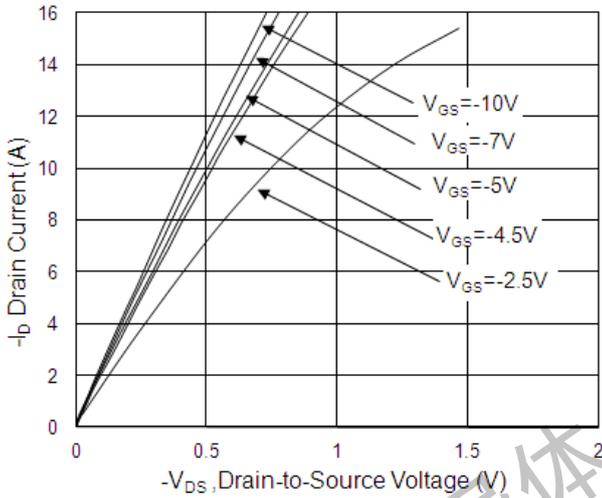


Fig.1 Typical Output Characteristics

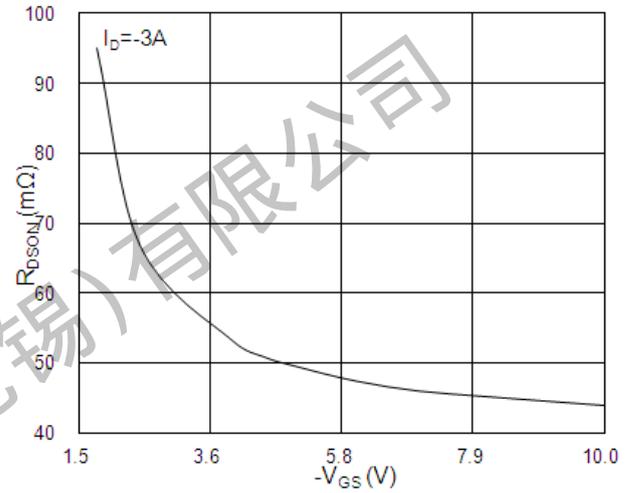


Fig.2 On-Resistance vs. G-S Voltage

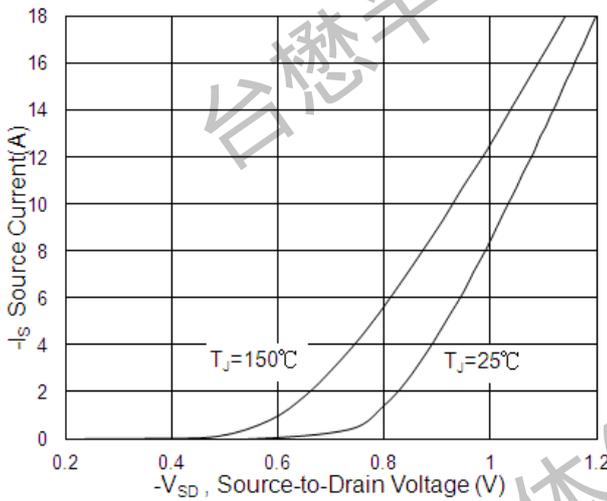


Fig.3 Forward Characteristics Of Reverse

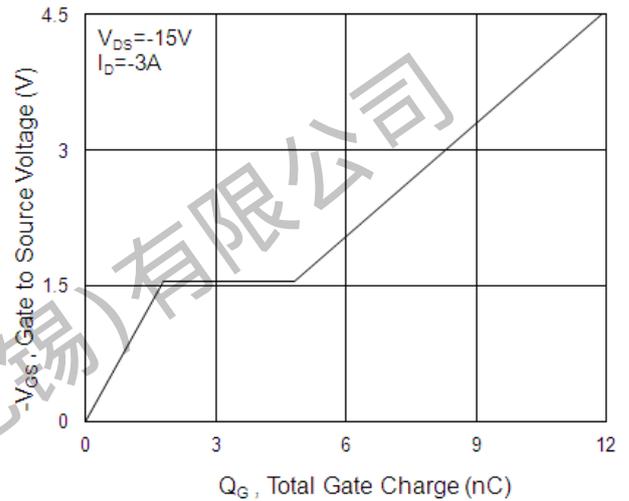


Fig.4 Gate-Charge Characteristics

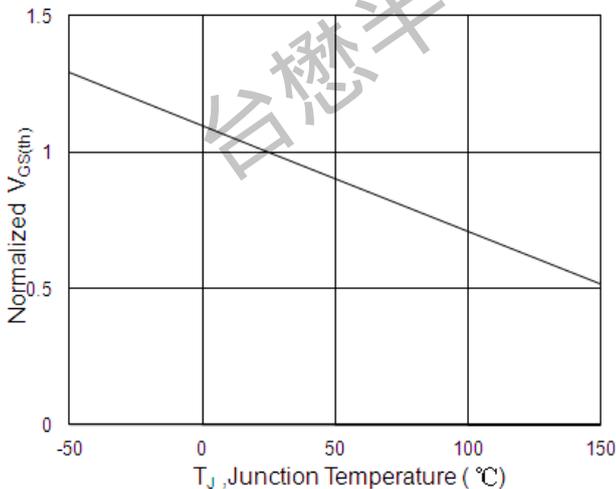


Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$

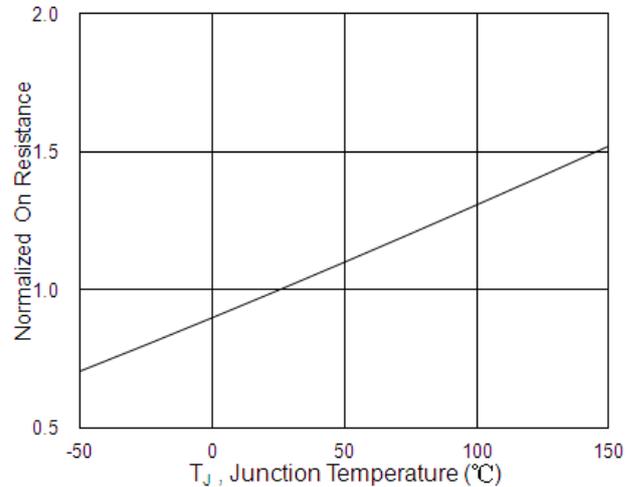


Fig.6 Normalized  $R_{DS(on)}$  vs.  $T_J$

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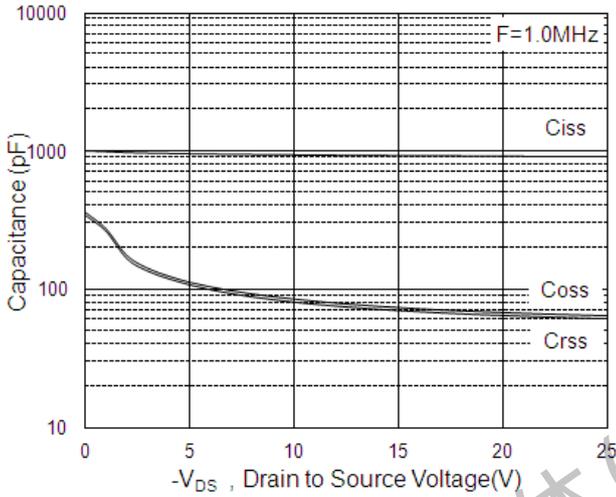


Fig.7 Capacitance

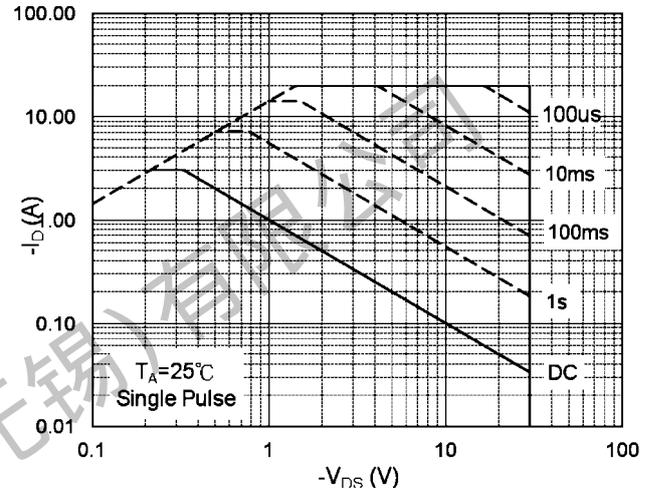


Fig.8 Safe Operating Area

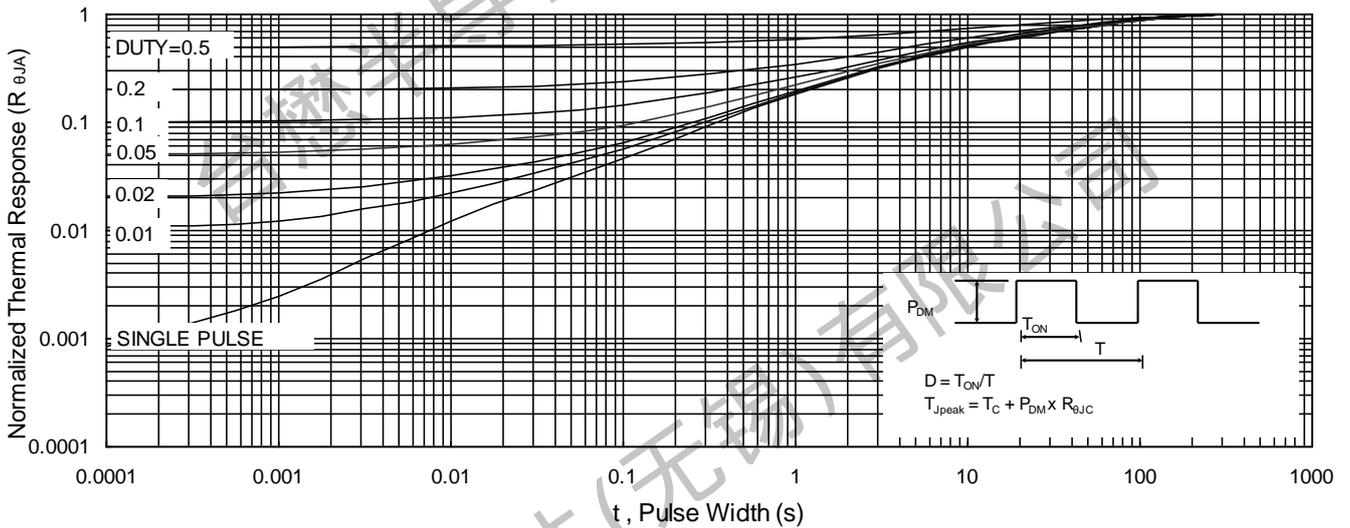


Fig.9 Normalized Maximum Transient Thermal Impedance

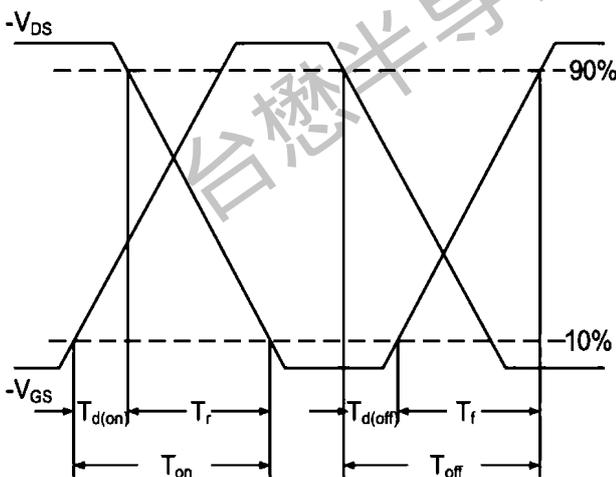


Fig.10 Switching Time Waveform

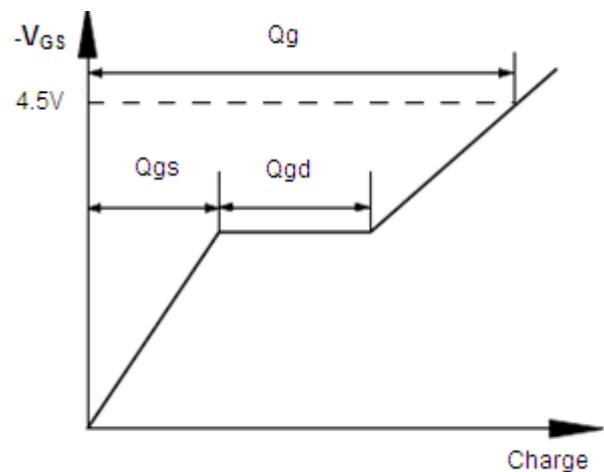


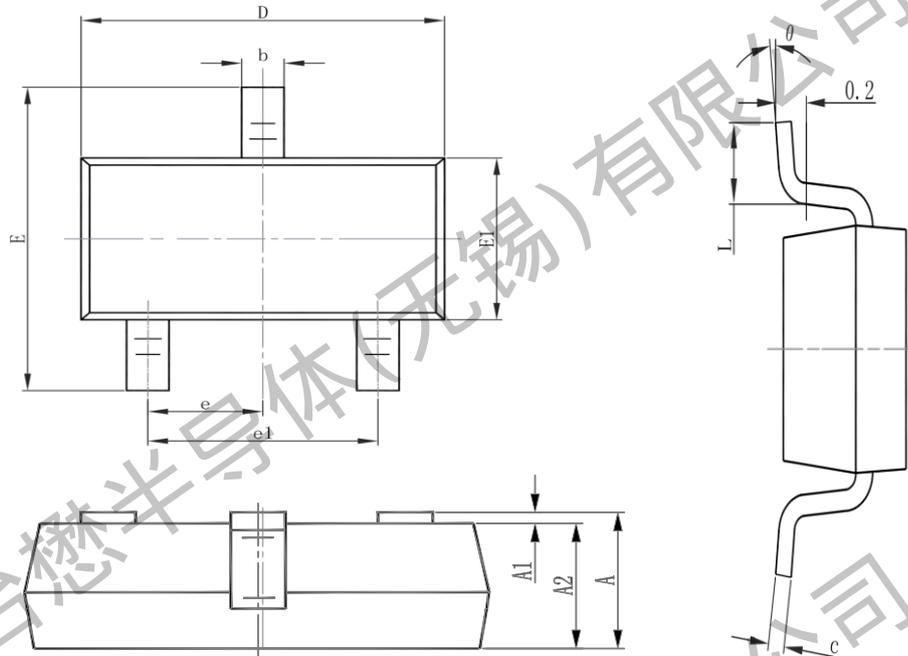
Fig.11 Gate Charge Waveform



TM05P03MI

P-Channel Enhancement Mosfet

Package Mechanical Data:SOT-23-3L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E1	1.500	1.700	0.059	0.067
E	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
theta	0°	8°	0°	8°

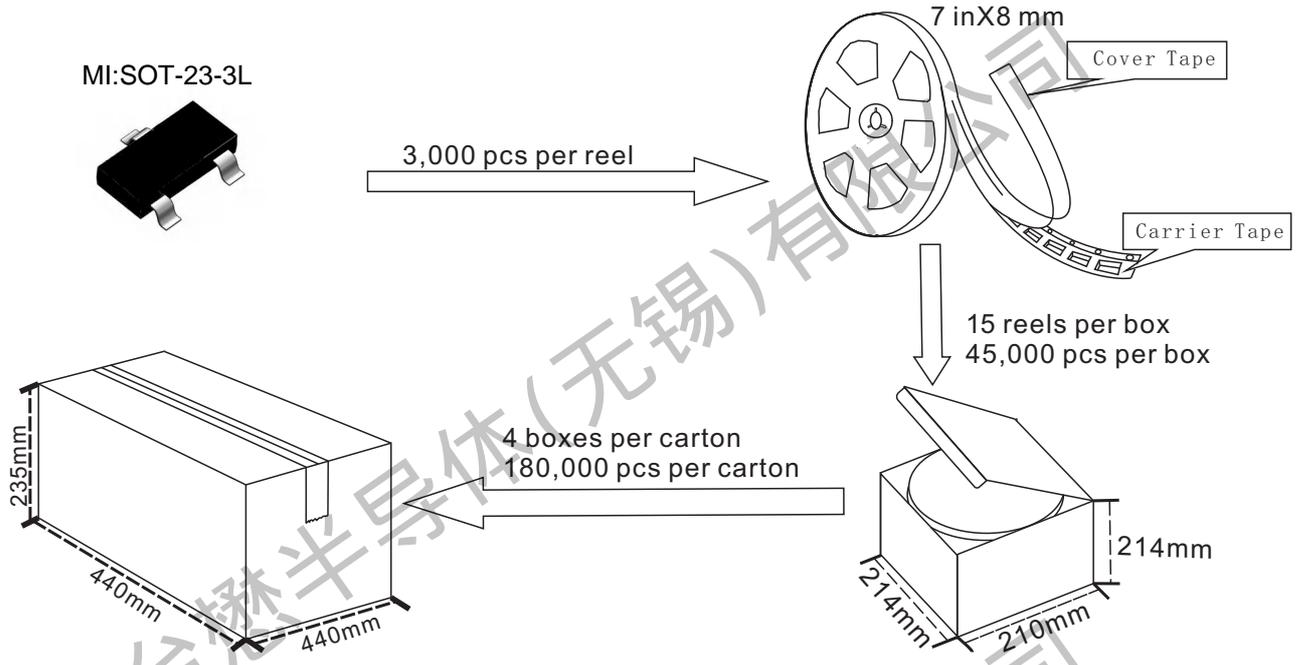


TM05P03MI

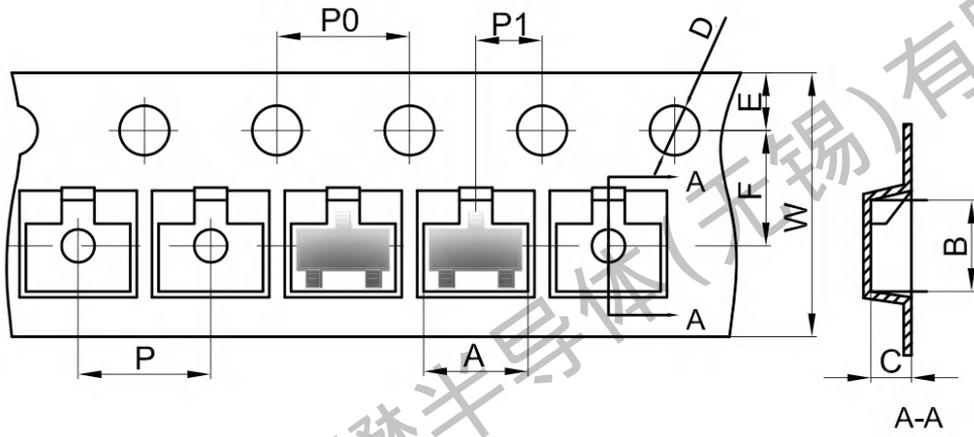
P-Channel Enhancement Mosfet

SOT-23-3L Packing

1. The method of packaging and dimension are shown as below figure. (Dimension in mm)



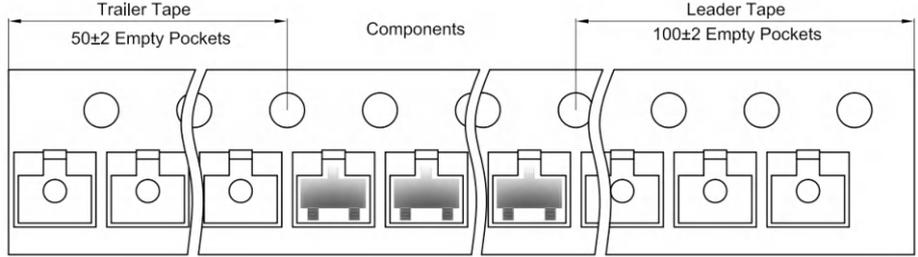
SOT-23-3L Embossed Carrier Tape



Dimensions are in millimeter

Pkg type	A	B	C	D	E	F	P0	P	P1	W
SOT-23-3L	3.15	2.77	1.22	Ø1.50	1.75	3.50	4.00	4.00	2.00	8.00

SOT-23-3L Tape Leader and Trailer





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Revision history:

Date	Rev	Description	Page
2023.05.04	23.05	Original	