

## AUFSL3607-VB Datasheet N-Channel 80 V (D-S) MOSFET

PRODUCT SUMMARY					
V <sub>DS</sub> (V)	$R_{DS(on)}(\Omega)$ Max.	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ.)		
	0.0065 at Vgs= 10 V	85 <sup>a</sup>			
80	0.0070 at Vgs =6.0 V	80ª	17.1 nC		
	0.010 at Vgs =4.5 V	60 <sup>a</sup>			

#### **FEATURES**

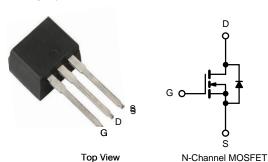
- Trench Power MOSFET
- 100 % R<sub>g</sub> and UIS Tested



#### **APPLICATIONS**

- Primary Side Switching
- Synchronous Rectification
- DC/AC Inverters
- LED Backlighting

#### TO-262



Parameter		Symbol	Limit	Unit	
Drain-Source Voltage	V <sub>DS</sub>	80			
Gate-Source Voltage	V <sub>GS</sub>	± 20			
	T <sub>C</sub> = 25 °C		85 <sup>a</sup>		
Continuous Dunis Comment (T. 150 °C)	T <sub>C</sub> = 70 °C		65	7	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	T <sub>A</sub> = 25 °C	I <sub>D</sub>	28.6 <sup>b, c</sup>		
	T <sub>A</sub> = 70 °C		24.9 <sup>b, c</sup>	Α	
Pulsed Drain Current (t = 100 μs)		I <sub>DM</sub>	250		
Continuous Courses Drain Diada Current	T <sub>C</sub> = 25 °C	,	85		
Continuous Source-Drain Diode Current	T <sub>A</sub> = 25 °C	I <sub>S</sub>	4.5 <sup>b, c</sup>		
Single Pulse Avalanche Current	. 0.1!!	I <sub>AS</sub>	30		
Single Pulse Avalanche Energy	L = 0.1 mH	E <sub>AS</sub>	45	mJ	
	T <sub>C</sub> = 25 °C		62.5		
Manian and Danier Disable attack	T <sub>C</sub> = 70 °C	Б	40	w	
Maximum Power Dissipation	T <sub>A</sub> = 25 °C	P <sub>D</sub>	5 <sup>b, c</sup>	VV	
	T <sub>A</sub> = 70 °C		3.2 <sup>b, c</sup>	7	
Operating Junction and Storage Temperature F	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C		
Soldering Recommendations (Peak Temperatur	-	260	°C		

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>b, f</sup>	t ≤ 10 s	$R_{thJA}$	20	25	°C/W
Maximum Junction-to-Case (Drain)	Steady State	$R_{thJC}$	1.5	2.0	C/VV

#### Notes

- a. Package limited.
- b. Surface mounted on 1" x 1" FR4 board.
- c. t = 10 s
- d. The TO-220 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- f. Maximum under steady state conditions is 70 °C/W.



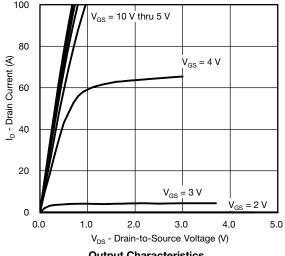
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	80			V
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$			37		1400
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I <sub>D</sub> = 250 μA		- 6.1		mV/°C
Gate-Source Threshold Voltage	V <sub>GS(th</sub> )	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	2.0		4.5	V
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA
7 0		$V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}$			1	μA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			10	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	30			Α
	, ,	$V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}$		0.0065		
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = 6 \text{ V}, I_D = 15 \text{ A}$		0.0070		Ω
	, ,	$V_{GS} = 4.5 \text{ V}, I_D = 10 \text{ A}$		0.0100		
Forward Transconductancea	9 <sub>fs</sub>	$V_{DS} = 10 \text{ V}, I_D = 20 \text{ A}$		60		S
Dynamic <sup>b</sup>						
Input Capacitance	C <sub>iss</sub>			8000		
Output Capacitance	C <sub>oss</sub>	$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		950		pF
Reverse Transfer Capacitance	C <sub>rss</sub>			276		1
Total Gate Charge		$V_{DS} = 40 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 10 \text{ A}$		35.5	54	
	$Q_g$	$V_{DS} = 40 \text{ V}, V_{GS} = 6 \text{ V}, I_D = 10 \text{ A}$		22	33	7
				17.1	26	
Gate-Source Charge	$Q_{gs}$	$V_{DS} = 40 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 10 \text{ A}$		5.3		nC
Gate-Drain Charge	$Q_{gd}$			7.3		1
Output Charge	Q <sub>oss</sub>	$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}$		57	86	
Gate Resistance	$R_g$	f = 1 MHz	0.5	1.3	2	Ω
Turn-On Delay Time	t <sub>d(on)</sub>			12	24	
Rise Time	t <sub>r</sub>	$V_{DD} = 40 \text{ V}, R_L = 4 \Omega$		8	16	
Turn-Off DelayTime	t <sub>d(off)</sub>	$I_D \cong 10^{\circ} \text{A}, V_{GEN} = 10^{\circ} \text{V}, R_g = 1^{\circ} \Omega$		32	64	
Fall Time	t <sub>f</sub>			7	14	1
Turn-On Delay Time	t <sub>d(on)</sub>			14	28	ns
Rise Time	t <sub>r</sub>	$V_{DD} = 40 \text{ V}, R_{L} = 4 \Omega$		11	22	<del>-</del> - -
Turn-Off DelayTime	t <sub>d(off)</sub>	$I_D \cong 10 \text{ A}, V_{GEN} = 6.0 \text{ V}, R_g = 1 \Omega$		30	60	
Fall Time	t <sub>f</sub>			8	16	
<b>Drain-Source Body Diode Characteristic</b>	s					
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			75	۸
Pulse Diode Forward Current (t = 100 μs)	I <sub>SM</sub>				150	A
Body Diode Voltage	$V_{SD}$	I <sub>S</sub> = 5 A		0.76	1.1	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>			38	75	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	L 10 A dl/d+ 100 A / T 05 °C		36	70	nC
Reverse Recovery Fall Time	ta	$I_F = 10 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 ^{\circ}\text{C}$		19		
Reverse Recovery Rise Time	t <sub>b</sub>			19		ns

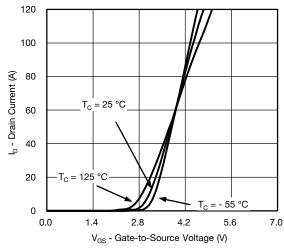
#### Notes

- a. Pulse test; pulse width  $\leq 300~\mu s,~duty~cycle \leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

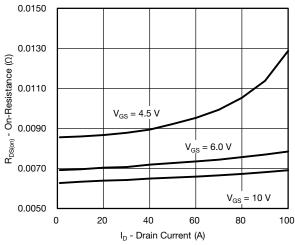


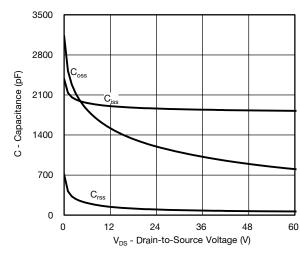






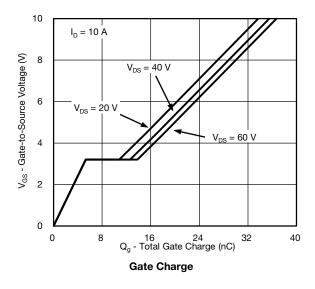


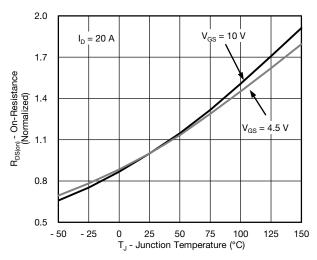




#### On-Resistance vs. Drain Current

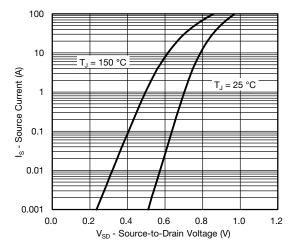
Capacitance



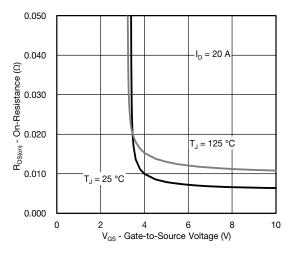


On-Resistance vs. Junction Temperature

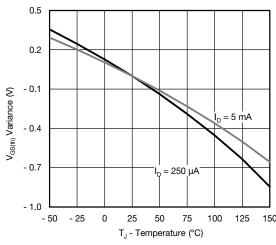




Source-Drain Diode Forward Voltage

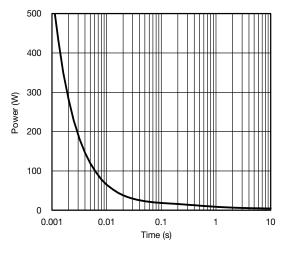


On-Resistance vs. Gate-to-Source Voltage

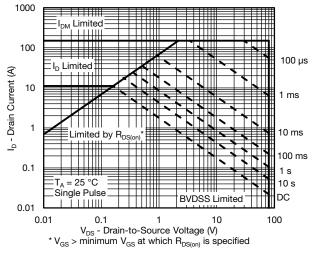


Threshold Voltage

4

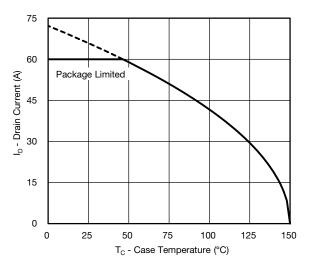


Single Pulse Power, Junction-to-Ambient

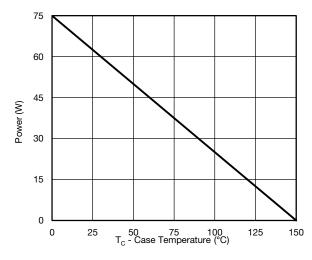


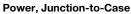
Safe Operating Area, Junction-to-Ambient

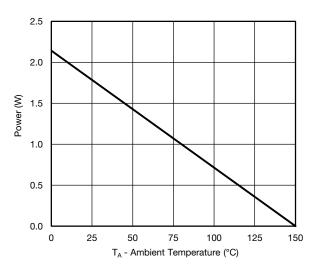




#### **Current Derating\***



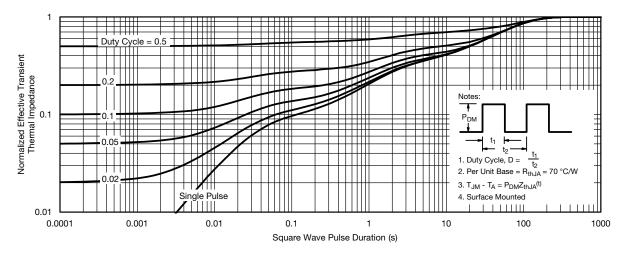




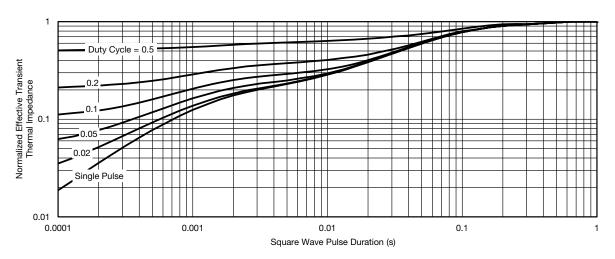
Power, Junction-to-Ambient

<sup>\*</sup> The power dissipation  $P_D$  is based on  $T_{J(max.)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





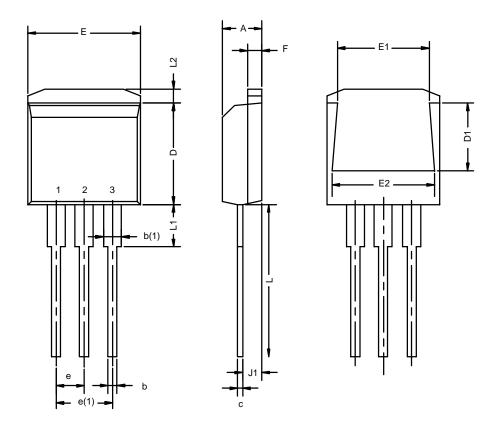
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case



## TO-262: 3-LEAD



	MILLIM	ETERS*	INC	HES		
Dim	Min	Max	Min	Max		
Α	4.32	4.70	0.170	0.185		
b	0.64	1.00	0.025	0.039		
b(1)	1.14	1.40	0.045	0.055		
С	0.36	0.50	0.014	0.020		
D	8.64	9.65	0.340	0.380		
D1	5.59	6.10	0.220	0.240		
е	2.41	2.67	0.095	0.105		
e(1)	4.95	5.33	0.195	0.210		
Е	10.03	10.41	0.395	0.410		
E1	7.87	8.64	0.310	0.340		
E2	9.02	9.53	0.355	0.375		
F	1.14	1.40	0.045	0.055		
J1	2.41	2.79	0.095	0.110		
L	13.08	14.22	0.515	0.560		
L1	-	3.81	-	0.150		
L2	1.02	1.40	0.040	0.055		
ECN: T-022 DWG: 585	234—Rev. C, 1 5	4-Oct-02				

<sup>\*</sup>Use millimeters as the primary measurement



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