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# NC7SZ32

## Single 2-Input Positive-OR Gate

www.sot23.com.tw

## General Description

This single 2-input positive-OR gate is designed for 1.65-V to 5.5-V $V_{CC}$ operation.

The NC7SZ32 performs the Boolean function = A + B or $Y = \overline{\overline{A} \cdot \overline{B}}$ in positive logic.

The CMOS device has high output drive while maintaining low static power dissipation over a broad $_{CC}$ operating range.

The NC7SZ32 device is available in a variety of packages.

## Features

- **Low Power Consumption, 10-μA Max ICC**
- **Supports 5-V VCC Operation**
- **Inputs Accept Voltages to 5.5 V**
- **Provides Down Translation to VCC**
- **Max tpd of 3.6 ns at 3.3 V**
- **±24-mA Output Drive at 3.3 V**

## Applications

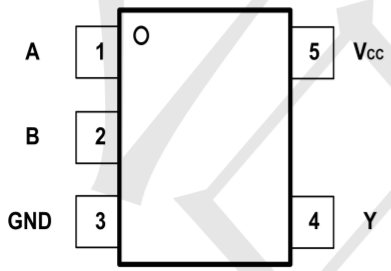
- **Personal Navigation Device (GPS)**
- **AV Receiver**
- **High-Speed Data Acquisition and Generation**
- **SSD: Internal and External**
- **Digital Picture Frame (DPF)**
- **TV: LCD/Digital and High-Definition (HDTV)**

## Ordering Information

| ORDER NUMBER | PACKAGE DESCRIPTION | PACKAGE OPTION |
|---|---|---|
| NC7SZ32M5X | SOT23-5 | Tape and Reel,3000 |
| NC7SZ32P5X | SOT353 | Tape and Reel,3000 |

## Pin Configuration

SOT23-5/SOT353




## Marking

**NC7SZ32M5X Marking:7Z32D**

**NC7SZ32P5X Marking:Z32C**

## Logic Diagram

**Simplified Schematic**


## Function Table

| INPUT(A) | INPUT(B) | OUTPUT(Y) |
|---|---|---|
| H | X | H |
| X | H | H |
| L | L | L |

Note: H: HIGH voltage level; L: LOW voltage level; X: Don't care.

## Absolute Maximum Ratings

| Parameters | Min. | Max. | Unit |
|---|---|---|---|
| Supply Voltage, VCC=(V+)-(V-), Single-supply | | 6.5 | V |
| Supply Voltage, VCC=(V+)-(V-), Dual-supply | | ±3.25 | V |
| Select Input Voltage | V- | V+ | V |
| Maximum Junction Temperature | -55 | 150 | ℃ |
| Storage Temperature Range | -55 | 150 | ℃ |
| Continuous Output Current | | ±50 | mA |
| Continuous Current through $V_{CC}$ or GND | | ±100 | mA |

## ESD Ratings

| ESD | | | VALUE | UNIT |
|---|---|---|---|---|
| V(ESD) | Electrostatic discharge | Human-body model (HBM) | 4K | V |
| | | Charge device model (CDM) | 2K | V |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

| Symbol | Parameters | Min | Max | Unit |
|---|---|---|---|---|
| VCC | Supply Voltage | 1.65 | 5.5 | V |
| TA | Operating Temperature | -40 | 125 | ℃ |

## Electrical Characteristics

Vcc=1.65V to 5.5V, FULL=–40°C to +125°C, Typical values are at TA = +25°C. (unless otherwise noted)

| Parameter | Symbol | Test conditions | Vcc | TA | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|---|
| OUTPUT | | | | | | | | |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = –100 μA | 1.65V to 5.5V | FULL | $V_{CC}$-0.1 | | | V |
| | | $I_{OH}$ = –4 mA | 1.65V | FULL | 1.2 | | | V |
| | | $I_{OH}$ = –8 mA | 2.3V | FULL | 1.9 | | | V |
| | | $I_{OH}$ = –16 mA | 3V | FULL | 2.4 | | | V |
| | | $I_{OH}$ = –24 mA | | FULL | 2.3 | | | V |
| | | $I_{OH}$ = –32 mA | 4.5V | FULL | 3.8 | | | V |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 100 μA | 1.65V to 5.5V | FULL | | | 0.1 | V |
| | | $I_{OL}$ = 4 mA | 1.65V | FULL | | | 0.45 | V |
| | | $I_{OL}$ = 8 mA | 2.3V | FULL | | | 0.3 | V |
| | | $I_{OL}$ = 16 mA | 3V | FULL | | | 0.4 | V |
| | | $I_{OL}$ = 24 mA | | FULL | | | 0.65 | V |
| | | $I_{OL}$ = 32 mA | 4.5V | FULL | | | 0.65 | V |
| Off-State Current | $I_{off}$ | $V_I$ or $V_O$ = 5.5 V | 0V | FULL | | | ±25 | μA |
| INPUT | | | | | | | | |
| Input Leakage Current | $I_I$ | $V_I$ = 5.5 V or GND | 0V to 5.5V | FULL | | | ±5 | μA |
| Input capacitance | $C_I$ | $V_I$ = $V_{CC}$ or GND | 3.3V | FULL | | 4 | | pF |

## Electrical specifications(continued)

Vcc=1.65V or 3.3V, FULL=–40°C to +125°C,Typical values are at TA = +25°C. (unless otherwise noted)

| Parameter | Symbol | Test conditions | Vcc | TA | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|---|
| DYNAMIC CHARACTERISTICS | | | | | | | | |
| Propagation Delay | $t_{pd}$ | $R_L$ = 1 MΩ, $C_L$ = 15 pF, $t_r/t_f$ = 2 ns | 1.65V to 1.95V | FULL | 1.9 | | 8 | ns |
| | | $R_L$ = 1 MΩ, $C_L$ = 15 pF, $t_r/t_f$ = 2 ns | 2.3V to 2.7V | FULL | 0.8 | | 4.4 | ns |
| | | $R_L$ = 1 MΩ, $C_L$ = 15 pF, $t_r/t_f$ = 2.5 ns | 3V to 3.6V | FULL | 0.8 | | 3.6 | ns |
| | | $R_L$ = 1 MΩ, $C_L$ = 15 pF, $t_r/t_f$ = 2.5 ns | 4.5V to 5.5V | FULL | 0.8 | | 3.4 | ns |
| | | $R_L$ = 1 kΩ, $C_L$ = 30 pF, $t_r/t_f$ = 2 ns | 1.65V to 1.95V | FULL | 2.8 | | 9 | ns |
| | | $R_L$ = 1 kΩ, $C_L$ = 30 pF, $t_r/t_f$ = 2 ns | 2.3V to 2.7V | FULL | 1.2 | | 6 | ns |
| | | $R_L$ = 500 Ω, $C_L$ = 50 pF, $t_r/t_f$ = 2.5 ns | 3V to 3.6V | FULL | 1 | | 5 | ns |
| | | $R_L$ = 500 Ω, $C_L$ = 50 pF, $t_r/t_f$ = 2.5 ns | 4.5V to 5.5V | FULL | 1 | | 4.5 | ns |
| POWER | | | | | | | | |
| Power Supply Range | $V_{CC}$ | | 1.65V to 5.5V | FULL | 1.65 | | 5.5 | V |
| Power Supply Current | $I_{CC}$ | $V_I$ = 5.5 V or GND, $I_O$ = 0 | 5.5V | FULL | | | 10 | μA |
| Delta Power Current | $\Delta I_{CC}$ | One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND | 3V to 5.5V | FULL | | | 500 | μA |
| Power dissipation capacitance | $C_{pd}$ | f = 10 MHz | 1.8V | +25°C | | 23 | | pF |
| | | f = 10 MHz | 2.5V | +25°C | | 23 | | pF |
| | | f = 10 MHz | 3.3V | +25°C | | 23 | | pF |
| | | f = 10 MHz | 5V | +25°C | | 25 | | pF |

## Typical Characteristics

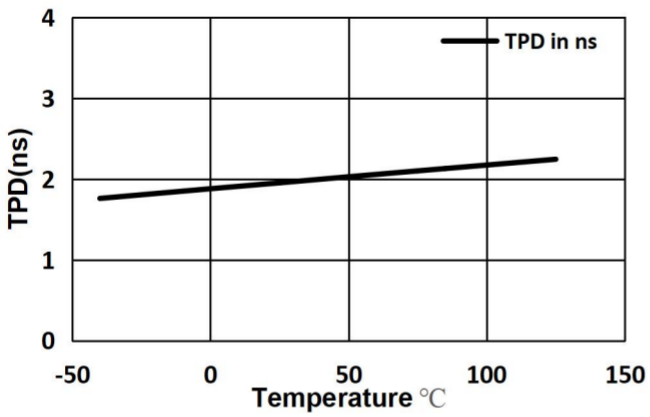



Fig. 8-1. TPD Across Temperature AT 3.3 V $V_{CC}$

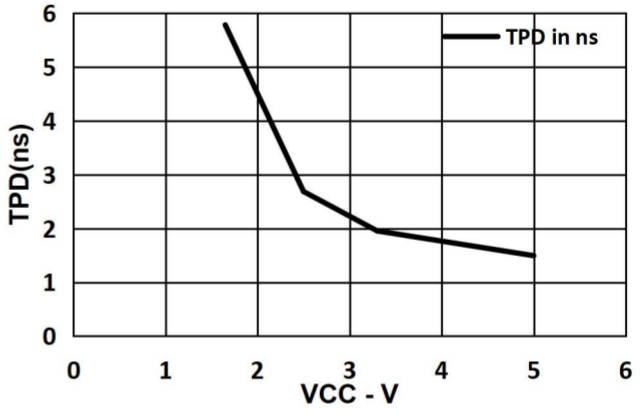


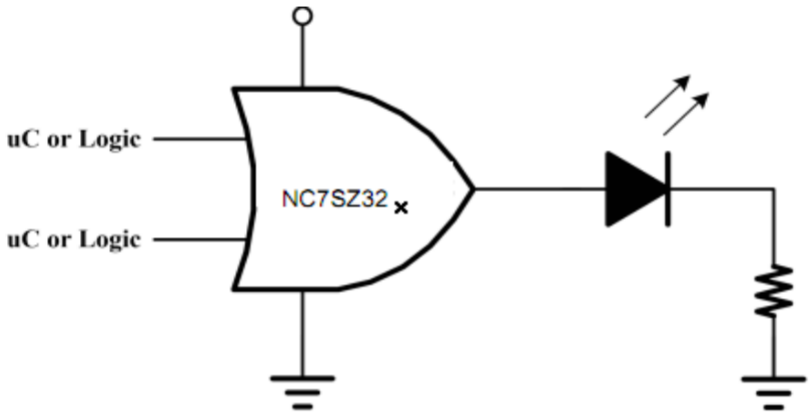

Fig. 8-2. TPD Across $V_{CC}$ at 25℃

## Detailed Description

The NC7SZ32 device contains one 2-input positive OR gate devices and performs the Boolean function $Y = A + B$ or $Y = \overline{\overline{A} \cdot \overline{B}}$. This device is fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The $I_{off}$ feature allows voltages on the inputs and outputs, when $V_{CC}$ is 0 V.

## Application Note

The NC7SZ32 is a high drive CMOS device that can be used for implement OR logic with a high output drive, such as an LED application. It can produce 24-mA of drive current at 3.3 V making it Ideal for driving multiple outputs and good for high speed applications up to 100 Mhz. The inputs are 5.5-V tolerant allowing translation down to $V_{CC}$.

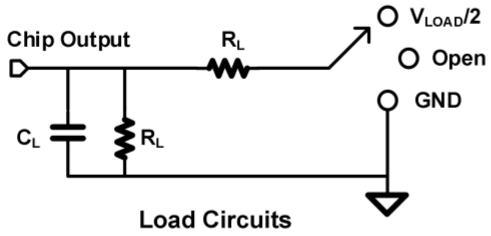



**Basic LED Driver**

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

Each VCC pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-pF capacitor is recommended. If there are multiple VCC pins, then a 0.01-pF or 0.022-pF capacitor is recommended for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1-pF and 1-pF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

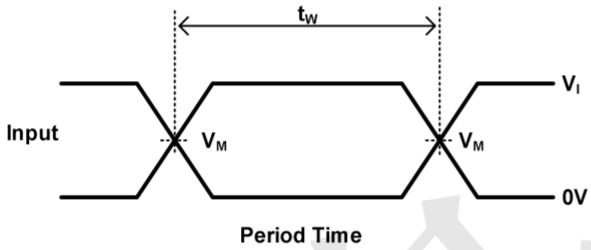
## Measurement Information



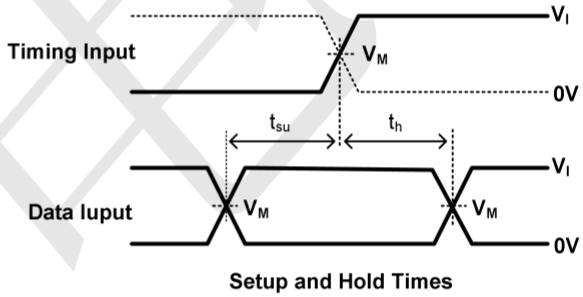

Load Circuits

| TEST | S1 |
|---|---|
| $T_{PHL}/T_{PLH}$ | OPEN |
| $T_{PLZ}/T_{PZL}$ | $V_{LOAD}$ |
| $T_{PHZ}/T_{PZH}$ | GND |

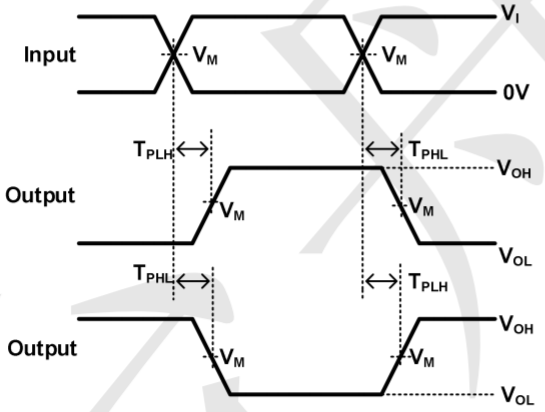
| $V_{CC}$ | INPUTS | | $V_M$ | $V_{LAOD}$ | $C_L$ | $R_L$ | $V_\Delta$ |
|---|---|---|---|---|---|---|---|
| | $V_I$ | $T_r/T_f$ | | | | | |
| 1.8V±0.15V | $V_{CC}$ | ≤2ns | $V_{CC}/2$ | $2\times V_{CC}$ | 15pF | 1MΩ | 0.15V |
| 2.5V±0.15V | $V_{CC}$ | ≤2ns | $V_{CC}/2$ | $2\times V_{CC}$ | 15pF | 1MΩ | 0.15V |
| 3.3V±0.15V | 3V | ≤2.5ns | 1.5V | 6V | 15pF | 1MΩ | 0.3V |
| 5V±0.15V | $V_{CC}$ | ≤2.5ns | $V_{CC}/2$ | $2\times V_{CC}$ | 15pF | 1MΩ | 0.3V |



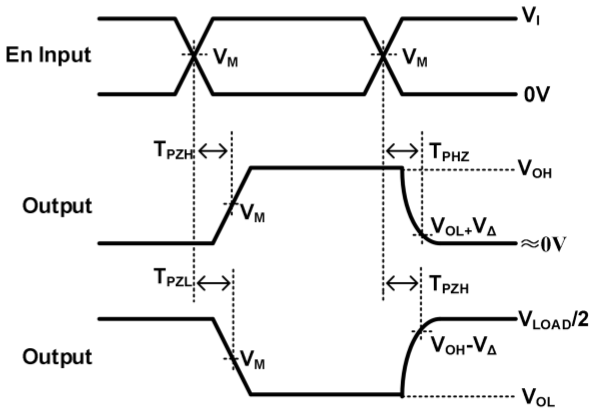

Period Time




Setup and Hold Times



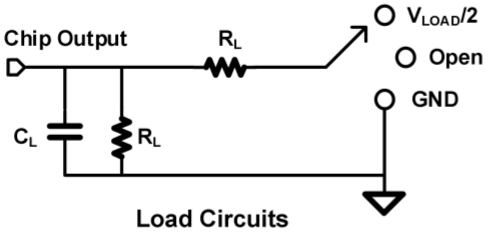

Propagation Delay
for Output and Inverted Output




Enable and Disable Times
Low-And High-Level Enabling

Notes: A. C includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR 10 MHz, Z = 50 .
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$ .
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$ .
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$ .
H. All parameters and waveforms are not applicable to all device.

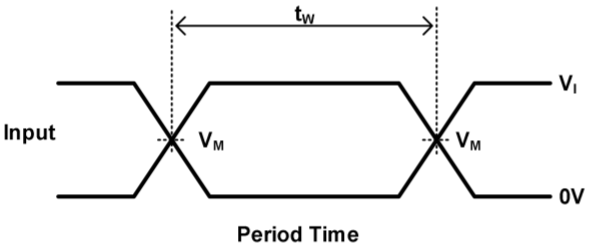
## Measurement Information (continued)



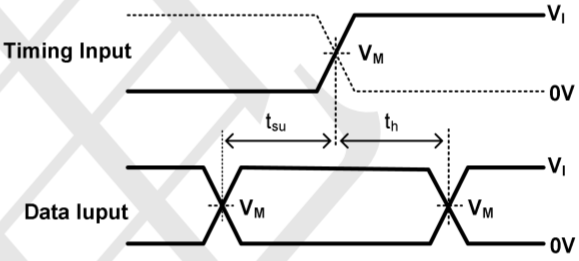

Load Circuits

| TEST | S1 |
|---|---|
| $T_{PHL}/T_{PLH}$ | OPEN |
| $T_{PLZ}/T_{PZL}$ | $V_{LOAD}$ |
| $T_{PHZ}/T_{PZH}$ | GND |

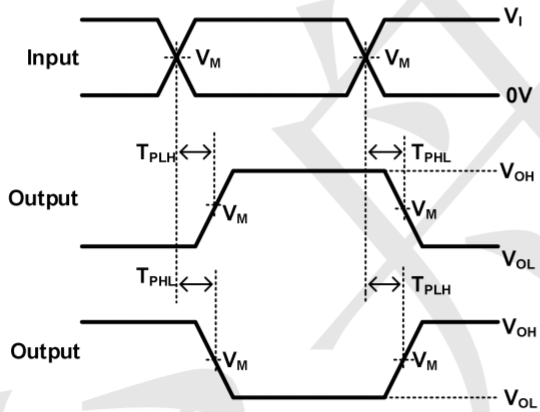
| $V_{CC}$ | INPUTS | | $V_M$ | $V_{LAOD}$ | $C_L$ | $R_L$ | $V_\Delta$ |
|---|---|---|---|---|---|---|---|
| | $V_I$ | $T_r/T_f$ | | | | | |
| 1.8V±0.15V | $V_{CC}$ | ≤2ns | $V_{CC}/2$ | $2\times V_{CC}$ | 30pF | 1kΩ | 0.15V |
| 2.5V±0.15V | $V_{CC}$ | ≤2ns | $V_{CC}/2$ | $2\times V_{CC}$ | 30pF | 500Ω | 0.15V |
| 3.3V±0.15V | 3V | ≤2.5ns | 1.5V | 6V | 50pF | 500Ω | 0.3V |
| 5V±0.15V | $V_{CC}$ | ≤2.5ns | $V_{CC}/2$ | $2\times V_{CC}$ | 50pF | 500Ω | 0.3V |



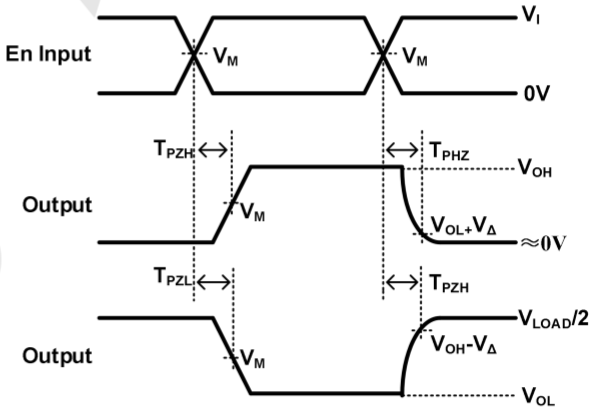

Period Time




Setup and Hold Times




Propagation Delay
for Output and Inverted Output

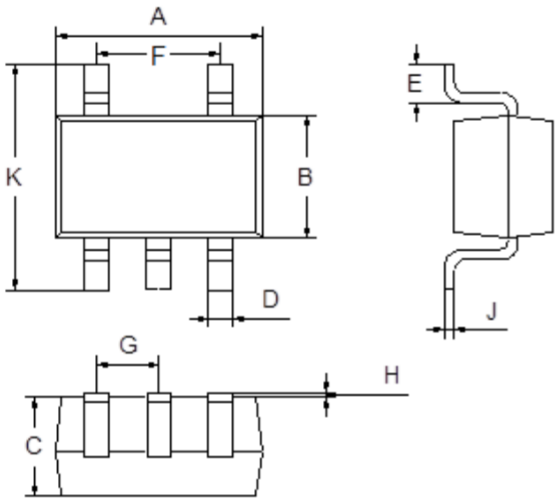



Enable and Disable Times
Low-And High-Level Enabling

Notes: A. C includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR 10 MHz, Z = 50 .
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$ .
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$ .
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$ .
H. All parameters and waveforms are not applicable to all device.

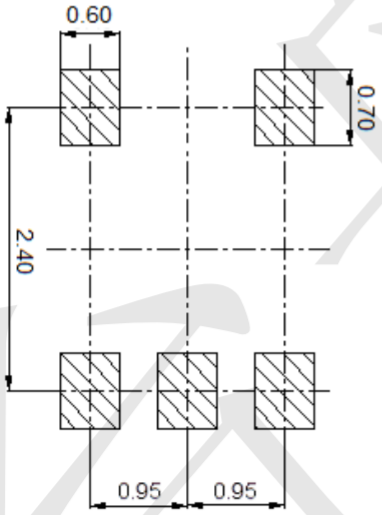
## Package Outline Dimensions (Unit: mm)

**SOT23-5**



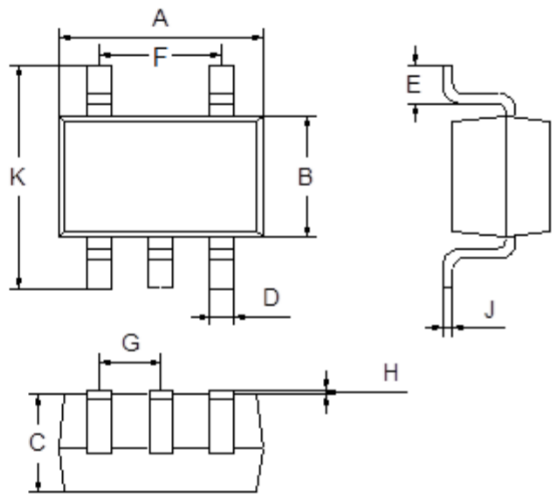

| Dimension | Min. | Max. |
|---|---|---|
| A | 2.80 | 3.00 |
| B | 1.50 | 1.70 |
| C | 1.00 | 1.20 |
| D | 0.35 | 0.45 |
| E | 0.35 | 0.55 |
| F | 1.80 | 2.00 |
| G | 0.90 | 1.00 |
| H | 0.02 | 0.10 |
| J | 0.10 | 0.20 |
| K | 2.60 | 3.00 |

## Mounting Pad Layout (Unit: mm)



## Package Outline Dimensions (Unit: mm)

**SOT353**




| Dimension | Min. | Max. |
|---|---|---|
| A | 2.00 | 2.20 |
| B | 1.15 | 1.35 |
| C | 0.85 | 1.05 |
| D | 0.15 | 0.35 |
| E | 0.25 | 0.40 |
| F | 1.20 | 1.40 |
| G | 0.60 | 0.70 |
| H | 0.02 | 0.10 |
| J | 0.05 | 0.15 |
| K | 2.20 | 2.40 |

## Mounting Pad Layout (Unit: mm)