GD25F128F-Automotive

DATASHEET

Contents

1 FEATURES

- 128M-bit Serial NOR Flash
  - 16M-Byte
  - 256 Bytes per programmable page
- Standard, Dual, Quad SPI, DTR
  - Standard SPI: SCLK, CS#, SI, SO, RESET#
  - Dual SPI: SCLK, CS#, IO0, IO1, RESET#
  - Quad SPI: SCLK, CS#, IO0, IO1, IO2, IO3, RESET#
  - SPI DTR (Double Transfer Rate) Read
- High Speed Clock Frequency
  - 166MHz for fast read
  - Dual I/O Data transfer up to 332Mbits/s
  - Quad I/O Data transfer up to 664Mbits/s
  - DTR Quad I/O Data transfer up to 832Mbits/s
- Software Write Protection
  - Write protect all/portion of memory via software
  - Top/Bottom Block protection
- Endurance and Data Retention
  - Minimum 100,000 Program/Erase Cycles
  - 20-year data retention typical
- On-chip ECC
  - 1-bit correction/2-bit detection every 8-Byte
- Allows XiP (eXecute In Place) Operation
  - High speed Read reduce overall XiP instruction fetch time
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- Fast Program/Erase Speed
  - Page Program time: 0.25ms typical
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- AEC-Q100 Qualified
- Temperature Ranges
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- Single Power Supply Voltage
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  - SOP8 208mil
  - SOP16 300mil
  - WSON8 (6x5mm)
  - WSON8 (8x6mm)
  - TFBGA-24ball (5x5 Ball Array)

2 GENERAL DESCRIPTIONS

The GD25F128F (128M-bit) Serial NOR flash supports the standard Serial Peripheral Interface (SPI), and the Dual/Quad SPI: Serial Clock, Chip Select, Serial Data I/O0 (SI), I/O1 (SO), I/O2, I/O3. The Dual I/O data is transferred with speed of 332Mbit/s, and the Quad I/O data is transferred with speed of 664Mbit/s. The DTR Quad I/O data is transferred with speed of 832Mbits/s.

CONNECTION DIAGRAM AND PIN DESCRIPTION

Figure 1 Connection Diagram for SOP8 package

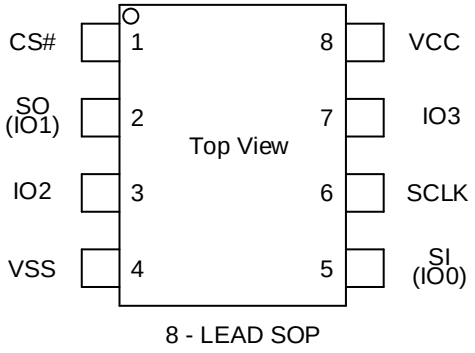


Table 1. Pin Description for SOP8 Package

Pin No.	Pin Name	I/O	Description
1	CS#	I	Chip Select Input
2	SO (IO1)	I/O	Data Output (Data Input Output 1)
3	IO2	I/O	Data Input Output 2
4	VSS		Ground
5	SI (IO0)	I/O	Data Input (Data Input Output 0)
6	SCLK	I	Serial Clock Input
7	IO3	I/O	Data Input Output 3
8	VCC		Power Supply

Note:

1. CS# must be driven high if chip is not selected. Please don't leave CS# floating any time after power is on.
2. If IO2/IO3 is unused, it must be driven high by the host, or an external pull-up resistor must be placed on the PCB in order to avoid allowing IO2/IO3 input to float.

Figure 2 Connection Diagram for SOP16 package

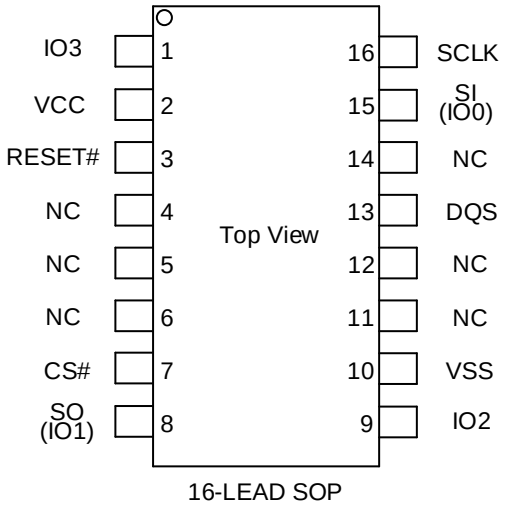


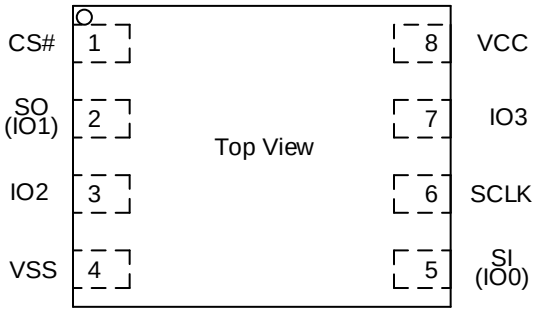
Table 2. Pin Description for SOP16 Package

Pin No.	Pin Name	I/O	Description
1	IO3	I/O	Data Input Output 3
2	VCC		Power Supply
3	RESET#	I	Reset Input
7	CS#	I	Chip Select Input
8	SO (IO1)	I/O	Data Output (Data Input Output 1)
9	IO2	I/O	Data Input Output 2
10	VSS		Ground
13	DQS	O	Data Strobe Signal Output
15	SI (IO0)	I/O	Data Input (Data Input Output 0)
16	SCLK	I	Serial Clock Input

Note:

1. CS# must be driven high if chip is not selected. Please don't leave CS# floating any time after power is on.
2. The NC pin is not connected to any internal signal. It is OK to connect it to the system ground (GND) or leave it floating.
3. The RESET# pin is a dedicated hardware reset pin regardless of device settings or operation states. If the hardware reset function is not used, this pin must be connected to VCC in the system.
4. If IO2/IO3 is unused, it must be driven high by the host, or an external pull-up resistor must be placed on the PCB in order to avoid allowing IO2/IO3 input to float.

Figure 3 Connection Diagram for WSON8 package



8 - LEAD WSON

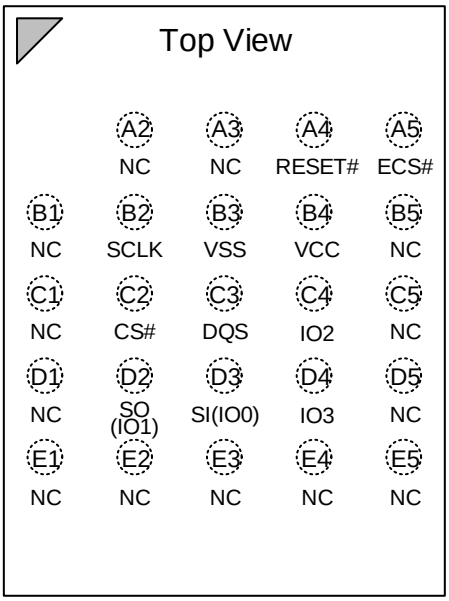
Table 3. Pin Description for WSON8 Package

Pin No.	Pin Name	I/O	Description
1	CS#	I	Chip Select Input
2	SO (IO1)	I/O	Data Output (Data Input Output 1)
3	IO2	I/O	Data Input Output 2
4	VSS		Ground
5	SI (IO0)	I/O	Data Input (Data Input Output 0)
6	SCLK	I	Serial Clock Input
7	IO3	I/O	Data Input Output 3
8	VCC		Power Supply

Note:

1. CS# must be driven high if chip is not selected. Please don't leave CS# floating any time after power is on.
2. If IO2/IO3 is unused, it must be driven high by the host, or an external pull-up resistor must be placed on the PCB in order to avoid allowing IO2/IO3 input to float.

Figure 4 Connection Diagram for TFBGA24 package



24-BALL TFBGA (5x5 ball array)

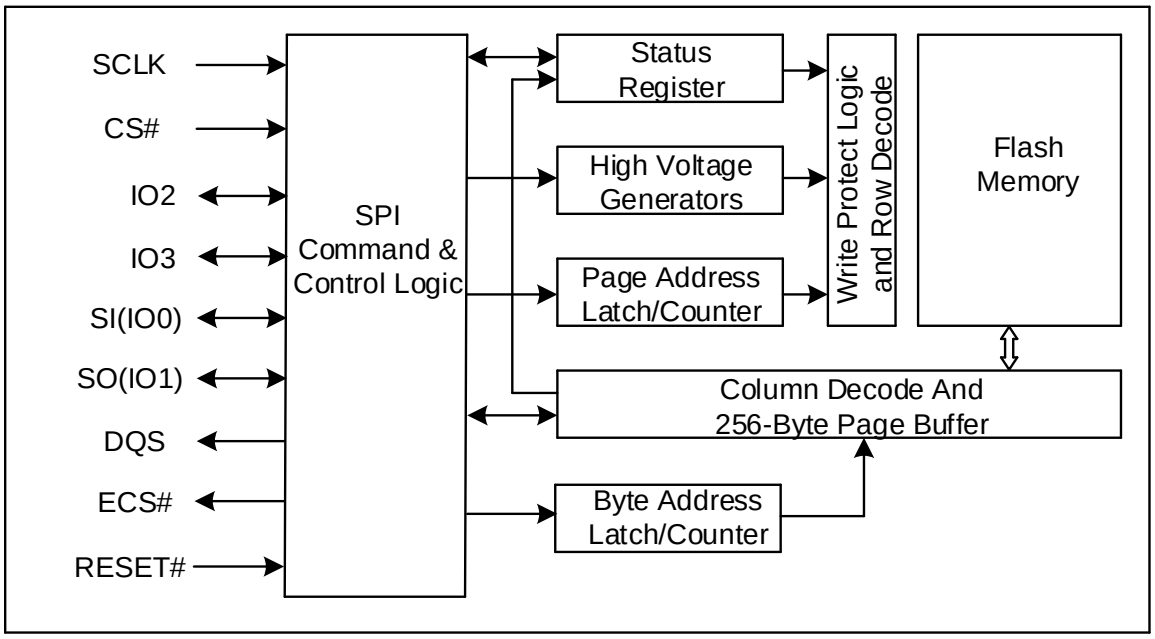
Table 4. Pin Description for TFBGA24 Package

Pin No.	Pin Name	I/O	Description
A4	RESET#	I	Reset Input
A5	ECS#	O	ECC Correction Signal
B2	SCLK	I	Serial Clock Input
B3	VSS		Ground
B4	VCC		Power Supply
C2	CS#	I	Chip Select Input
C3	DQS	O	Data Strobe Signal Output
C4	IO2	I/O	Data Input Output 2
D2	SO (IO1)	I/O	Data Output (Data Input Output 1)
D3	SI (IO0)	I/O	Data Input (Data Input Output 0)
D4	IO3	I/O	Data Input Output 3

Note:

1. CS# must be driven high if chip is not selected. Please don't leave CS# floating any time after power is on.
2. The NC ball is not connected to any internal signal. It is OK to connect it to the system ground (GND) or leave it floating.
3. The RESET# pin is a dedicated hardware reset pin regardless of device settings or operation states. If the hardware reset function is not used, this pin must be connected to VCC in the system.
4. If IO2/IO3 is unused, it must be driven high by the host, or an external pull-up resistor must be placed on the PCB in order to avoid allowing IO2/IO3 input to float.

BLOCK DIAGRAM



3 MEMORY ORGANIZATION

GD25F128F

Each device has	Each block has	Each sector has	Each page has	
16M	64/32K	4K	256	Bytes
64K	256/128	16	-	pages
4K	16/8	-	-	sectors
256/512	-	-	-	blocks

UNIFORM BLOCK SECTOR ARCHITECTURE

GD25F128F 64K Bytes Block Sector Architecture

Block	Sector	Address range	
255	4095	FFF000H	FFFFFFH
	.....	.....	.....
	4080	FF0000H	FF0FFFH
254	4079	FEF000H	FEFFFFH
	.....	.....	.....
	4064	FE0000H	FE0FFFH
.....	.....	.....	.....
	.....	.....	.....
	.....	.....	.....
.....	.....	.....	.....
	.....	.....	.....
	.....	.....	.....
2	47	02F000H	02FFFFH
	.....	.....	.....
	32	020000H	020FFFH
1	31	01F000H	01FFFFH
	.....	.....	.....
	16	010000H	010FFFH
0	15	00F000H	00FFFFH
	.....	.....	.....
	0	000000H	000FFFH

4 DEVICE OPERATIONS

4.1 SPI Mode

Standard SPI

The GD25F128F features a serial peripheral interface on 4 signals bus: Serial Clock (SCLK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO). Both SPI bus mode 0 and 3 are supported. Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK.

Dual SPI

The GD25F128F supports Dual SPI operation when using the “Dual Output Fast Read” and “Dual I/O Fast Read” (3Bh and BBh) commands. These commands allow data to be transferred to or from the device at twice the rate of the standard SPI. When using the Dual SPI commands, the SI and SO pins become bidirectional I/O pins: IO0 and IO1.

Quad SPI

The GD25F128F supports Quad SPI operation when using the “Quad Output Fast Read”, “Quad I/O Fast Read” (6Bh, EBh) commands. These commands allow data to be transferred to or from the device at four times the rate of the standard SPI. When using the Quad SPI commands, the SI and SO pins become bidirectional I/O pins: IO0 and IO1, in addition to IO2 and IO3 pins. For GD25F128F, the QE bit is set to 1 as default and cannot be changed.

DTR Quad SPI

The GD25F128F supports DTR Quad SPI operation when using the “DTR Quad I/O Fast Read” (EDh) command. This command allows data to be transferred to or from the device at eight times the rate of the standard SPI, and data output will be latched on both rising and falling edges of the serial clock. When using the DTR Quad SPI command, the SI and SO pins become bidirectional I/O pins: IO0 and IO1, in addition to IO2 and IO3 pins. For GD25F128F, the QE bit is set to 1 as default and cannot be changed.

4.2 ECC Function

The ECC Correction Signal pin is provided to the system hardware designers to determine the ECC status during any Read operation. When the internal ECC engine is disabled (ECC=0 in Status Register), the ECS# pin is also disabled. When ECC is enabled (ECC=1 in Status Register), the ECS# pin will be pulled low during any 8-Byte Read data output period in which an ECC event has occurred. Depending on the ECS bit setting in the Extended Register, ECS# pin can be used to represent either SEC (Single Error Correction) or DED (Double Error Detection). Interrupt Output pin is an Open-Drain connection.

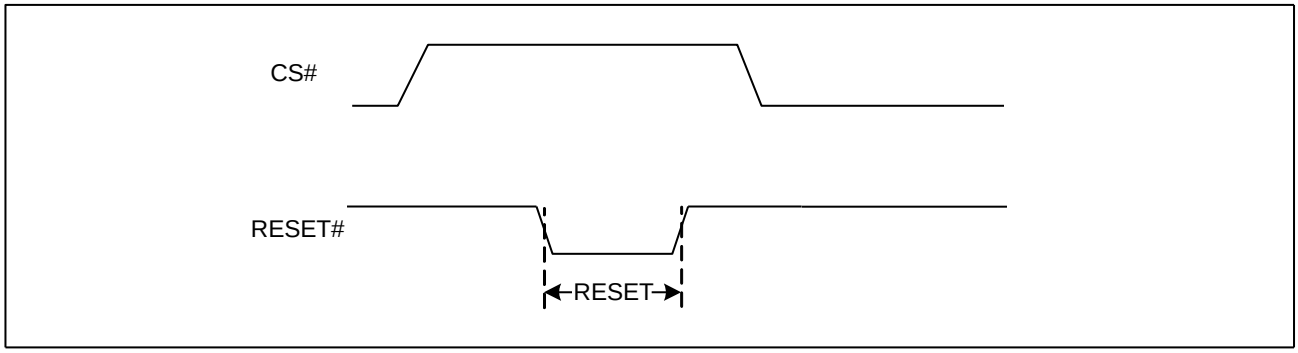
4.3 RESET Function

The RESET# pin goes low for a minimum period of tRLRH (1μs) will reset the flash. After reset cycle, the flash is at the following states:

-Standby mode

-All the volatile bits will return to the default status as power on.

Figure 5 RESET Condition



5 DATA PROTECTION

The GD25F128F provide the following data protection methods:

- Write Enable (WREN) command: The WREN command is set the Write Enable Latch bit (WEL). The WEL bit will return to reset by the following situation:
  -Power-Up / Hardware Reset / Software Reset (66h+99h)
  -Write Disable (WRDI)
  -Write Status Register (WRSR)
  -Page Program (PP)
  -Sector Erase (SE) / Block Erase (BE) / Chip Erase (CE)
- Software Protection Mode: The Block Protect bits (BP4-BP0) define the section of the memory array that can be read but not changed.
- Deep Power-Down Mode: In Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down Mode command and Software Reset (66h+99h).
- Write Inhibit Voltage (VWI): Device would reset automatically when VCC is below a certain threshold VWI.

Table 5. GD25F128F Protected area size

Status Register Content					Memory Content			
BP4	BP3	BP2	BP1	BP0	Blocks	Addresses	Density	Portion
X	0	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	255	00FF0000h-00FFFFFFh	64KB	Upper 1/256
0	0	0	1	0	254 to 255	00FE0000h-00FFFFFFh	128KB	Upper 1/128
0	0	0	1	1	252 to 255	00FC0000h-00FFFFFFh	256KB	Upper 1/64
0	0	1	0	0	248 to 255	00F80000h-00FFFFFFh	512KB	Upper 1/32
0	0	1	0	1	240 to 255	00F00000h-00FFFFFFh	1MB	Upper 1/16
0	0	1	1	0	224 to 255	00E00000h-00FFFFFFh	2MB	Upper 1/8
0	0	1	1	1	192 to 255	00C00000h-00FFFFFFh	4MB	Upper 1/4
0	1	0	0	0	128 to 255	00800000h-00FFFFFFh	8MB	Upper 1/2
1	0	0	0	1	0	00000000h-0000FFFFh	64KB	Lower 1/256
1	0	0	1	0	0 to 1	00000000h-0001FFFFh	128KB	Lower 1/128
1	0	0	1	1	0 to 3	00000000h-0003FFFFh	256KB	Lower 1/64
1	0	1	0	0	0 to 7	00000000h-0007FFFFh	512KB	Lower 1/32
1	0	1	0	1	0 to 15	00000000h-000FFFFFh	1MB	Lower 1/16
1	0	1	1	0	0 to 31	00000000h-001FFFFFh	2MB	Lower 1/8
1	0	1	1	1	0 to 63	00000000h-003FFFFFh	4MB	Lower 1/4
1	1	0	0	0	0 to 127	00000000h-007FFFFFh	8MB	Lower 1/2
X	1	0	0	1	ALL	00000000h-00FFFFFFh	16MB	ALL
X	1	0	1	X	ALL	00000000h-00FFFFFFh	16MB	ALL
X	1	1	X	X	ALL	00000000h-00FFFFFFh	16MB	ALL

6 ECC OPERATION

6.1 ECC (Error Checking and Correcting)

Error Correction Codes (ECC) is a commonly used technique in non-volatile memory to reduce the device Bit Error Rate (BER) during the device operation life and improve device reliability. To achieve error detection and correction, redundancy data must be added to store the ECC calculation results for a given length of data. In GD25F128F, every aligned 8- Byte data (A[2:0] = 0, 0, 0), stored in the memory array will be checked by the internal ECC engine using SEC-DED (Single Error Correction - Double Error Detection) Hsiao Codes algorithm. With 8-Byte ECC data granularity, ECC calculation latency time can be minimized and highest level of data integrity can be preserved.

The default value of all memory data is FFH (Erased) when the device is shipped from the factory. A “Page Program (02h)” or “Quad Page Program (32h)” command can be used to program the user data into the memory array. When ECC is enabled, ECC calculation will be performed during the internal programming operation and the results are stored in the redundancy or spare area of the memory array. It is necessary to program every page in aligned 8-Byte granularity, so that ECC engine can store and preserve the correct ECC information. Multiple programming attempts to previously programmed 8-Byte aligned memory will disable the internal ECC engine. Once the 8-Byte aligned memory chunk internal ECC is disabled, read memory access will only be directed to the memory array without error correction. An Erase is required to recover back ECC enable of these affected 8-Byte aligned memories.

A technique previously known as “Incremental Byte/Bit Programming to the same Byte location” can be used for GD25F128F when ECC is enabled; however, the 8-Byte aligned memory locations that were attempted with multiple programming will have ECC disabled and read operation will only access the memory array without ECC.

A Read operation can start from any Byte address and continue through the entire memory array, so it is not necessary to align the 8-Byte granularity boundary address to start a Read command. During data read operations, the internal ECC engine will check the ECC results stored in the spare area and apply necessary error correction or error detection to the main array data being read out. It is necessary to check the ECC Status Bits (SEC and DED) in the Extended Address Register after every Read operation to see if the data read out contains error(s) or not.

Additional hardware monitoring of the ECC status can also be used to observe the ECC status in real time during any data output. When configured, the ECS# (ECC Correction Signal) pin will be pulled low during any aligned 8-Byte data output if it contains SEC or DED.

The SEC and DED bits can be reset through any of the following situations:

- Sending a new Read Command
- Issuing Software Reset Command
- Hardware Reset
- Power-up cycle

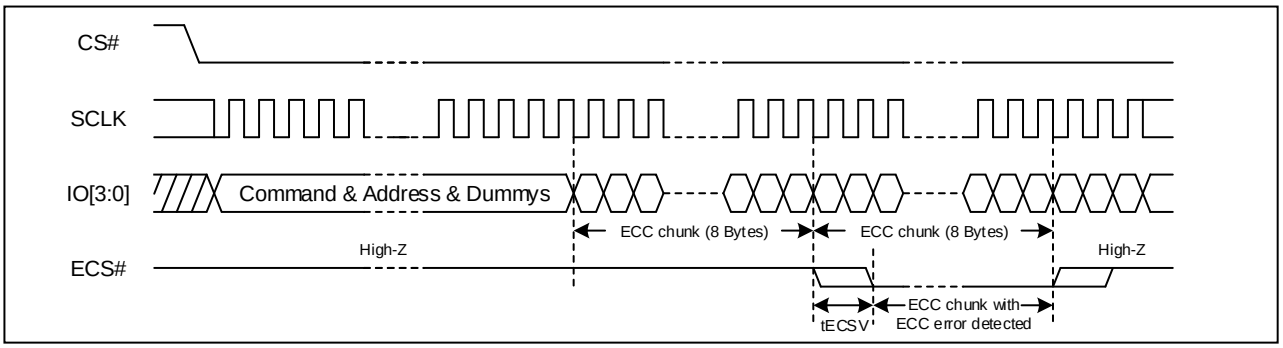
When an address range is erased, the target memory and the stored ECC data is reverted to its erased FFH state.

6.2 ECS# (Error Corrected Signal) Pin

The ECS# pin is a real time hardware signal to feedback the ECC correction status. The ECS# pin is designed as an open drain structure and a pull-up resistor (Rp) is required. In normal situation, the ECS# is kept on High-Z state. Once error correction begins, the ECS# pin will pull low during the whole ECC chunk unit after a duration of tECSV delay timing.

The ECS# (ECC Correction Signal) pin will be pulled low during any aligned 8-Byte data output if it contains SEC (Single Error Correction) event.

Figure 6. ECS# Timing



7 REGISTERS

7.1 Status Register

Table 6. Status Register-SR No.1

No.	Name	Description	Note
S7	Reserved	Reserved	Reserved
S6	BP4	Block Protect Bit	Non-volatile writable
S5	BP3	Block Protect Bit	Non-volatile writable
S4	BP2	Block Protect Bit	Non-volatile writable
S3	BP1	Block Protect Bit	Non-volatile writable
S2	BP0	Block Protect Bit	Non-volatile writable
S1	WEL	Write Enable Latch	Volatile, read only
S0	WIP	Erase/Write In Progress	Volatile, read only

Table 7. Status Register-SR No.2

No.	Name	Description	Note
S15	SUS1	Erase Suspend Bit	Volatile, read only
S14	ECC	ECC Enable Bit	Non-volatile writable
S13	LB3	Security Register Lock Bit	Non-volatile writable (OTP)
S12	LB2	Security Register Lock Bit	Non-volatile writable (OTP)
S11	LB1	Security Register Lock Bit	Non-volatile writable (OTP)
S10	SUS2	Program Suspend Bit	Volatile, read only
S9	QE	Quad Enable Bit	QE = 1 permanently
S8	Reserved	Reserved	Reserved

Table 8. Status Register-SR No.3

No.	Name	Description	Note
S23	Reserved	Reserved	Reserved
S22	DRV1	Output Driver Strength Bit	Non-volatile writable
S21	DRV0	Output Driver Strength Bit	Non-volatile writable
S20	Reserved	Reserved	Reserved
S19	EE	Erase Error Bit	Volatile, read only
S18	PE	Program Error Bit	Volatile, read only
S17	DC1	Dummy Configuration Bit	Non-volatile writable
S16	DC0	Dummy Configuration Bit	Non-volatile writable

The status and control bits of the Status Register are as follows:

WIP bit

The Write in Progress (WIP) bit indicates whether the memory is busy in program/erase/write status register progress. When WIP bit sets to 1, means the device is busy in program/erase/write status register progress, when WIP bit sets 0, means the device is not in program/erase/write status register progress.

WEL bit

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase command is accepted.

BP4, BP3, BP2, BP1, BP0 bits

The Block Protect (BP4, BP3, BP2, BP1, and BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase commands. These bits are written with the Write Status Register (WRSR) command. When the Block Protect (BP4, BP3, BP2, BP1, BP0) bits are set to 1, the relevant memory area (as defined in Table 4) becomes protected against Page Program (PP), Sector Erase (SE), Block Erase (BE), and Chip Erase (CE) commands.

QE bit

The Quad Enable (QE) bit is a non-volatile bit in the Status Register that allows Quad operation. The default value of QE bit is 1 and it cannot be changed, so that the IO2 and IO3 pins are enabled all the time.

LB3, LB2, LB1 bits

The LB3, LB2 and LB1 bits are non-volatile One Time Program (OTP) bits in Status Register (S13, S12 and S11) that provide the write protect control and status to the Security Registers. The default state of LB3, LB2 and LB1 bits are 0, the security registers are unlocked. The LB3, LB2 and LB1 bits can be set to 1 individually using the Write Register instruction. The LB3, LB2 and LB1 bits are One Time Programmable, once they are set to 1, the Security Registers will become read-only permanently.

ECC Enable bit

The on chip ECC engine can be enabled or disabled by the ECC Enable bit. When ECC=1, ECC function is enabled for all Program and Read operations to ensure data integrity and improve device reliability. Aligned 8-Byte granularity is required for Program operations, but not for Read operations.

When ECC is enabled, it is required to program minimum one or multiple aligned 8-Byte granularities. Every aligned 8-Byte granularity should only be programmed once before Erase to ensure correct ECC operations.

The default value of ECC bit is 1, ECC is enabled.

SUS1, SUS2 bits

The SUS1 and SUS2 bits are read only bits in the status register (S15 and S10) that are set to 1 after executing an Erase/Program Suspend (75h) command (The Erase Suspend will set the SUS1 bit to 1, and the Program Suspend will set the SUS2 bit to 1). The SUS1 and SUS2 bits are cleared to 0 by Erase/Program Resume (7Ah) command, hardware Reset, software reset (66h+99h) command, as well as a power-down, power-up cycle.

DC1, DC0 bits

The Dummy Configuration (DC) bits are non-volatile, which select the number of dummy cycles between the end of address and the start of read data output. Dummy cycles provide additional latency that is needed to complete the initial read access of the flash array before data can be returned to the host system. Some read commands require additional dummy cycles as the SCLK frequency increases.

The following dummy cycle tables provide different dummy cycle settings that are configured.

Command	DC1, DC0	Dummy Cycles	Freq.(MHz)
BBh	00	4	104
	01	8	166
	other	Reserved	Reserved
EBh	00	6	104
	01	10	166
	other	Reserved	Reserved
EDh	00	8	104
	10	6	70
	other	Reserved	Reserved

PE bit

The Program Error (PE) bit is a read-only bit that indicates a program failure. It will also be set when the user attempts to program a protected array sector or access the locked OTP space. PE is cleared to "0" after program operation resumes.

EE bit

The Erase Error (EE) bit is a read-only bit that indicates an erase failure. It will also be set when the user attempts to erase a protected array sector or access the locked OTP space. EE is cleared to "0" after erase operation resumes

DRV1, DRV0 bits

The DRV1 and DRV0 bits are used to determine the output driver strength for the Read operations.

Table 9. Driver Strength for Read Operations

DRV1, DRV0	Driver Strength
00	100%
01	75% (default)
10	50%
11	25%

Reserved bit

It is recommended to set the value of the reserved bit as “0”.

7.2 Extended Address Register

Table 10. Extended Address Register

No.	Name	Description	Note
EA7	SEC	Single Error Correction bit	Volatile, read only
EA6	DED	Double Error Detection bit	Volatile, read only
EA5	Reserved	Reserved	Reserved
EA4	Reserved	Reserved	Reserved
EA3	DLP	Data Learning Pattern Enable bit	Volatile writable
EA2	ECS	ECC Correction Signal bit	Volatile writable
EA1	Reserved	Reserved	Reserved
EA0	Reserved	Reserved	Reserved

The bits of the Extended Address Register are as follows:

DLP bit

The DLP bit is Data Learning Pattern Enable bit, which is volatile writable by 56h command. For Quad DTR Read commands, a pre-defined “Data Learning Pattern” can be used by the flash memory controller to determine the flash data output timing on 4 I/O pins. When DLP=1, during the last 4 dummy clocks just prior to the data output, the flash will output “00110100” Data Learning Pattern sequence on each of the 4 I/O pins. During this period, controller can fine tune the data latching timing for each I/O pins to achieve optimum system performance. DLP=0 will disable the Data Learning Pattern output. The Data Learning Pattern can also be defined by a “Write Data Learning Pattern (4Ah)” command followed by 8-bit user-defined pattern. The user defined pattern is volatile. After device power cycle, the Data Learning Pattern will return to its “00110100” default value.

Reserved bit

It is recommended to set the value of the reserved bit as “0”.

ECS bit

The ECS bit is ECC Correction Signal bit, which is volatile writable by 56h command. The hardware ECS# Pin is used by the system to detect ECC events during Read operations when ECC is enabled (ECC=1). When ECS=0, the ECS# Pin will be pulled low during the aligned 8-Byte data output period if there is a SEC (Single Error Correction) or DED (Double Error Detection) event within the 8-Byte ECC granularity. When ECS=1, the ECS# Pin will be pulled low for DED (Double Error Detection) events. When ECC is disabled (ECC=0), the ECS bit value is ignored and ESC# Pin is disabled.

SEC, DED bits

SEC (Single Error Correction) and DED (Double Error Detection) Status Bits are used to show the ECC results for the last Read operation. SEC and DED bits will be cleared to 0 once the device accepts a new Read command.

SEC, DED	Definitions
0, 0	No ECC events in all aligned 8-Byte granularities
1, 0	SEC events in single or multiple 8-Byte granularities, and the data is OK to use. (Unless it contains more than one odd bit errors in 8-Byte granularity)
0, 1	DED events in single or multiple 8-Byte granularities, and the data contains 2 or more even bit errors.
1, 1	Both SEC & DED occurred in multiple 8-Byte granularities, and the data contains 2 or more bit errors.

8 COMMAND DESCRIPTIONS

All commands, addresses and data are shifted in and out of the device, beginning with the most significant bit on the first rising edge of SCLK after CS# is driven low. Then, the one-byte command code must be shifted in to the device, with most significant bit first on SI, and each bit is latched on the rising edges of SCLK.

Every command sequence starts with a one-byte command code. Depending on the command, this might be followed by address bytes, or by data bytes, or by both or none. CS# must be driven high after the last bit of the command sequence has been completed. For the command of Read, Fast Read, Read Status Register or Release from Deep Power-Down, and Read Device ID, the shifted-in command sequence is followed by a data-out sequence. All read instruction can be completed after any bit of the data-out sequence is being shifted out, and then CS# must be driven high to return to deselected status.

For the command of Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write Enable, Write Disable or Deep Power-Down command, CS# must be driven high exactly at a byte boundary, otherwise the command is rejected, and is not executed. That is CS# must be driven high when the number of clock pulses after CS# being driven low is an exact multiple of eight. For Page Program, if at any time the input byte is not a full byte, nothing will happen and WEL will not be reset.

Table 11. Commands

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9
Write Enable	06h								
Write Disable	04h								
Read Status Register-1	05h	(S7-S0)	(cont.)						
Read Status Register-2	35h	(S15-S8)	(cont.)						
Read Status Register-3	15h	(S23-S16)	(cont.)						
Write Status Register-1	01h	S7-S0							
Write Status Register-2	31h	S15-S8							
Write Status Register-3	11h	S23-S16							
Read Extended Addr. Register	C8h	(EA7-EA0)							
Write Extended Addr. Register (Except Address bits)	56h	EA7-EA0							
Volatile SR write Enable	50h								
Read Data	03h	A23-A16	A15-A8	A7-A0	(D7-D0)	(cont.)			
Fast Read	0Bh	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(cont.)		
Dual Output Fast Read	3Bh	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)(1)	(cont.)		
Quad Output Fast Read	6Bh	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)(2)	(cont.)		

Dual I/O Fast Read	BBh	A23-A16[3]	A15-A8[3]	A7-A0[3]	M7-M0[4]	(D7-D0)[1]	(cont.)		
Quad I/O Fast Read	EBh	A23-A16[5]	A15-A8[5]	A7-A0[5]	M7-M0[6]	dummy	dummy	(D7-D0)[2]	(cont.)
DTR Quad I/O Fast Read	EDh	A23-A16[5]	A15-A8[5]	A7-A0[5]	M7-M0[6]	n-CLK dummy	(D7-D0)[2]	(cont.)	
Set Burst with Wrap	77h	dummy[7]	dummy[7]	dummy[7]	W7-W0[7]				
Write Data Learning Pattern	4Ah	P7-P0							
Page Program	02h	A23-A16	A15-A8	A7-A0	D7-D0	Next Byte			
Quad Page Program	32h	A23-A16	A15-A8	A7-A0	D7-D0[8]	Next Byte			
Sector Erase	20h	A23-A16	A15-A8	A7-A0					
Block Erase (32K)	52h	A23-A16	A15-A8	A7-A0					
Block Erase (64K)	D8h	A23-A16	A15-A8	A7-A0					
Chip Erase	C7/60h								
Read Manufacturer/ Device ID	90h	00H	00H	00H	(MID7-MID0)	(ID7-ID0)	(cont.)		
Read Identification	9Fh	(MID7-MID0)	(ID15-ID8)	(ID7-ID0)	(cont.)				
Read Unique ID	4Bh	00H	00H	00H	dummy	(UID7-UID0)	(cont.)		
Erase Security Registers[9]	44h	A23-A16	A15-A8	A7-A0					
Program Security Registers[9]	42h	A23-A16	A15-A8	A7-A0	D7-D0	Next Byte			
Read Security Registers[9]	48h	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(cont.)		
Enable Reset	66h								
Reset	99h								
Program/Erase Suspend	75h								
Program/Erase Resume	7Ah								
Deep Power-Down	B9h								
Release From Deep Power-Down	ABh								
Release From Deep Power-Down and Read Device ID	ABh	dummy	dummy	dummy	(ID7-ID0)	(cont.)			
Read Serial Flash Discoverable Parameter	5Ah	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(cont.)		

Note:

1. Dual Output data

IO0 = (D6, D4, D2, D0)

IO1 = (D7, D5, D3, D1)

2. Quad Output Data

IO0 = (D4, D0, …)

IO1 = (D5, D1, …)

IO2 = (D6, D2, …)

IO3 = (D7, D3, …)

3. Dual Input Address

IO0 = A22, A20, A18, A16, A14, A12, A10, A8 A6, A4, A2, A0

IO1 = A23, A21, A19, A17, A15, A13, A11, A9 A7, A5, A3, A1

4. Dual Input Mode bit

IO0 = M6, M4, M2, M0

IO1 = M7, M5, M3, M1

5. Quad Input Address

IO0 = A20, A16, A12, A8, A4, A0

IO1 = A21, A17, A13, A9, A5, A1

IO2 = A22, A18, A14, A10, A6, A2

IO3 = A23, A19, A15, A11, A7, A3

6. Quad Input Mode bit

IO0 = M4, M0

IO1 = M5, M1

IO2 = M6, M2

IO3 = M7, M3

7. Dummy bits and Wrap Bits

IO0 = (x, x, x, x, x, x, W4, x)

IO1 = (x, x, x, x, x, x, W5, x)

IO2 = (x, x, x, x, x, x, W6, x)

IO3 = (x, x, x, x, x, x, x, x)

8. Quad Output Data

IO0 = D4, D0, …

IO1 = D5, D1, …

IO2 = D6, D2, …

IO3 = D7, D3, …

9. Security Registers Address

Security Register: A23-A16=00H, A15-A12=1H, A11 = 0b, A10-A0= Byte Address;

Security Register: A23-A16=00H, A15-A12=2H, A11 = 0b, A10-A0= Byte Address;

Security Register: A23-A16=00H, A15-A12=3H, A11 = 0b, A10-A0= Byte Address;

TABLE OF ID DEFINITIONS

GD25F128F

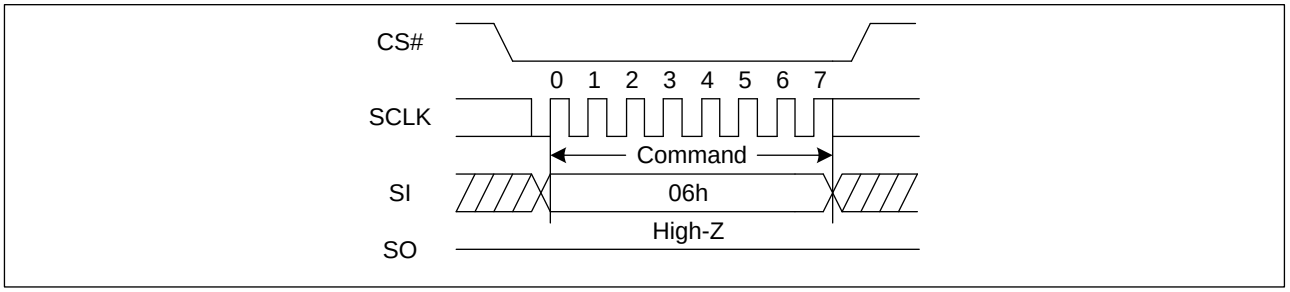
Operation Code	MID7-MID0	ID15-ID8	ID7-ID0
9Fh	C8	43	18
90h	C8		17
ABh			17

8.1 Write Enable (WREN) (06h)

The Write Enable (WREN) command is for setting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Quad Page Program (QPP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE), Write Status Register (WRSR) and Erase/Program Security Registers command.

The Write Enable (WREN) command sequence: CS# goes low → sending the Write Enable command → CS# goes high.

Figure 7. Write Enable Sequence Diagram



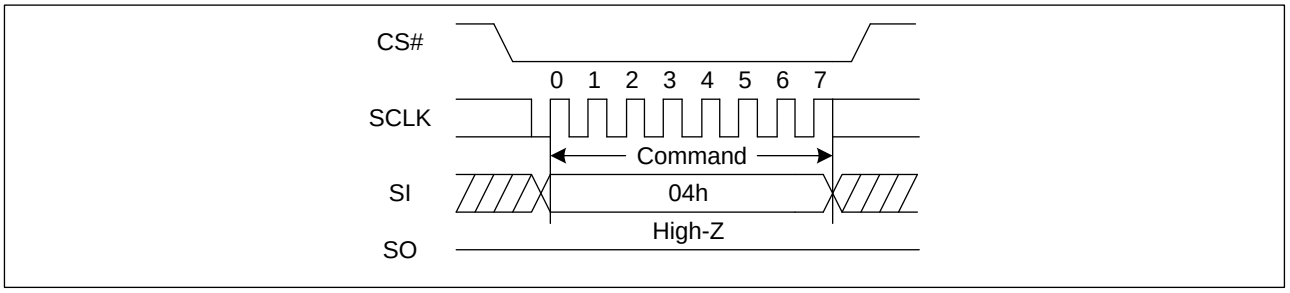
8.2 Write Disable (WRDI) (04h)

The Write Disable command is for resetting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit may be set to 0 by issuing the Write Disable (WRDI) command to disable Page Program (PP), Quad Page Program (QPP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE), Write Status Register (WRSR), that require WEL be set to 1 for execution. The WRDI command can be used by the user to protect memory areas against inadvertent writes that can possibly corrupt the contents of the memory. The WRDI command is ignored during an embedded operation while WIP bit =1.

The WEL bit is reset by following condition: Write Disable command (WRDI), Power-up, and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase and Chip Erase commands.

The Write Disable command sequence: CS# goes low →Sending the Write Disable command →CS# goes high.

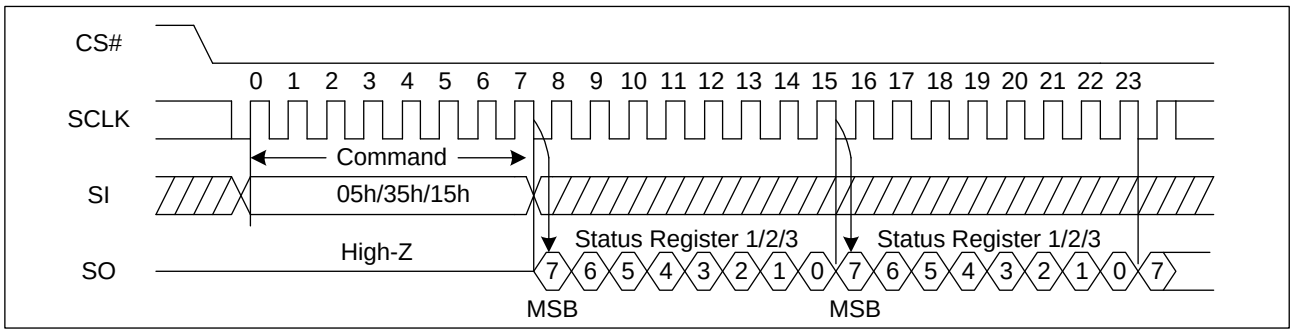
Figure 8. Write Disable Sequence Diagram



8.3 Read Status Register (RDSR) (05h/35h/15h)

The Read Status Register (RDSR) command is for reading the Status Register. The Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write in Progress (WIP) bit before sending a new command to the device. It is also possible to read the Status Register continuously. For command code of “05h” / “35h” / “15h”, the SO will output Status Register bits S7~S0 / S15~S8 / S23~S16.

Figure 9. Read Status Register Sequence Diagram



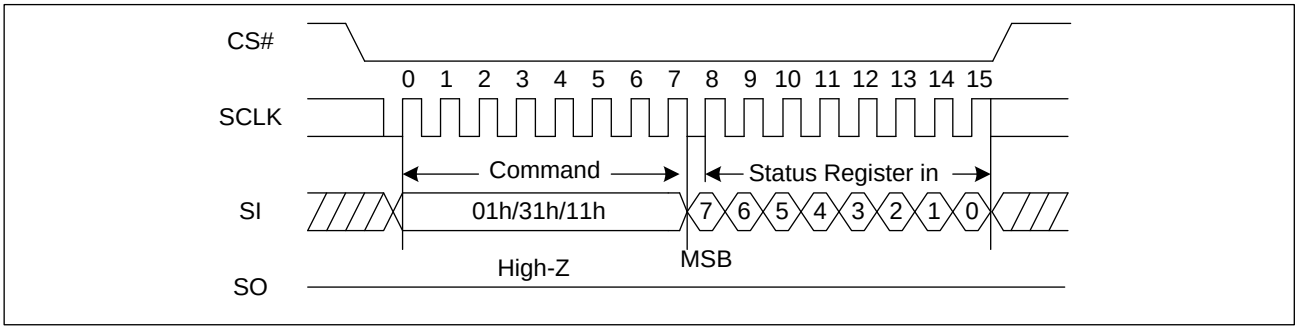
8.4 Write Status Register (WRSR) (01h/31h/11h)

The Write Status Register (WRSR) command allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) command must previously have been executed. After the Write Enable (WREN) command has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register (WRSR) command has no effect on S19, S18, S15, S10, S9, S1 and S0 of the Status Register. For command code of "01h" / "31h" / "11h", the Status Register bits S7~S0 / S15~S8 / S23~S16 would be written. CS# must be driven high after the eighth bit of the data byte has been latched in. Otherwise, the Write Status Register (WRSR) command is not executed. As soon as CS# is driven high, the self-timed Write Status Register cycle (whose duration is t_W) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register (WRSR) command allows the user to change the values of the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits, to define the size of the area that is to be treated as read-only.

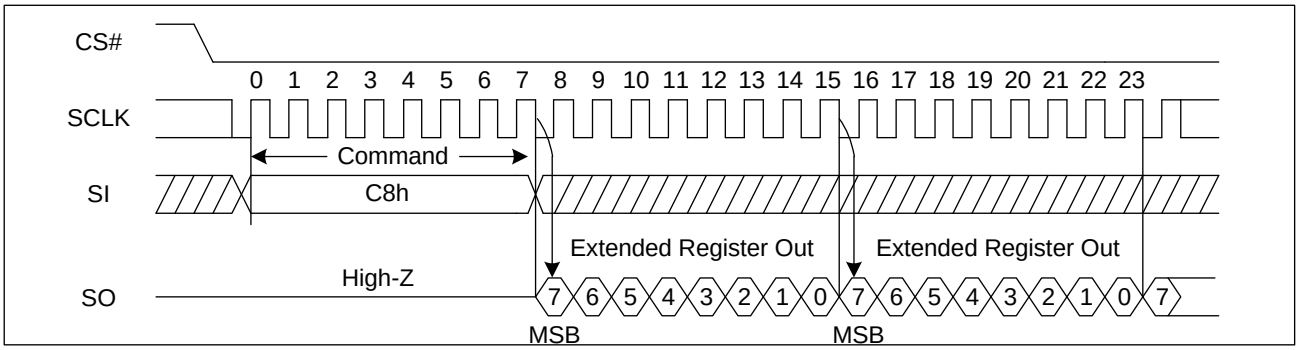
Figure 10. Write Status Register Sequence Diagram



8.5 Read Extended Register (C8h)

Extended Register contains ECC Status Bits, several device configuration bits. The Read Extended Register instruction is entered by driving CS# low and shifting the instruction code “C8h” into the SI pin on the rising edge of SCLK. The Extended Register bits are then shifted out on the SO pin at the falling edge of SCLK with most significant bit (MSB) first. When the device is in the 4-Byte Address Mode, the value of Address Bit is not ignored.

Figure 11 Read Extended Register Sequence Diagram

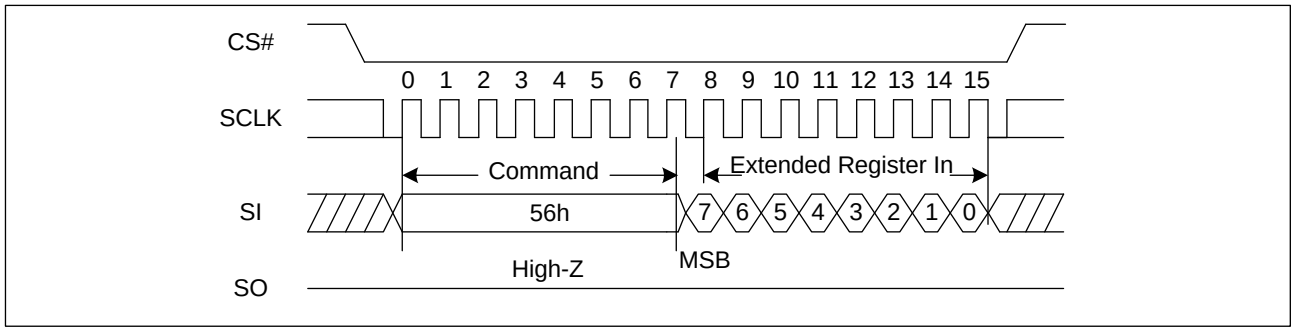


8.6 Write Extended Address Register (56h)

The Write Extended Address Register command could be executed no matter the Write Enable Latch (WEL) bit is 0 or 1. The Write Extended Address Register instruction is entered by driving CS# low, sending the instruction code “56h”, and then writing the Extended Address Register data Byte as illustrated in Figure 11.

Upon power up or the execution of a Software/Hardware Reset, the Extended Address Register bit values will be cleared to 0.

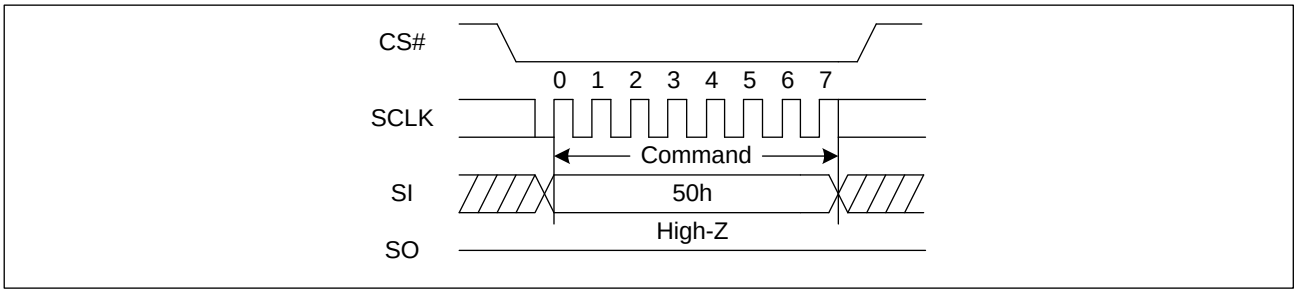
Figure 12 Write Extended Register Address Sequence Diagram



8.7 Write Enable for Volatile Status Register (50h)

The non-volatile Status Register bits can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. The Write Enable for Volatile Status Register command must be issued prior to a Write Status Register command and any other commands can’t be inserted between them. Otherwise, Write Enable for Volatile Status Register will be cleared. The Write Enable for Volatile Status Register command will not set the Write Enable Latch bit, it is only valid for the Write Status Register command to change the volatile Status Register bit values.

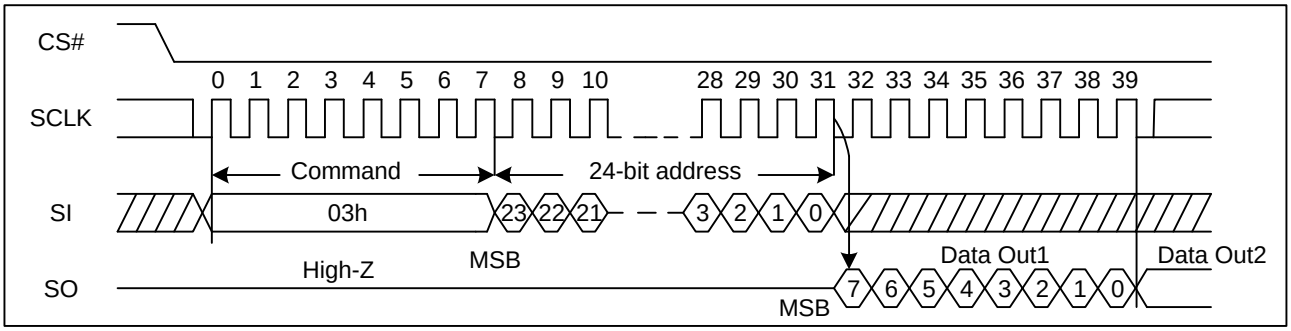
Figure 13. Write Enable for Volatile Status Register Sequence Diagram



8.8 Read Data Bytes (READ) (03h)

The Read Data Bytes (READ) command is followed by a 3-byte address (A23-A0), and each bit is latched-in on the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, and each bit is shifted out, at a Max frequency f_R, on the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) command. Any Read Data Bytes (READ) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

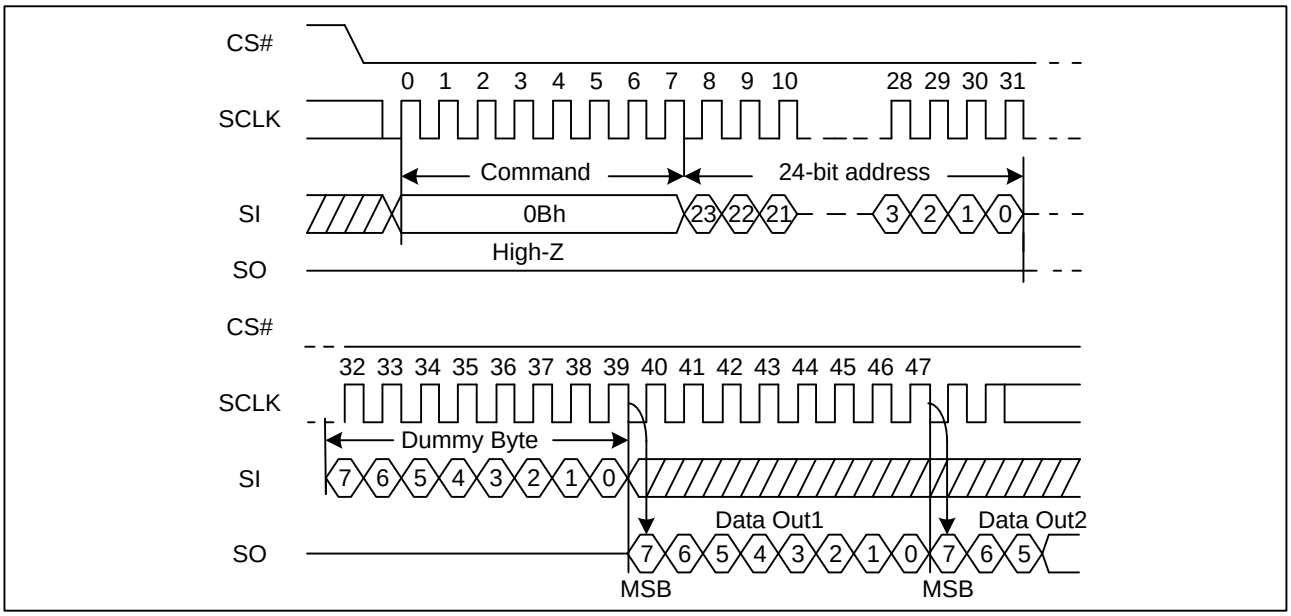
Figure 14. Read Data Bytes Sequence Diagram



8.9 Read Data Bytes at Higher Speed (Fast Read) (0Bh)

The Read Data Bytes at Higher Speed (Fast Read) command is for quickly reading data out. It is followed by a 3-byte address (A23-A0) and a dummy byte, and each bit is latched-in on the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, and each bit is shifted out, at a Max frequency f_C, on the falling edge of SCLK. The first byte address can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

Figure 15. Read Data Bytes at Higher Speed Sequence Diagram

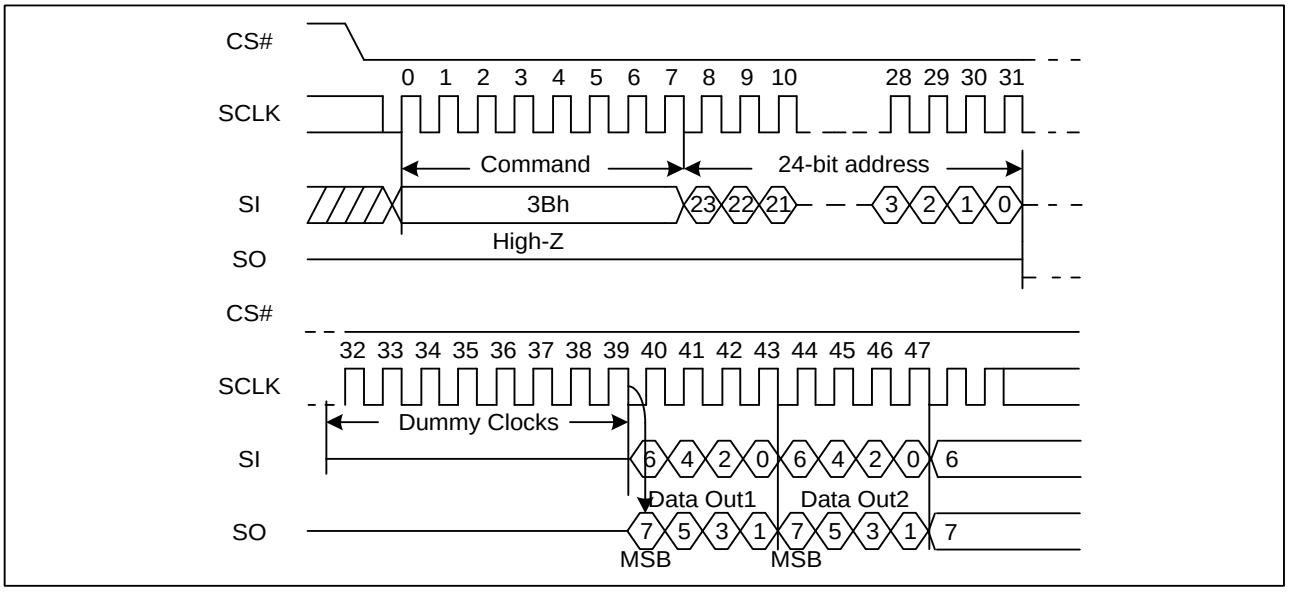


8.10 Dual Output Fast Read (3Bh)

The Dual Output Fast Read command is followed by 3-byte address (A23-A0) and a dummy byte, and each bit is latched in on the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO.

The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

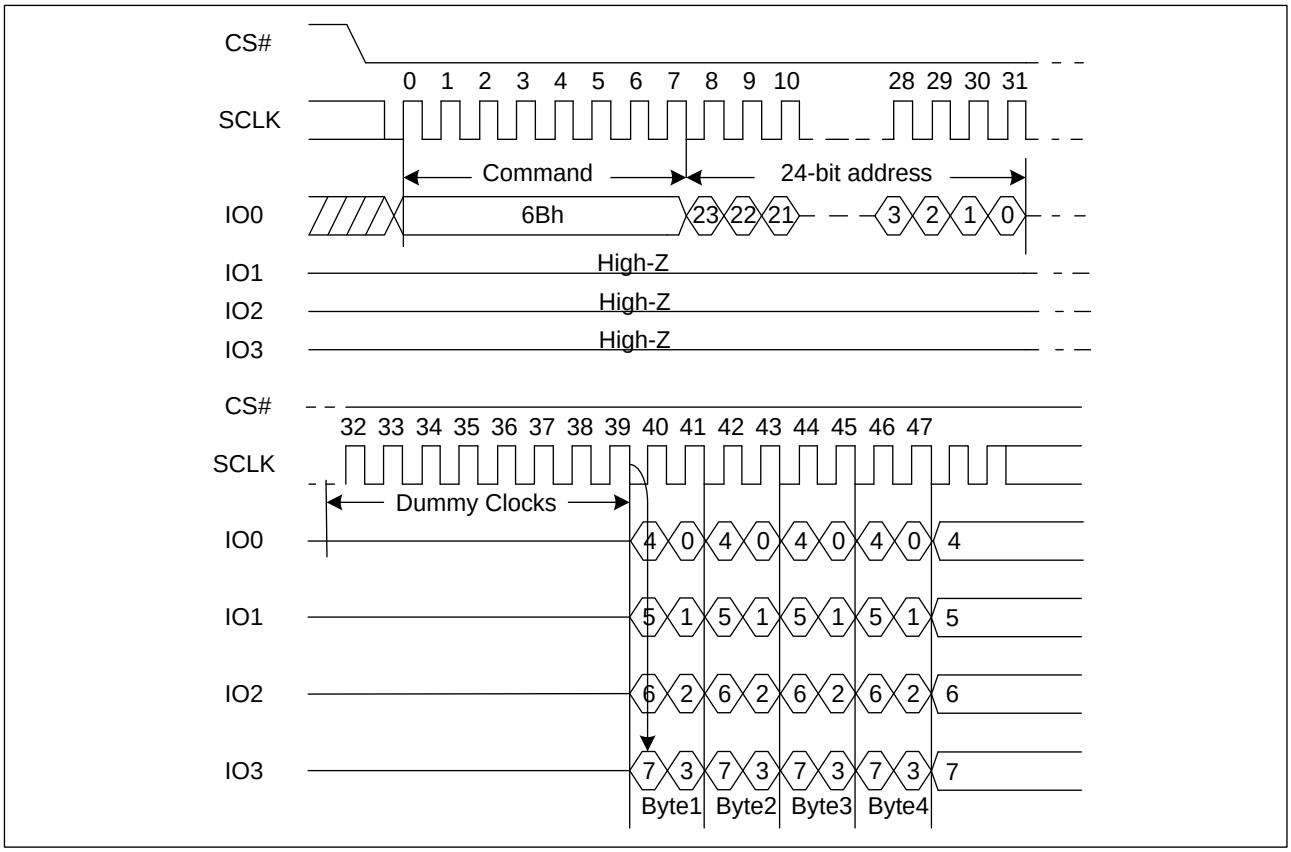
Figure 16. Dual Output Fast Read Sequence Diagram



8.11 Quad Output Fast Read (6Bh)

The Quad Output Fast Read command is followed by 3-byte address (A23-A0) and a dummy byte, and each bit is latched in on the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO3, IO2, IO1 and IO0. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

Figure 17. Quad Output Fast Read Sequence Diagram



8.12 Dual I/O Fast Read (BBh)

The Dual I/O Fast Read command is similar to the Dual Output Fast Read command but with the capability to input the 3-byte address (A23-A0) and a “Continuous Read Mode” byte 2-bit per clock by SI and SO, and each bit is latched in on the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

Dual I/O Fast Read with “Continuous Read Mode”

The Dual I/O Fast Read command can further reduce command overhead through setting the “Continuous Read Mode” bits (M7-0) after the input 3-byte address (A23-A0). If the “Continuous Read Mode” bits (M5-4) = (1, 0), then the next Dual I/O Fast Read command (after CS# is raised and then lowered) does not require the BBh command code. If the “Continuous Read Mode” bits (M5-4) ≠ (1, 0), the next command requires the command code, thus returning to normal operation. A Reset command can be also used to reset (M7-0) before issuing normal command.

Figure 18. Dual I/O Fast Read Sequence Diagram ((M5-4) ≠ (1, 0))

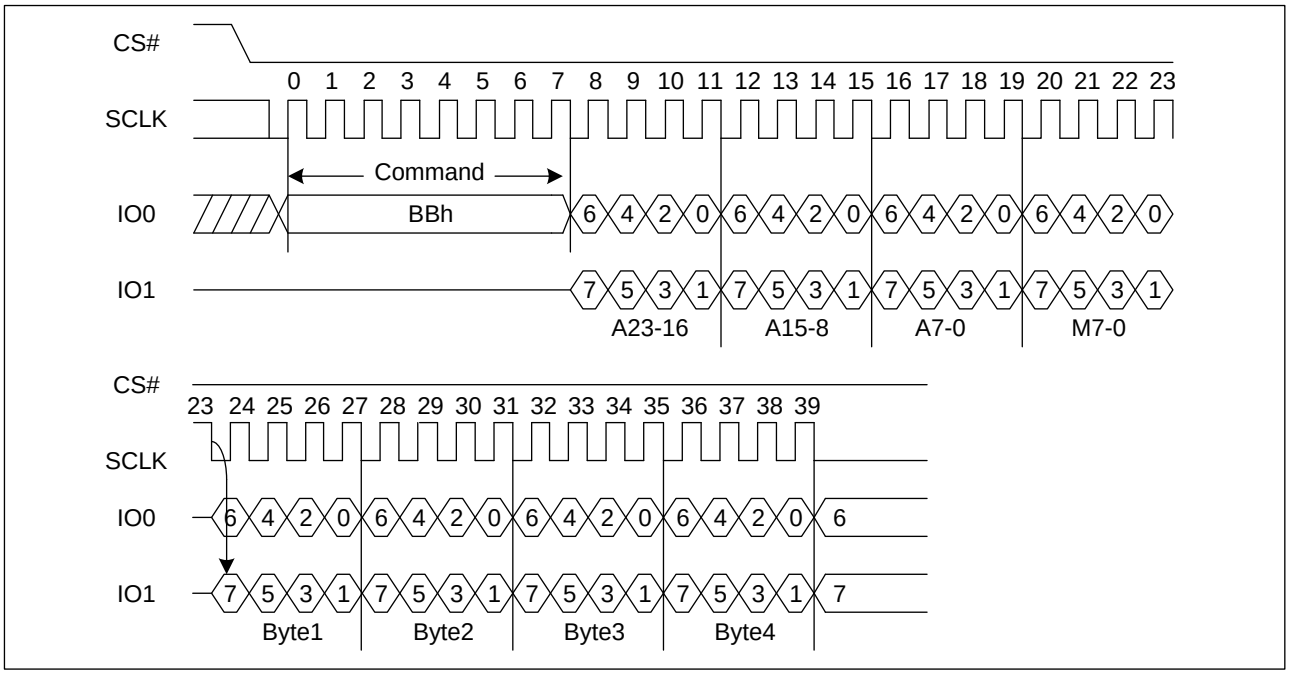
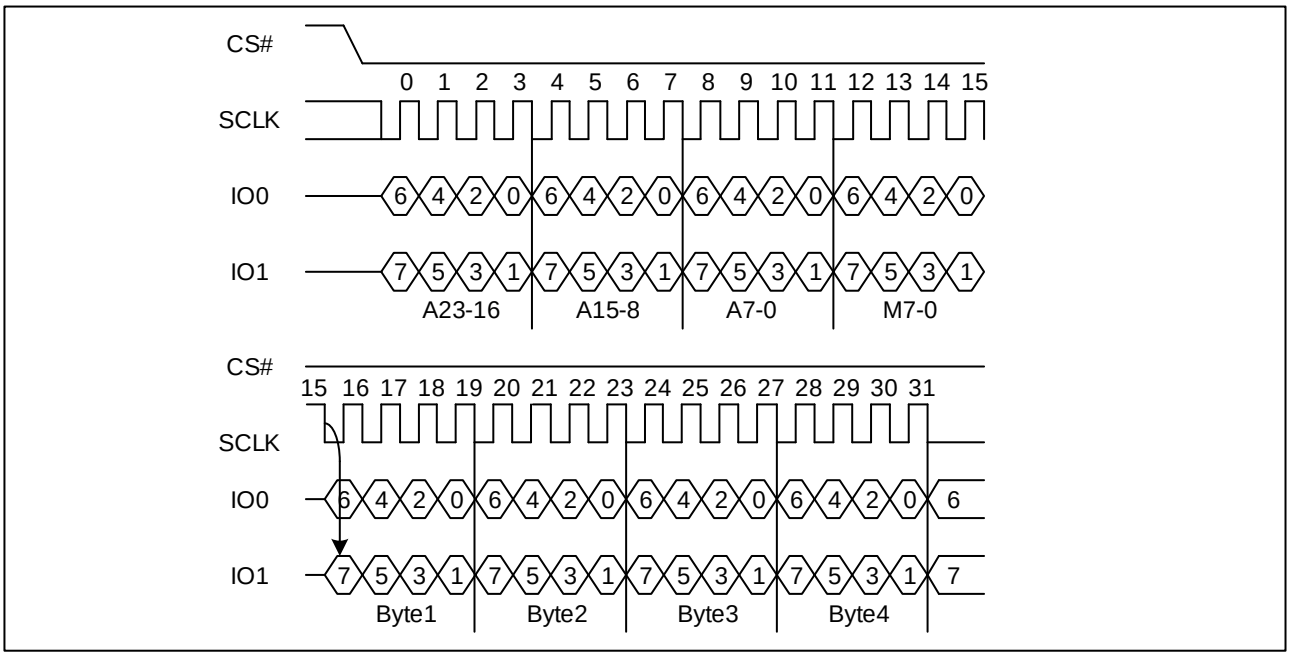


Figure 19. Dual I/O Fast Read Sequence Diagram ((M5-4) = (1, 0))



8.13 Quad I/O Fast Read (EBh)

The Quad I/O Fast Read command is similar to the Quad Output Fast Read command but with the capability to input the 3-byte address (A23-A0) and a “Continuous Read Mode” byte and 4-dummy clock 4-bit per clock by IO0, IO1, IO2, IO3, and each bit is latched in on the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO0, IO1, IO2, IO3. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

Quad I/O Fast Read with “Continuous Read Mode”

The Quad I/O Fast Read command can further reduce command overhead through setting the “Continuous Read Mode” bits (M7-0) after the input 3-byte address (A23-A0). If the “Continuous Read Mode” bits (M5-4) = (1, 0), then the next Quad I/O Fast Read command (after CS# is raised and then lowered) does not require the EBh command code. If the “Continuous Read Mode” bits (M5-4) ≠ (1, 0), the next command requires the command code, thus returning to normal operation. A Reset command can be also used to reset (M7-0) before issuing normal command.

Figure 20. Quad I/O Fast Read Sequence Diagram ((M5-4) ≠ (1, 0))

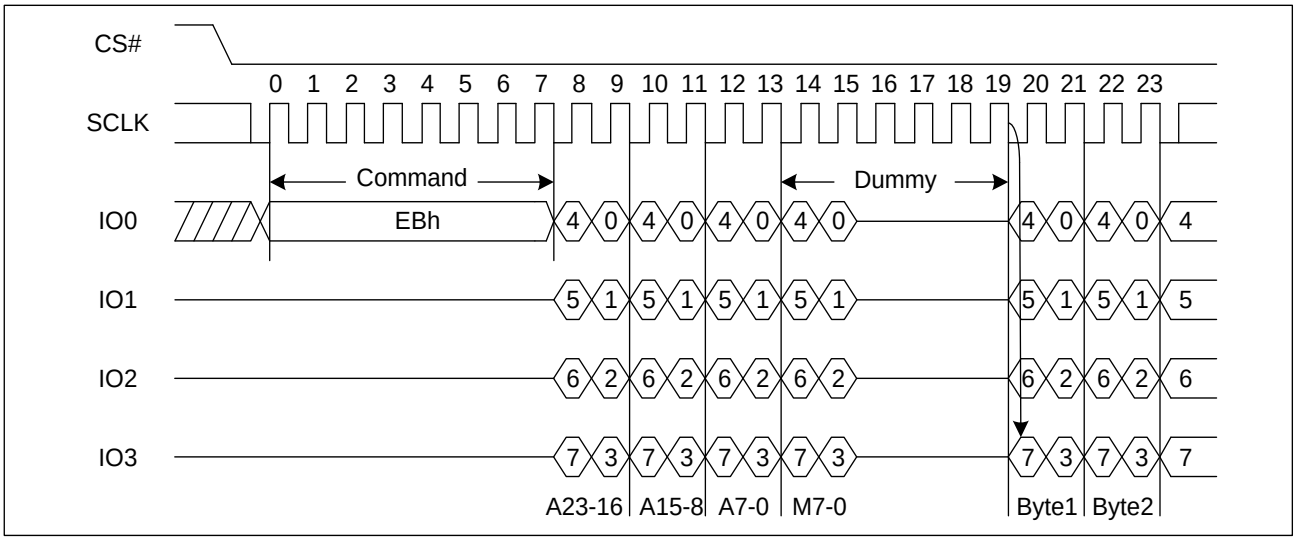
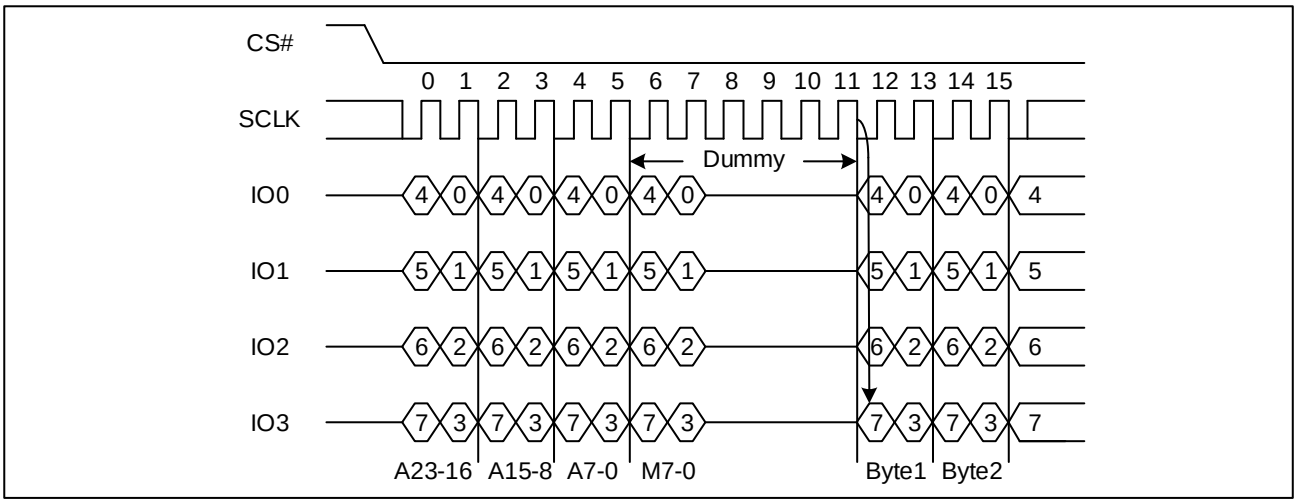


Figure 21. Quad I/O Fast Read Sequence Diagram ((M5-4) = (1, 0))



Quad I/O Fast Read with “8/16/32/64-Byte Wrap Around” in Standard SPI mode

The Quad I/O Fast Read command can be used to access a specific portion within a page by issuing “Set Burst with Wrap” (77h) commands prior to EBh. The “Set Burst with Wrap” (77h) command can either enable or disable the “Wrap Around” feature for the following EBh commands. When “Wrap Around” is enabled, the data being accessed can be limited to either an 8/16/32/64-byte section of a 256-byte page. The output data starts at the initial address specified in the command, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around the beginning boundary automatically until CS# is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands. The “Set Burst with Wrap”

command allows three “Wrap Bits” W6-W4 to be set. The W4 bit is used to enable or disable the “Wrap Around” operation while W6-W5 is used to specify the length of the wrap around section within a page.

8.14 DTR Quad I/O Fast Read (EDh)

The DTRQIO instruction enables Double Transfer Rate throughput on quad I/O of Serial Flash in read mode. The address (interleave on 4 I/O pins) is latched on both rising and falling edge of SCLK, and data (interleave on 4 I/O pins) shift out on both rising and falling edge of SCLK. The 8-bit address can be latched-in at one clock, and 8-bit data can be read out at one clock, which means four bits at rising edge of clock, the other four bits at falling edge of clock. The first address Byte can be at any location. The address is automatically increased to the next higher address after each Byte data is shifted out, so the whole memory can be read out at a single DTRQIO instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing DTRQIO instruction, the following address/dummy/data out will perform as 8-bit instead of previous 1-bit.

While Program/Erase/Write Status Register cycle is in progress, DTRQIO instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Quad I/O DTR Read with “Continuous Read Mode”

The Quad I/O DTR Read command can further reduce command overhead through setting the “Continuous Read Mode” bits (M7-0) after the input address. If the “Continuous Read Mode” bits (M5-4) = (1, 0), then the next Quad I/O DTR Read command (after CS# is raised and then lowered) does not require the EDh command code. If the “Continuous Read Mode” bits (M5-4) do not equal to (1, 0), the next command requires the first EDh command code, thus returning to normal operation. The only way to quit the Quad I/O DTR Continuous Read Mode” is to set the “Continuous Read Mode” bits (M5-4) not equal to (1, 0).

Figure 22. DTR Quad I/O Fast Read Sequence Diagram ((M5-4)≠ (1, 0))

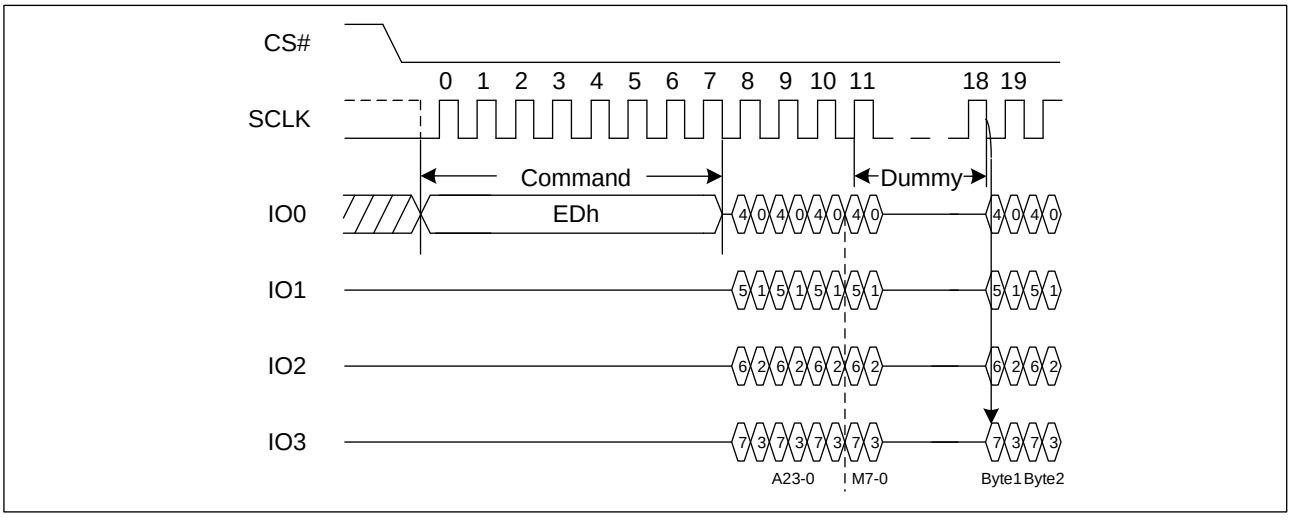
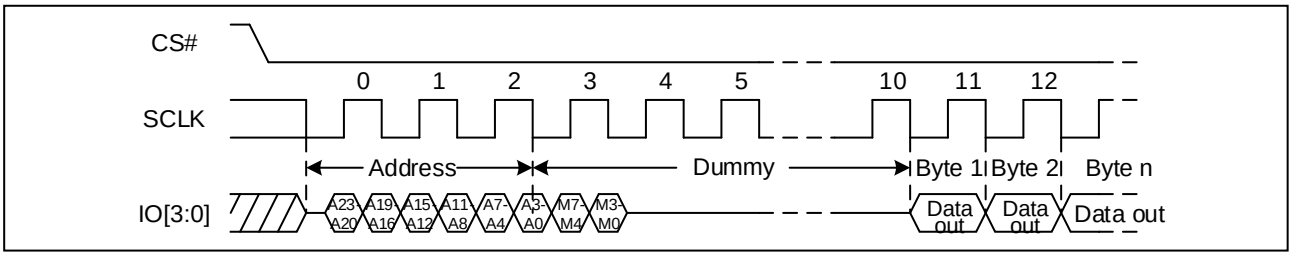


Figure 23. DTR Quad I/O Fast Read Sequence Diagram ((M5-4) = (1, 0))



8.15 Set Burst with Wrap (77h)

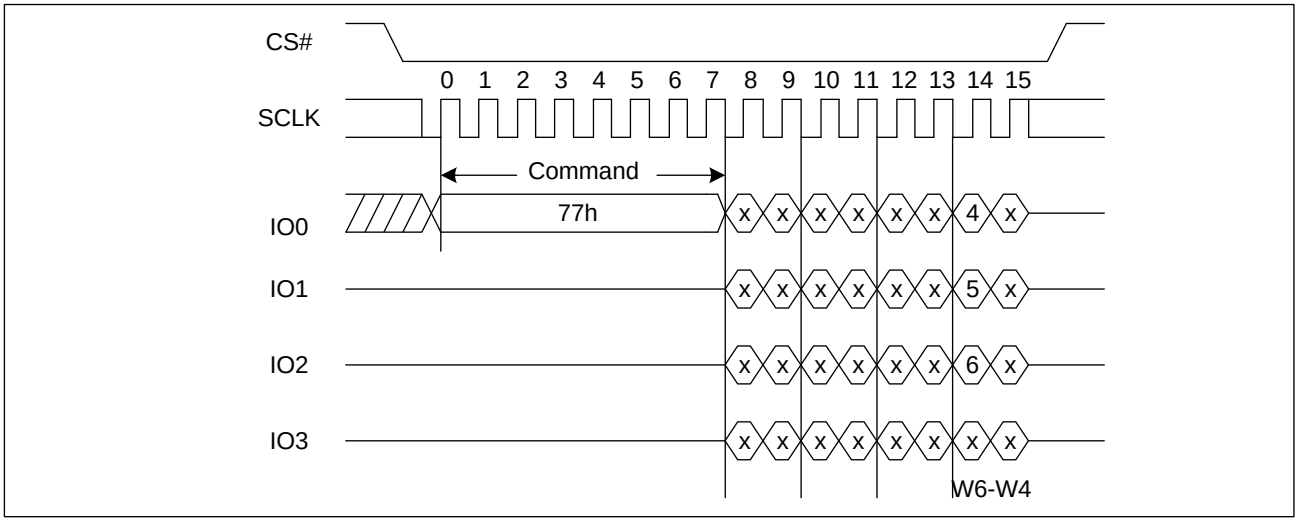
The Set Burst with Wrap command is used in conjunction with "Quad I/O Fast Read" command to access a fixed length of 8/16/32/64-byte section within a 256-byte page, in standard SPI mode.

The Set Burst with Wrap command sequence: CS# goes low → Send Set Burst with Wrap command → Send 24 dummy bits → Send 8 bits "Wrap bits" → CS# goes high.

W6,W5	W4=0		W4=1 (default)	
	Wrap Around	Wrap Length	Wrap Around	Wrap Length
0, 0	Yes	8-byte	No	N/A
0, 1	Yes	16-byte	No	N/A
1, 0	Yes	32-byte	No	N/A
1, 1	Yes	64-byte	No	N/A

If the W6-W4 bits are set by the Set Burst with Wrap command, all the following "Quad I/O Fast Read" command will use the W6-W4 setting to access the 8/16/32/64-byte section within any page. To exit the "Wrap Around" function and return to normal read operation, another Set Burst with Wrap command should be issued to set W4=1.

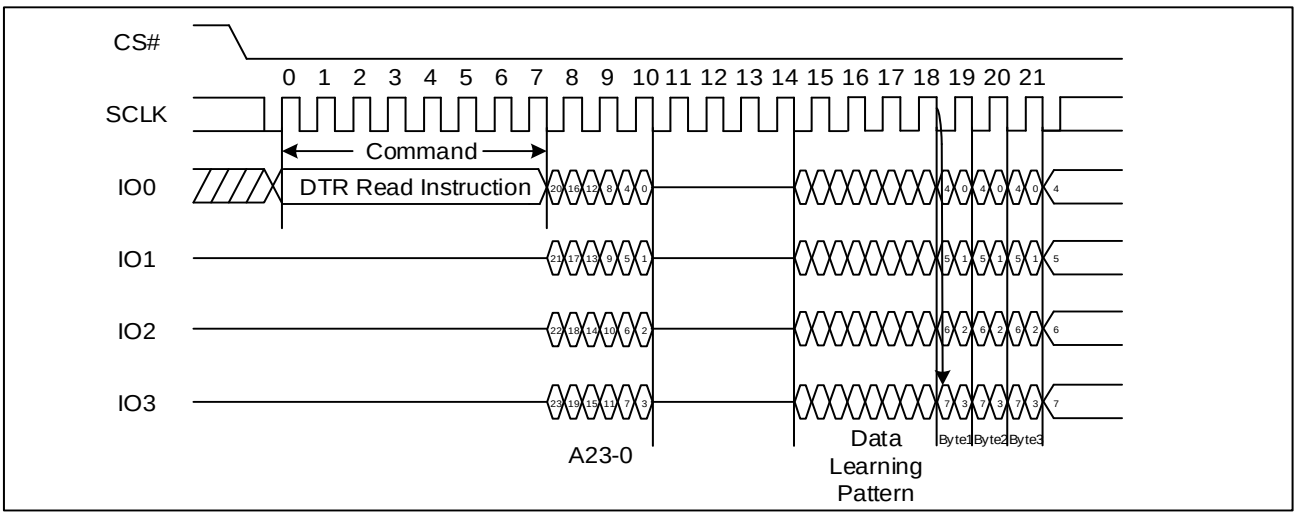
Figure 24. Set Burst with Wrap Sequence Diagram



8.16 Write Data Learning Pattern (4Ah)

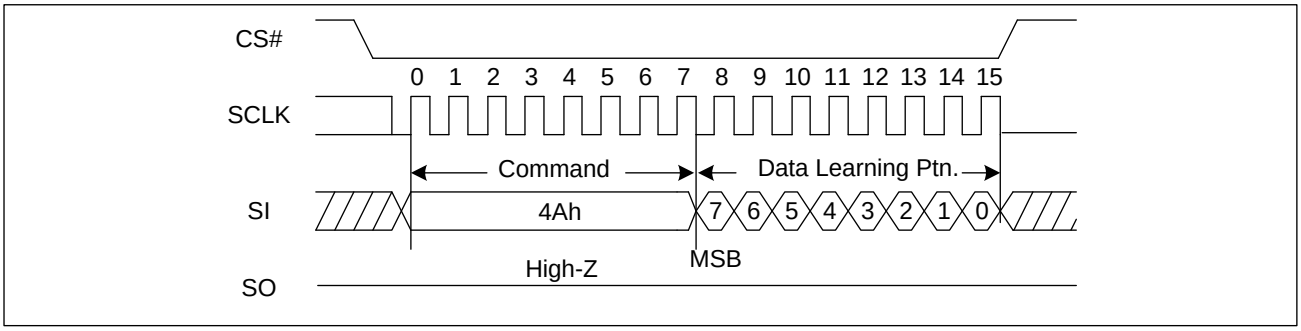
For Quad DTR Read commands, a pre-defined "Data Learning Pattern" can be used by the flash memory controller to determine the flash data output timing on 4 I/O pins. When DLP=1, during the last 4 dummy clocks just prior to the data output, GD25F128F will output "00110100" Data Learning Pattern sequence on each of the 4 I/O pins. During this period, controller can fine tune the data latching timing for each I/O pin to achieve optimum system performance. Setting DLP=0 will disable the Data Learning Pattern output.

Figure 25. Data Learning Pattern Output Sequence Diagram



The Data Learning Pattern can also be defined by a “Write Data Learning Pattern (4Ah)” command followed by 8-bit user-defined pattern. The user defined pattern is volatile. After device power cycle, the Data Learning Pattern will return to the default value of “00110100”.

Figure 26. Write Data Learning Pattern Sequence Diagram



8.17 Page Program (PP) (02h)

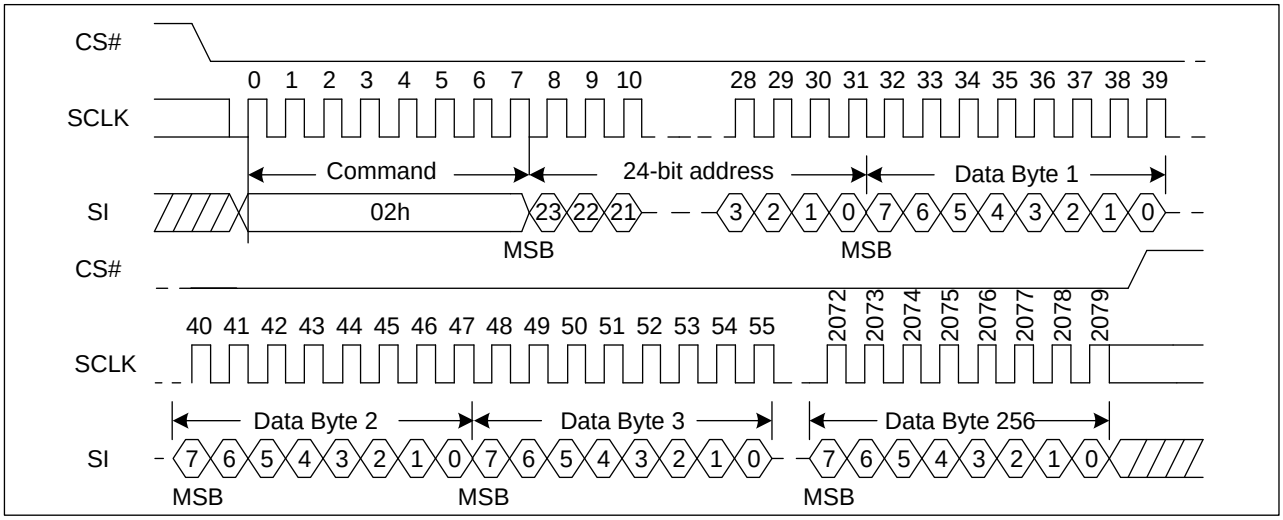
The Page Program (PP) command is for programming the memory. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command.

The Page Program (PP) command is entered by driving CS# Low, followed by the command code, three address bytes and at least one data byte on SI. If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). CS# must be driven low for the entire duration of the sequence. The Page Program command sequence: CS# goes low → sending Page Program command → 3-byte address on SI → at least 1 byte data on SI → CS# goes high. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Page Program (PP) command is not executed.

As soon as CS# is driven high, the self-timed Page Program cycle (whose duration is t_{PP}) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Page Program (PP) command applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) is not executed.

Figure 27. Page Program Sequence Diagram



8.18 Quad Page Program (32h)

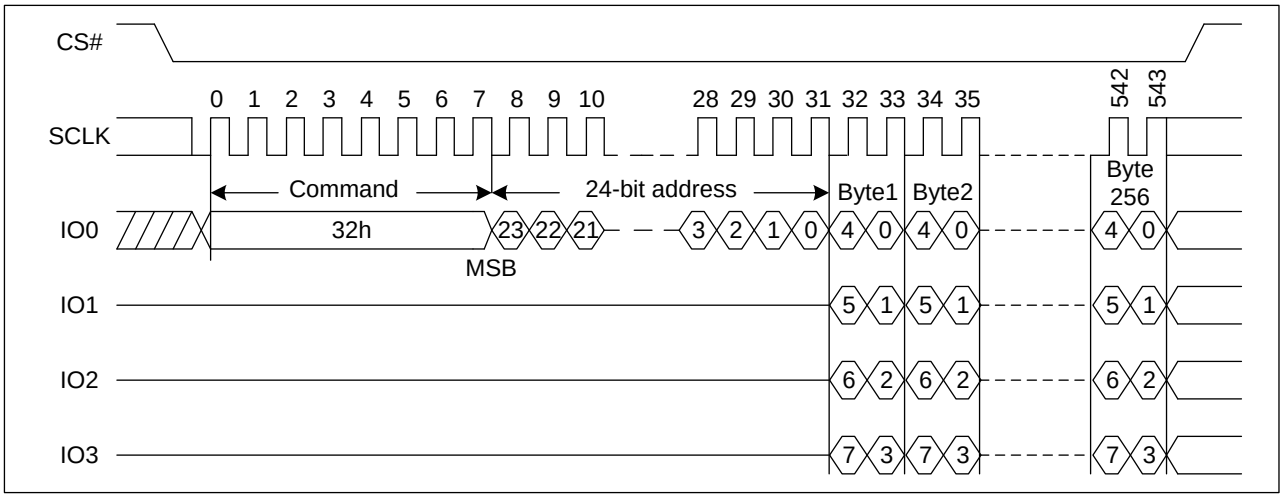
The Quad Page Program command is for programming the memory using four pins: IO0, IO1, IO2, and IO3. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command. The quad Page Program command is entered by driving CS# Low, followed by the command code (32h), three address bytes and at least one data byte on IO pins.

If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Quad Page Program (PP) command is not executed.

As soon as CS# is driven high, the self-timed Quad Page Program cycle (whose duration is t_{PP}) is initiated. While the Quad Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Quad Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Quad Page Program command applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) is not executed.

Figure 28. Quad Page Program Sequence Diagram

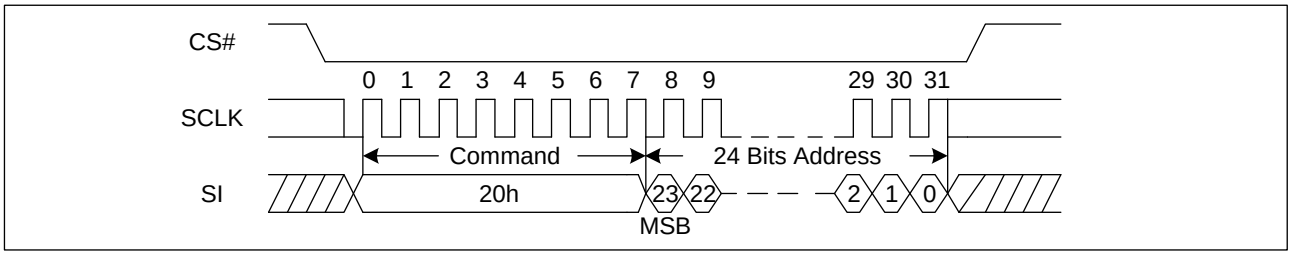


8.19 Sector Erase (SE) (20h)

The Sector Erase (SE) command is for erasing the all data of the chosen sector. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The Sector Erase (SE) command is entered by driving CS# low, followed by the command code, and 3-address byte on SI. Any address inside the sector is a valid address for the Sector Erase (SE) command. CS# must be driven low for the entire duration of the sequence.

The Sector Erase command sequence: CS# goes low → sending Sector Erase command → 3-byte address on SI → CS# goes high. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the Sector Erase (SE) command is not executed. As soon as CS# is driven high, the self-timed Sector Erase cycle (whose duration is t_{SE}) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A Sector Erase (SE) command applied to a sector which is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) bit is not executed.

Figure 29. Sector Erase Sequence Diagram



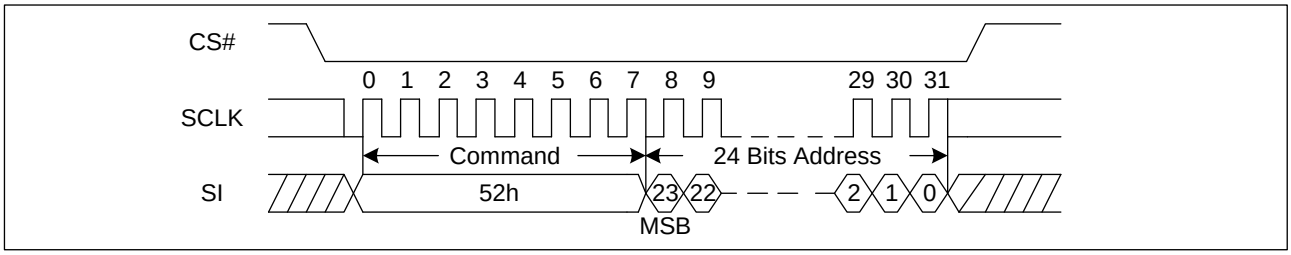
8.20 32KB Block Erase (BE32) (52h)

The 32KB Block Erase command is for erasing the all data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 32KB Block Erase command is entered by driving CS# low, followed by the command code, and three address bytes on SI. Any address inside the block is a valid address for the 32KB Block Erase command. CS# must be driven low for the entire duration of the sequence.

The 32KB Block Erase command sequence: CS# goes low → sending 32KB Block Erase command → 3-byte address on SI → CS# goes high. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise

the 32KB Block Erase command is not executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is t_{BE1}) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 32KB Block Erase command applied to a block which is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits is not executed.

Figure 30. 32KB Block Erase Sequence Diagram

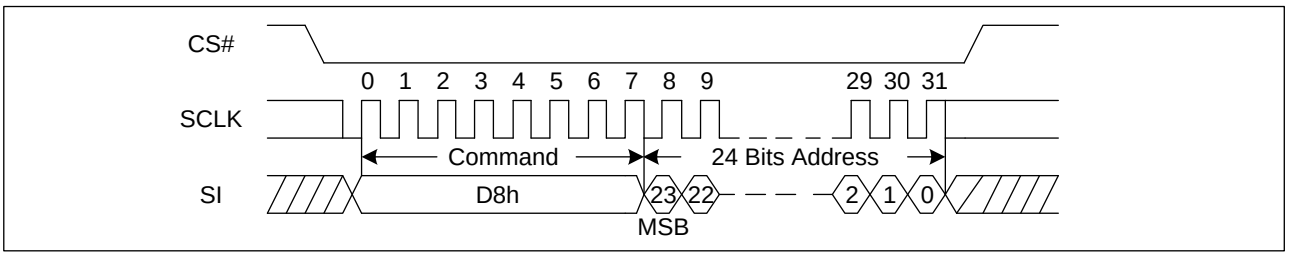


8.21 64KB Block Erase (BE64) (D8h)

The 64KB Block Erase command is for erasing the all data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 64KB Block Erase command is entered by driving CS# low, followed by the command code, and three address bytes on SI. Any address inside the block is a valid address for the 64KB Block Erase command. CS# must be driven low for the entire duration of the sequence.

The 64KB Block Erase command sequence: CS# goes low → sending 64KB Block Erase command → 3-byte address on SI → CS# goes high. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 64KB Block Erase command is not executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is t_{BE2}) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 64KB Block Erase command applied to a block which is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits is not executed.

Figure 31. 64KB Block Erase Sequence Diagram



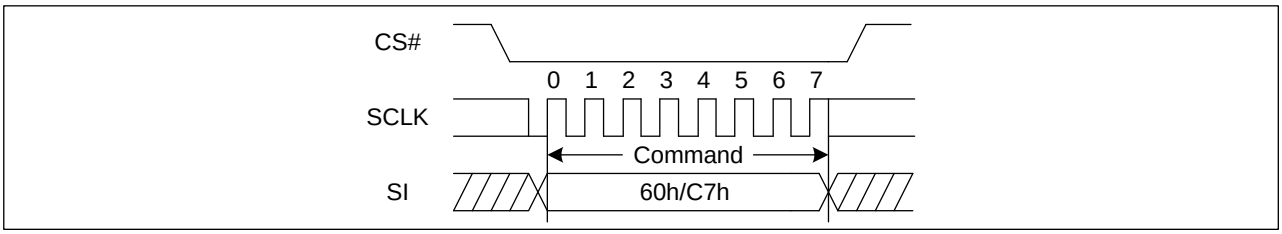
8.22 Chip Erase (CE) (60h/C7h)

The Chip Erase (CE) command is for erasing the all data of the chip. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit .The Chip Erase (CE) command is entered by driving CS# Low, followed by the command code on Serial Data Input (SI). CS# must be driven Low for the entire duration of the sequence.

The Chip Erase command sequence: CS# goes low → sending Chip Erase command → CS# goes high. CS# must be driven high after the eighth bit of the command code has been latched in; otherwise the Chip Erase command is not executed.

As soon as CS# is driven high, the self-timed Chip Erase cycle (whose duration is t_{CE}) is initiated. While the Chip Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Chip Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Chip Erase (CE) command is executed, if the no block is protected by the Block Protect bits. The Chip Erase (CE) command is ignored if one or more sectors are protected.

Figure 32. Chip Erase Sequence Diagram

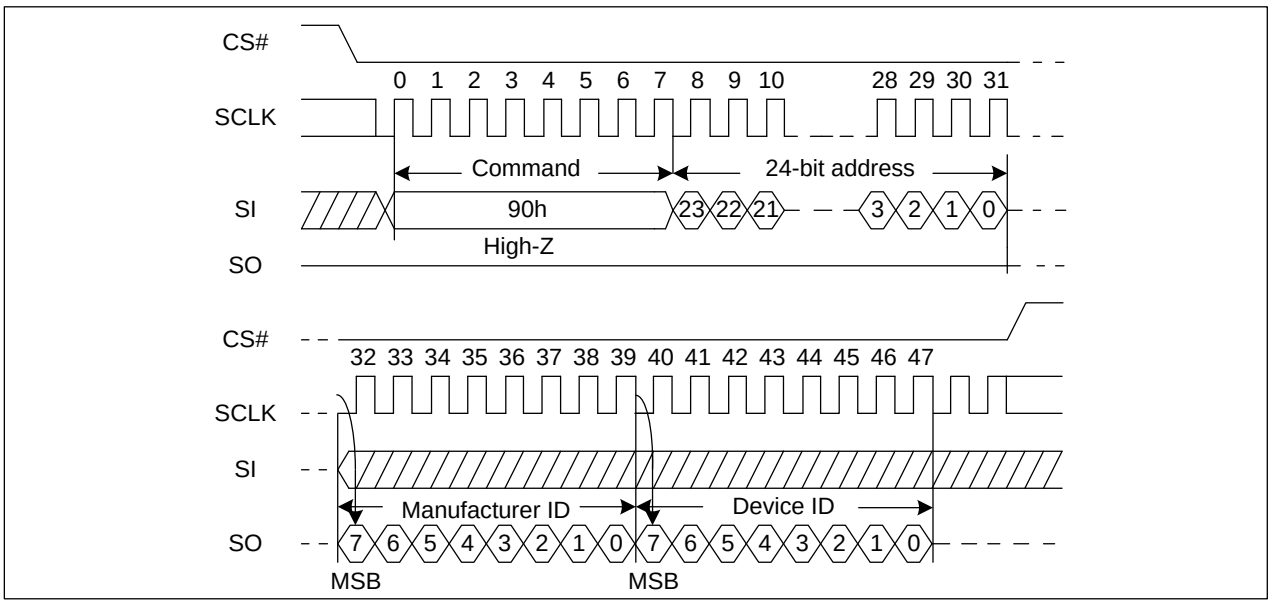


8.23 Read Manufacture ID/ Device ID (REMS) (90h)

The Read Manufacturer/Device ID command is an alternative to the Release from Power-Down / Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID.

The command is initiated by driving the CS# pin low and shifting the command code “90h” followed by a 24-bit address (A23-A0) of 000000H. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first.

Figure 33. Read Manufacture ID/ Device ID Sequence Diagram



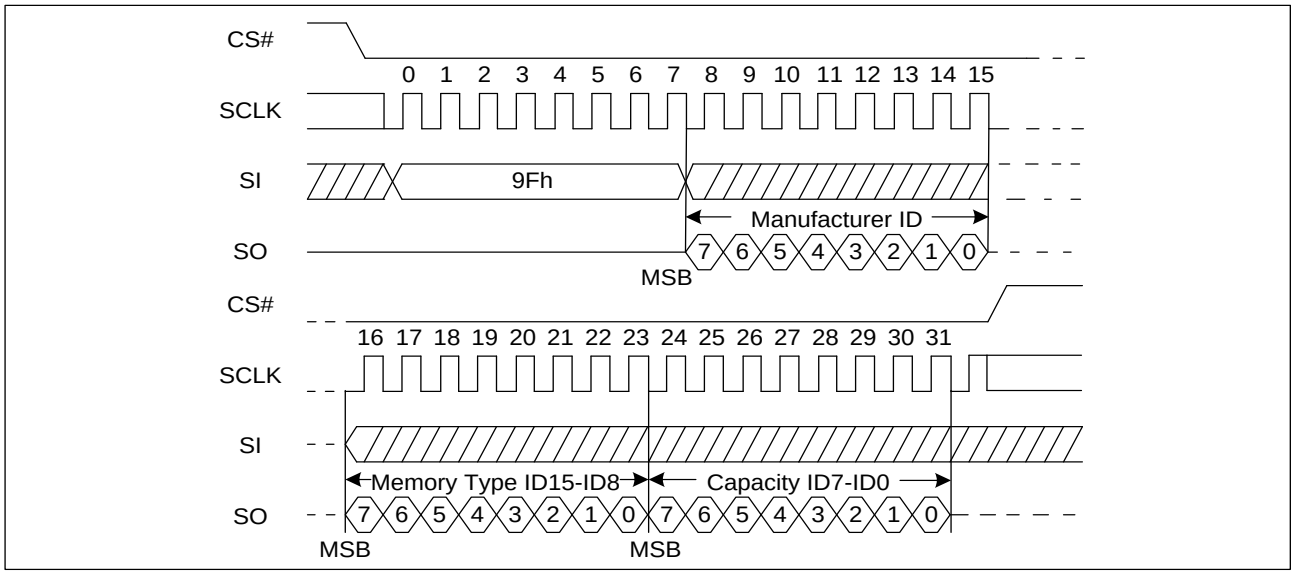
8.24 Read Identification (RDID) (9Fh)

The Read Identification (RDID) command allows the 8-bit manufacturer identification to be read, followed by two bytes of device identification. The device identification indicates the memory type in the first byte, and the memory capacity of the device in the second byte. The Read Identification (RDID) command while an Erase or Program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress. The Read Identification (RDID) command should not be issued while the device is in Deep Power-Down Mode.

The device is first selected by driving CS# low. Then, the 8-bit command code for the command is shifted in. This is followed by the 24-bit device identification, stored in the memory. Each bit is shifted out on the falling edge of Serial Clock. The Read

Identification (RDID) command is terminated by driving CS# high at any time during data output. When CS# is driven high, the device is in the Standby Mode. Once in the Standby Mode, the device waits to be selected, so that it can receive, decode and execute commands.

Figure 34. Read Identification ID Sequence Diagram

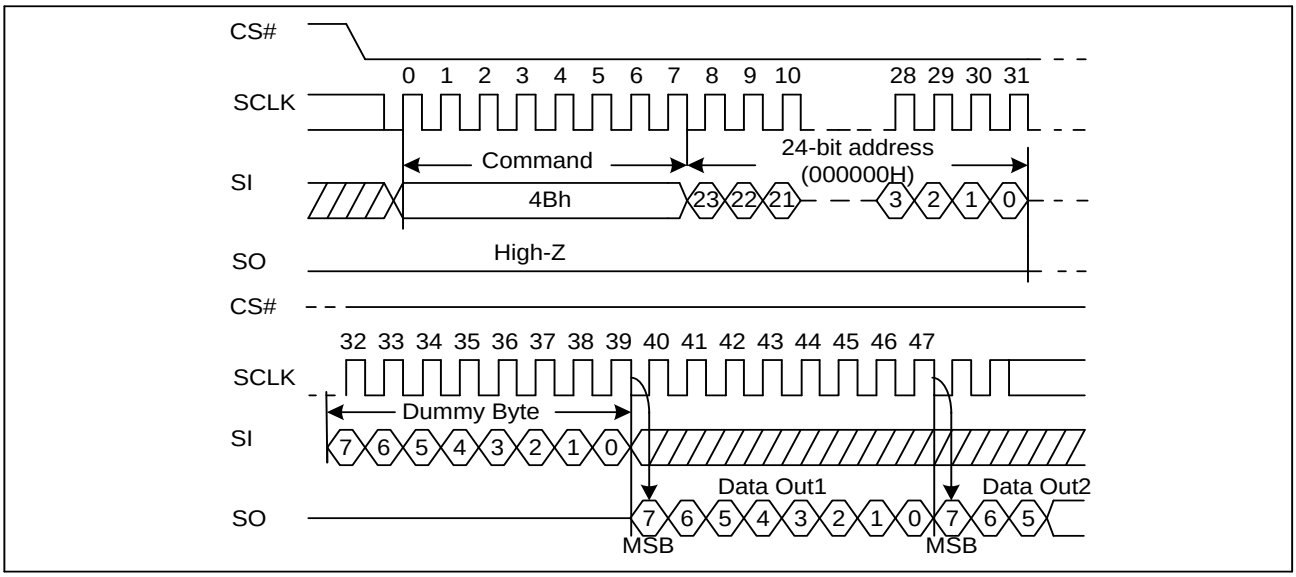


8.25 Read Unique ID (4Bh)

The Read Unique ID command accesses a factory-set read-only 128bit number that is unique to each device. The Unique ID can be used in conjunction with user software methods to help prevent copying or cloning of a system.

The Read Unique ID command sequence: CS# goes low → sending Read Unique ID command → 3-Byte Address (000000H) →Dummy Byte→128bit Unique ID Out →CS# goes high.

Figure 35. Read Unique ID Sequence Diagram



8.26 Erase Security Registers (44h)

The GD25F128F provides 3x2048-Byte Security Registers which can be erased and programmed individually. These registers may be used by the system manufacturers to store security and other important information separately from the

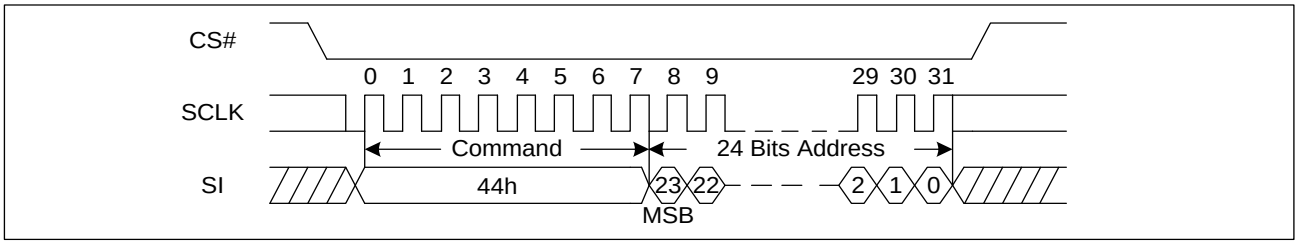
main memory array.

The Erase Security Registers command is similar to Sector/Block Erase command. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit.

The Erase Security Registers command sequence: CS# goes low → sending Erase Security Registers command → 3-byte address on SI → CS# goes high. The command sequence is shown below. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the Erase Security Registers command is not executed. As soon as CS# is driven high, the self-timed Erase Security Registers cycle (whose duration is t_{SE}) is initiated. While the Erase Security Registers cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Erase Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Security Registers Lock Bit (LB1, LB2, LB3) in the Status Register can be used to OTP protect the security registers. Once the LB bit is set to 1, the Security Registers will be permanently locked; the Erase Security Registers command will be ignored.

Address	A23-16	A15-12	A11	A10-0
Security Register #1	00H	0001b	0b	Don't care
Security Register #2	00H	0010b	0b	Don't care
Security Register #3	00H	0011b	0b	Don't care

Figure 36. Erase Security Registers command Sequence Diagram



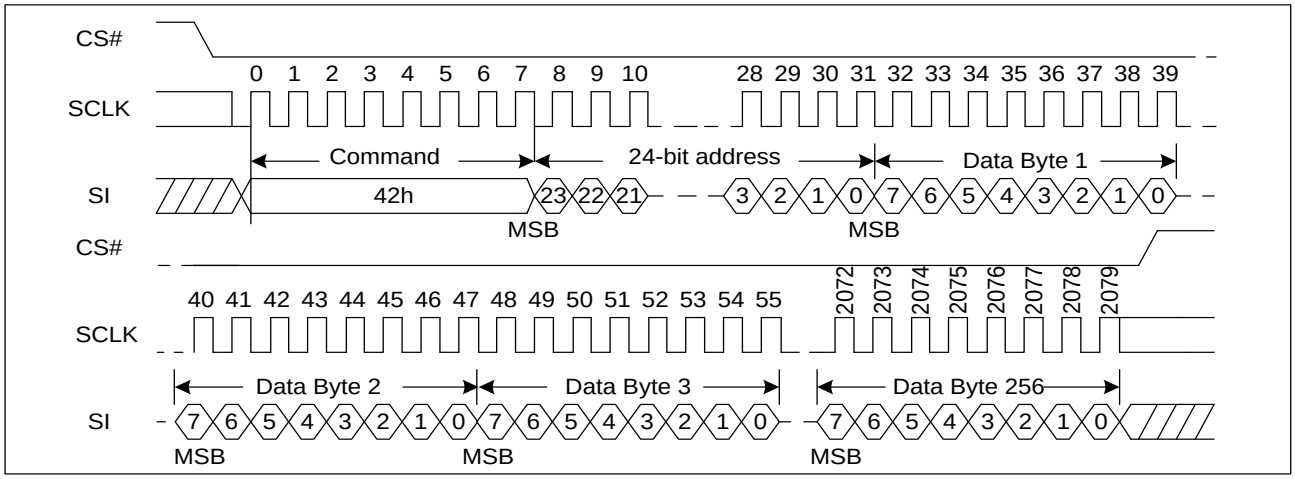
8.27 Program Security Registers (42h)

The Program Security Registers command is similar to the Page Program command. Each security register contains eight pages content. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Program Security Registers command. The Program Security Registers command is entered by driving CS# Low, followed by the command code (42h), three address bytes and at least one data byte on SI. As soon as CS# is driven high, the self-timed Program Security Registers cycle (whose duration is t_{PP}) is initiated. While the Program Security Registers cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Program Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

If the Security Registers Lock Bit (LB1, LB2, LB3) is set to 1, the Security Registers will be permanently locked. Program Security Registers command will be ignored.

Address	A23-16	A15-12	A11	A10-0
Security Register #1	00H	0001b	0b	Byte Address
Security Register #2	00H	0010b	0b	Byte Address
Security Register #3	00H	0011b	0b	Byte Address

Figure 37. Program Security Registers command Sequence Diagram

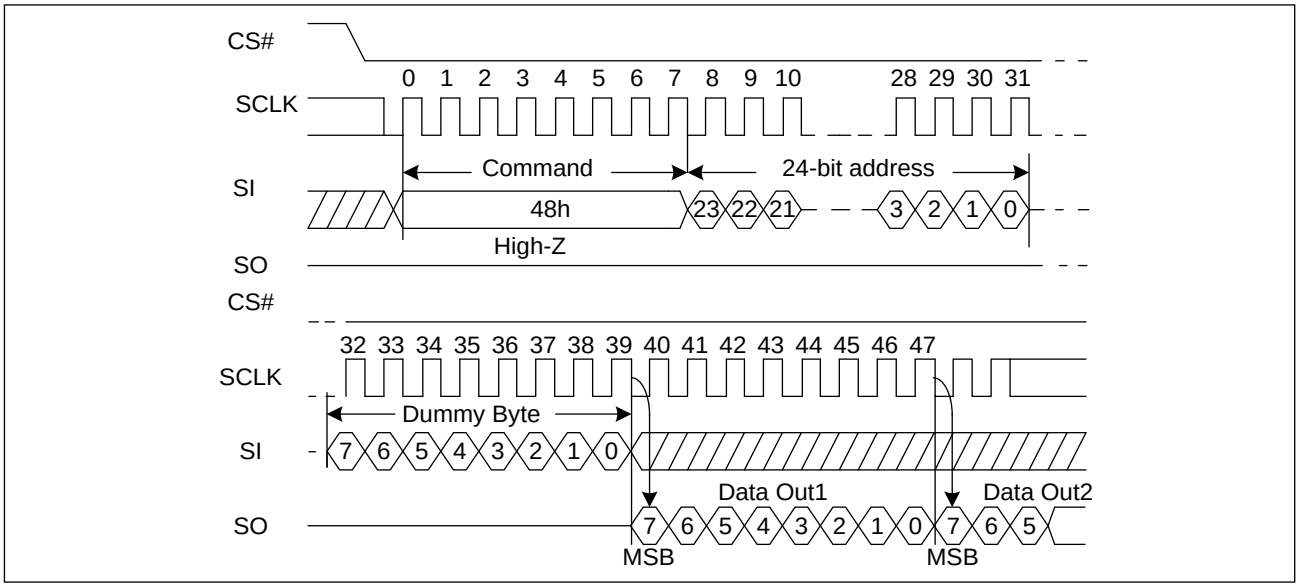


8.28 Read Security Registers (48h)

The Read Security Registers command is similar to Fast Read command. The command is followed by a 3-byte address (A23-A0) and a dummy byte, and each bit is latched-in on the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, and each bit is shifted out, at a Max frequency f_C, on the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. Once the A10-0 address reaches the last byte of the register (Byte 7FFH), it will reset to 000H, the command is completed by driving CS# high.

Address	A23-16	A15-12	A11	A10-0
Security Register #1	00H	0001b	0b	Byte Address
Security Register #2	00H	0010b	0b	Byte Address
Security Register #3	00H	0011b	0b	Byte Address

Figure 38. Read Security Registers command Sequence Diagram

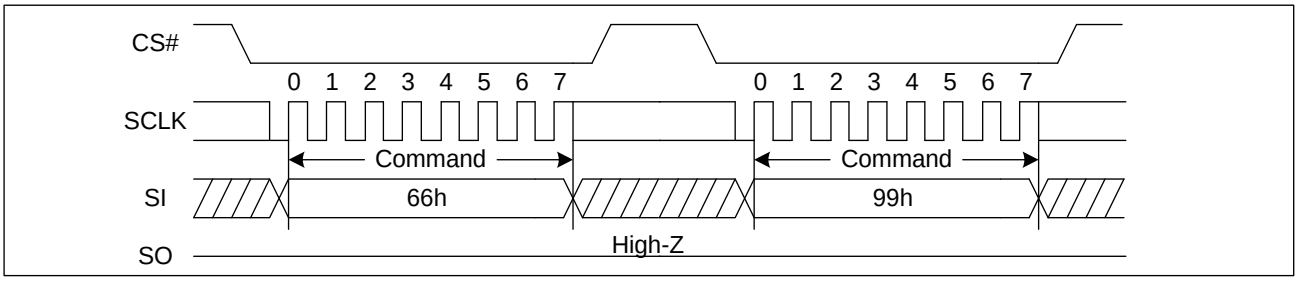


8.29 Enable Reset (66h) and Reset (99h)

If the Reset command is accepted, any on-going internal operation will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch status (WEL), Program/Erase Suspend status, Read Parameter setting (P7-P0), Deep Power Down Mode, Continuous Read Mode bit setting (M7-M0) and Wrap Bit Setting (W6-W4).

The "Enable Reset (66h)" and "Reset (99h)" command sequence as follow: CS# goes low → Sending Enable Reset command → CS# goes high → CS# goes low → Sending Reset command → CS# goes high. Once the Reset command is accepted by the device, the device will take approximately t_{RST} / t_{RST_E} to reset. During this period, no command will be accepted. Data corruption may happen if there is an on-going or suspended internal Erase or Program operation when Reset command sequence is accepted by the device. It is recommended to check the WIP bit and the SUS1/SUS2 bit in Status Register before issuing the Reset command sequence.

Figure 39. Enable Reset and Reset command Sequence Diagram



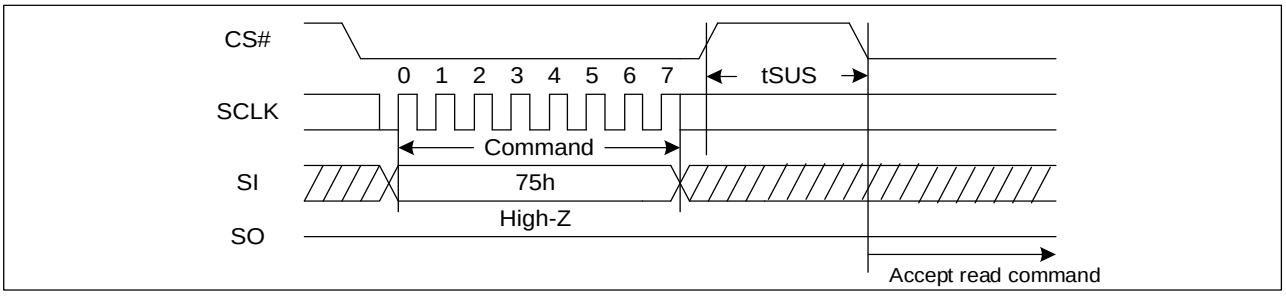
Note: Enable Reset (66h) and Reset (99h) commands cannot reset the device when the device is in Quad I/O DTR Continuous Read Mode. The only way to quit the Quad I/O DTR Continuous Read Mode is to set the "Continuous Read Mode" bits (M5-4) not equal to (1,0).

8.30 Program/Erase Suspend (PES) (75h)

The Program/Erase Suspend command "75h", allows the system to interrupt a page program or sector/block erase operation and then read data from any other sector or block. The Write Status Register command (01h, 31h, 11h) and Erase/Program Security Registers command (44h, 42h) and Erase commands (20h, 52h, D8h, C7h, 60h) and Page Program command (02h, 32h) are not allowed during Program suspend. The Write Status Register command (01h, 31h, 11h) and Erase Security Registers command (44h) and Erase commands (20h, 52h, D8h, C7h, 60h) are not allowed during Erase suspend. Program/Erase Suspend is valid only during the page program or sector/block erase operation. A maximum of time of "tsus" (See AC Characteristics) is required to suspend the program/erase operation.

The Program/Erase Suspend command will be accepted by the device only if the SUS1/SUS2 bit in the Status Register equal to 0 and WIP bit equal to 1 while a Page Program or a Sector or Block Erase operation is on-going. If the SUS1/SUS2 bit equal to 1 or WIP bit equal to 0, the Suspend command will be ignored by the device. The WIP bit will be cleared from 1 to 0 within "tsus" and the SUS1/SUS2 bit will be set from 0 to 1 immediately after Program/Erase Suspend. A power-off during the suspend period will reset the device and release the suspend state.

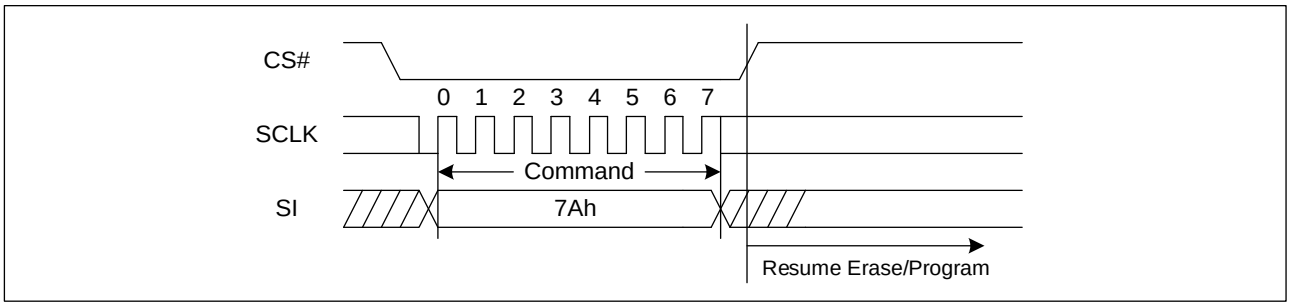
Figure 40. Program/Erase Suspend Sequence Diagram



8.31 Program/Erase Resume (PER) (7Ah)

The Program/Erase Resume command must be written to resume the program or sector/block erase operation after a Program/Erase Suspend command. The Program/Erase Resume command will be accepted by the device only if the SUS1/SUS2 bit equal to 1 and the WIP bit equal to 0. After issued the SUS1/SUS2 bit in the status register will be cleared from 1 to 0 immediately, the WIP bit will be set from 0 to 1 within 200ns and the Sector or Block will complete the erase operation or the page will complete the program operation. The Program/Erase Resume command will be ignored unless a Program/Erase Suspend is active.

Figure 41. Program/Erase Resume Sequence Diagram



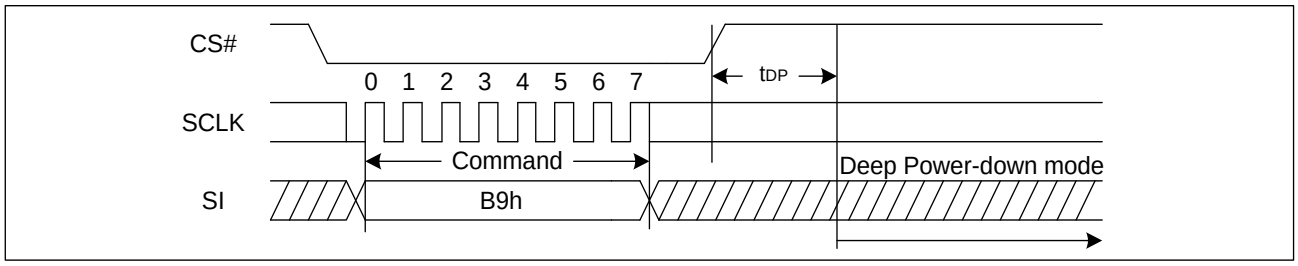
8.32 Deep Power-Down (DP) (B9h)

Executing the Deep Power-Down (DP) command is the only way to put the device in the lowest consumption mode (the Deep Power-Down Mode). It can also be used as an extra software protection mechanism, while the device is not in active use, since in this mode, the device ignores all Write, Program and Erase commands. Driving CS# high deselects the device, and puts the device in the Standby Mode (if there is no internal cycle currently in progress). But this mode is not the Deep Power-Down Mode. The Deep Power-Down Mode can only be entered by executing the Deep Power-Down (DP) command. Once the device has entered the Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down and Read Device ID (RDI) command or software reset command. The Release from Deep Power-Down and Read Device ID (RDI) command releases the device from Deep Power-Down mode, also allows the Device ID of the device to be output on SO.

The Deep Power-Down Mode automatically stops at Power-Down, and the device always in the Standby Mode after Power-Up.

The Deep Power-Down command sequence: CS# goes low → sending Deep Power-Down command → CS# goes high. CS# must be driven high after the eighth bit of the command code has been latched in; otherwise the Deep Power-Down (DP) command is not executed. As soon as CS# is driven high, it requires a delay of t_{DP} before the supply current is reduced to I_{CC2} and the Deep Power-Down Mode is entered. Any Deep Power-Down (DP) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 42. Deep Power-Down Sequence Diagram



8.33 Release from Deep Power-Down and Read Device ID (RDI) (ABh)

The Release from Power-Down and Read Device ID command is a multi-purpose command. It can be used to release the device from the Power-Down state or obtain the devices electronic identification (ID) number.

To release the device from the Power-Down state, the command is issued by driving the CS# pin low, shifting the instruction code "ABh" and driving CS# high. Release from Power-Down will take the time duration of t_{RES1} (See AC Characteristics) before the device will resume normal operation and other command are accepted. The CS# pin must remain high during the t_{RES1} time duration.

When used only to obtain the Device ID while not in the Power-Down state, the command is initiated by driving the CS# pin low and shifting the instruction code "ABh" followed by 3-dummy byte. The ID7~ID0 are then shifted out on the falling edge of SCLK with most significant bit (MSB) first. The Device ID value is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The command is completed by driving CS# high.

When used to release the device from the Power-Down state and obtain the ID7~ID0, the command is the same as previously described, except that after CS# is driven high it must remain high for a time duration of t_{RES2} (See AC Characteristics). After this time duration the device will resume normal operation and other command will be accepted. If the Release from Power-Down / Device ID command is issued while an Erase, Program or Write cycle is in process (when WIP equals 1) the command is ignored and will not have any effects on the current cycle.

Figure 43. Release Power-Down Sequence Diagram

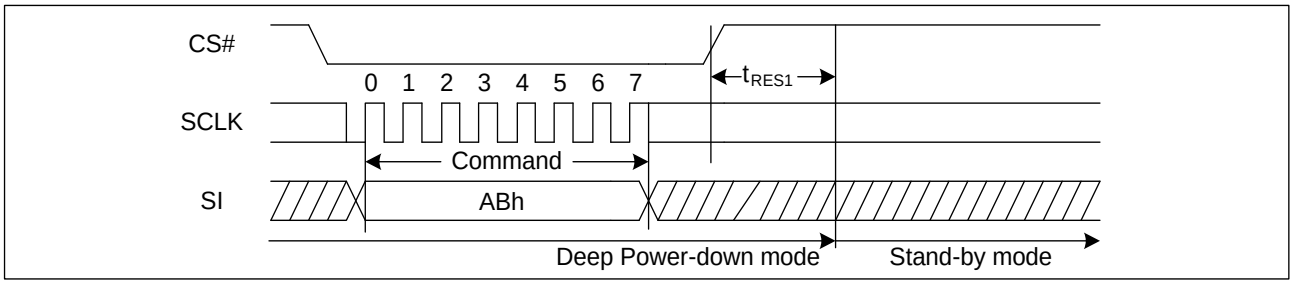
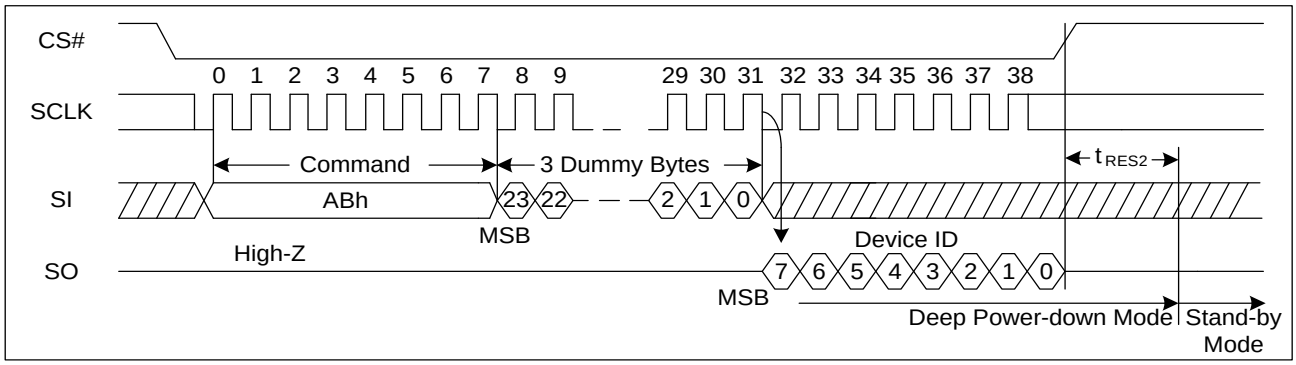


Figure 44. Release Power-Down/Read Device ID Sequence Diagram



8.34 Read Serial Flash Discoverable Parameter (5Ah)

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI. SFDP is a standard of JEDEC Standard No.216B.

Figure 45. Read Serial Flash Discoverable Parameter command Sequence Diagram

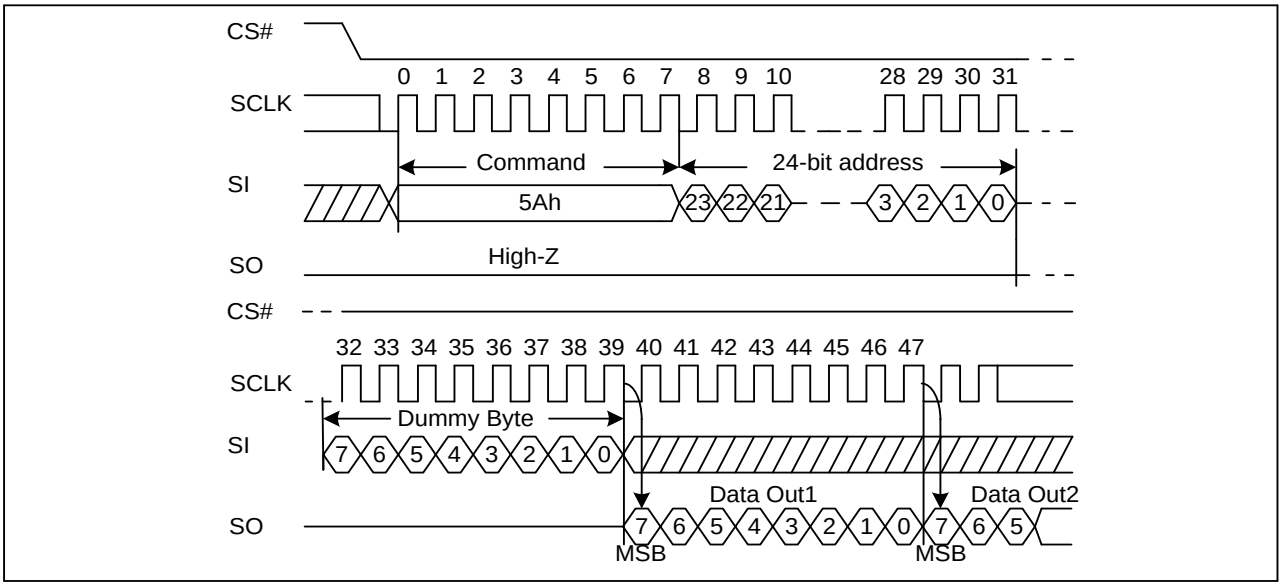


Table 12. Signature and Parameter Identification Data Values (Please contact GigaDevice for Details)

9 ELECTRICAL CHARACTERISTICS

9.1 Power-On Timing

Figure 46. Power-On Timing Sequence Diagram

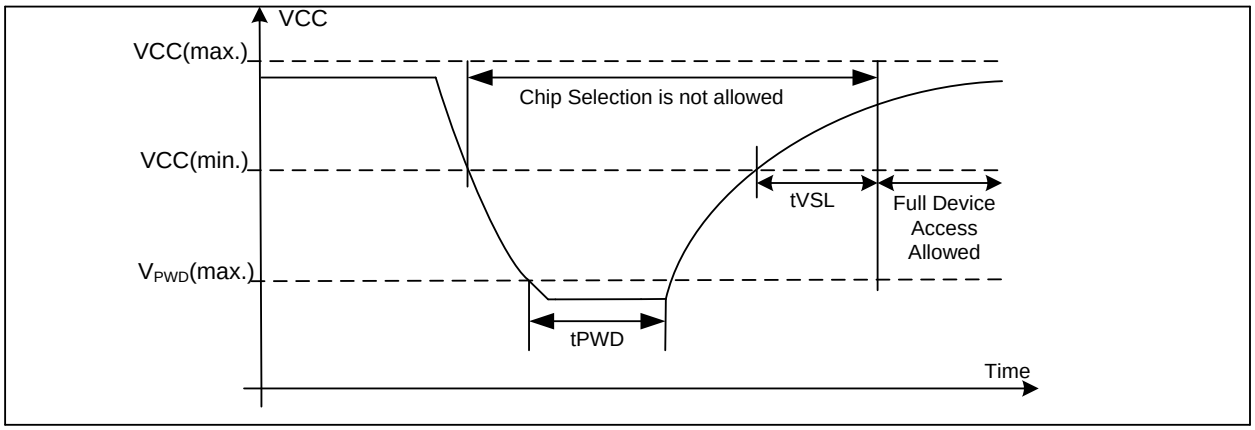


Table 13. Power-Up Timing and Write Inhibit Threshold

Symbol	Parameter	Min.	Max.	Unit
tVSL	VCC (min.) to device operation	2.5		ms
VWI	Write Inhibit Voltage	1.5	2.5	V
VPWD	VCC voltage needed to below VPWD for ensuring initialization will occur		0.5	V
tPWD	The minimum duration for ensuring initialization will occur	300		μs

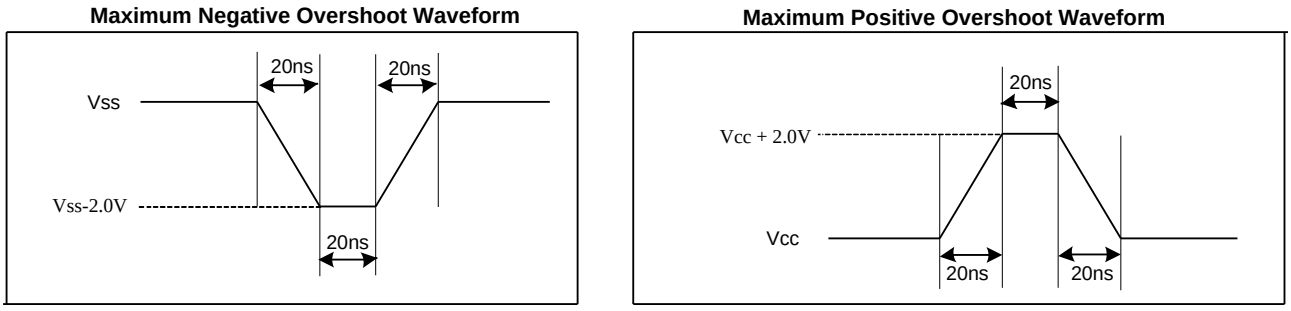
9.2 Initial Delivery State

The device is delivered with the memory array erased: all bits are set to 1 (each Byte contains FFH). The Status Register contains 00H, except that DRV0 bit (S21) and ECC bit (S14) and QE bit (S9) are set to 1.

9.3 Absolute Maximum Ratings

Parameter	Value	Unit
Ambient Operating Temperature (T_A)	Grade3: -40 to 85 Grade2: -40 to 105 Grade1: -40 to 125	℃
Storage Temperature	-65 to 150	℃
Transient Input/Output Voltage (note: overshoot)	-2.0 to VCC+2.0	V
Applied Input/Output Voltage	-0.6 to VCC+0.4	V
VCC	-0.6 to 4.2	V

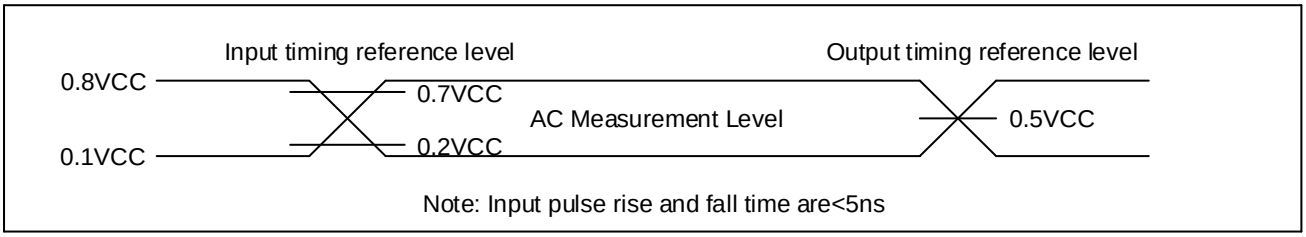
Figure 47. Input Test Waveform and Measurement Level



9.4 Capacitance Measurement Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
CIN	Input Capacitance			6	pF	VIN=0V
COUT	Output Capacitance			8	pF	VOUT=0V
C_L	Load Capacitance		30		pF	
	Input Rise And Fall time			5	ns	
	Input Pulse Voltage		0.1VCC to 0.8VCC		V	
	Input Timing Reference Voltage		0.2VCC to 0.7VCC		V	
	Output Timing Reference Voltage		0.5VCC		V	

Figure 48. Absolute Maximum Ratings Diagram



9.5 DC Characteristics

(T_A = -40℃~85℃, VCC=2.7~3.6V)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit.
I_{LI}	Input Leakage Current				±2	μA
I_{LO}	Output Leakage Current				±2	μA
I_{CC1}	Standby Current	CS#=VCC, VIN=VCC or VSS		16	100	μA
I_{CC2}	Deep Power-Down Current	CS#=VCC, VIN=VCC or VSS		1	25	μA
I_{CC3}	Operating Current (Read)	CLK=0.1VCC / 0.9VCC at 166MHz, Q=Open(x4 I/O)		19	35	mA
		CLK=0.1VCC / 0.9VCC at 80MHz, Q=Open(x4 I/O)		12	20	mA
		CLK=0.1VCC / 0.9VCC at 104MHz DTR, Q=Open(x4 I/O)		18	35	mA
I_{CC4}	Operating Current (PP)	CS#=VCC		12	25	mA
I_{CC5}	Operating Current (WRSR)	CS#=VCC		12	25	mA
I_{CC6}	Operating Current (SE)	CS#=VCC		12	25	mA
I_{CC7}	Operating Current (BE)	CS#=VCC		12	25	mA
I_{CC8}	Operating Current (CE)	CS#=VCC		12	25	mA
V_{IL}	Input Low Voltage		-0.5		0.2VCC	V
V_{IH}	Input High Voltage		0.7VCC		VCC+0.4	V
V_{OL}	Output Low Voltage	I_{OL} = 100μA			0.2	V
V_{OH}	Output High Voltage	I_{OH} = -100μA	VCC-0.2			V

Note:

1. Typical value at T_A = 25℃, VCC = 3.3V.
2. Value guaranteed by design and/or characterization, not 100% tested in production.

(T_A = -40℃~105℃, VCC=2.7~3.6V)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit.
I_{LI}	Input Leakage Current				±2	μA
I_{LO}	Output Leakage Current				±2	μA
I_{CC1}	Standby Current	CS#=VCC, VIN=VCC or VSS		16	150	μA
I_{CC2}	Deep Power-Down Current	CS#=VCC, VIN=VCC or VSS		1	45	μA
I_{CC3}	Operating Current (Read)	CLK=0.1VCC / 0.9VCC at 166MHz, Q=Open(x4 I/O)		19	40	mA
		CLK=0.1VCC / 0.9VCC at 80MHz, Q=Open(x4 I/O)		12	25	mA
		CLK=0.1VCC / 0.9VCC at 104MHz DTR, Q=Open(x4 I/O)		18	40	mA
I_{CC4}	Operating Current (PP)	CS#=VCC		12	30	mA
I_{CC5}	Operating Current (WRSR)	CS#=VCC		12	30	mA
I_{CC6}	Operating Current (SE)	CS#=VCC		12	30	mA
I_{CC7}	Operating Current (BE)	CS#=VCC		12	30	mA
I_{CC8}	Operating Current (CE)	CS#=VCC		12	30	mA
V_{IL}	Input Low Voltage		-0.5		0.2VCC	V
V_{IH}	Input High Voltage		0.7VCC		VCC+0.4	V
V_{OL}	Output Low Voltage	I_{OL} = 100μA			0.2	V
V_{OH}	Output High Voltage	I_{OH} = -100μA	VCC-0.2			V

Note:

1. Typical value at T_A = 25℃, VCC = 3.3V.
2. Value guaranteed by design and/or characterization, not 100% tested in production.

(T_A = -40℃~125℃, VCC=2.7~3.6V)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit.
I_{LI}	Input Leakage Current				±2	μA
I_{LO}	Output Leakage Current				±2	μA
I_{CC1}	Standby Current	CS#=VCC, VIN=VCC or VSS		16	250	μA
I_{CC2}	Deep Power-Down Current	CS#=VCC, VIN=VCC or VSS		1	80	μA
I_{CC3}	Operating Current (Read)	CLK=0.1VCC / 0.9VCC at 133MHz, Q=Open(x4 I/O)		14	40	mA
		CLK=0.1VCC / 0.9VCC at 80MHz, Q=Open(x4 I/O)		12	30	mA
		CLK=0.1VCC / 0.9VCC at 84MHz DTR, Q=Open(x4 I/O)		16	35	mA
I_{CC4}	Operating Current (PP)	CS#=VCC		12	30	mA
I_{CC5}	Operating Current (WRSR)	CS#=VCC		12	30	mA
I_{CC6}	Operating Current (SE)	CS#=VCC		12	30	mA
I_{CC7}	Operating Current (BE)	CS#=VCC		12	30	mA
I_{CC8}	Operating Current (CE)	CS#=VCC		12	30	mA
V_{IL}	Input Low Voltage		-0.5		0.2VCC	V
V_{IH}	Input High Voltage		0.7VCC		VCC+0.4	V
V_{OL}	Output Low Voltage	I_{OL} = 100μA			0.2	V
V_{OH}	Output High Voltage	I_{OH} = -100μA	VCC-0.2			V

Note:

1. Typical value at T_A = 25℃, VCC = 3.3V.
2. Value guaranteed by design and/or characterization, not 100% tested in production.

9.6 AC Characteristics

(T_A = -40℃~85℃, VCC=2.7~3.6V)

Symbol	Parameter	Min.	Typ.	Max.	Unit.
f_{C1}	Serial Clock Frequency For: all commands except 03h, EDh			166	MHz
f_{C2}	Serial Clock Frequency For: DTR Quad I/O Fast Read (EDh)			104	MHz
f_R	Serial Clock Frequency For: Read (03h)			80	MHz
t_{CLH}	Serial Clock High Time	45% ($1/Fc_{Max}$)			ns
t_{CLL}	Serial Clock Low Time	45% ($1/Fc_{Max}$)			ns
t_{CLCH}	Serial Clock Rise Time (Slew Rate)	0.2			V/ns
t_{CHCL}	Serial Clock Fall Time (Slew Rate)	0.2			V/ns
t_{SLCH}	CS# Active Setup Time	5			ns
t_{CHSH} t_{CLSH}	CS# Active Hold Time	5			ns
t_{SHCH}	CS# Not Active Setup Time	5			ns
t_{CHSL}	CS# Not Active Hold Time	5			ns
t_{SHSL}	CS# High Time (Read/Write)	20			ns
t_{SHQZ}	Output Disable Time			6	ns
t_{CLQX} t_{CHQX}	Output Hold Time	1.2			ns
t_{DVCH} t_{DVCL}	Data In Setup Time	2			ns
t_{CHDX} t_{CLDX}	Data In Hold Time	2			ns
t_{CLQV}	Clock Low To Output Valid (30pF)			7	ns
t_{CHQV}	Clock Low To Output Valid (10pF)			5	ns
t_{ECSV}	ECS# Setup Time			10	ns
t_{DP}	CS# High To Deep Power-Down Mode			3	μs
t_{RES1}	CS# High To Standby Mode Without Electronic Signature Read			30	μs
t_{RES2}	CS# High To Standby Mode With Electronic Signature Read			30	μs
t_{SUS}	CS# High To Next Command After Suspend			20	μs
t_{RS}(3)	Latency Between Resume And Next Suspend	100			μs
t_{RST}	CS# High To Next Command After Reset (Except From Erase)			30	μs
t_{RST_E}	CS# High To Next Command After Reset (From Erase)			12	ms
t_W	Write Status Register Cycle Time		5	25	ms

t_{BP}	Byte Program Time (First Byte)		40	150	μs
t_{PP}	Page Programming Time		0.25	3	ms
t_{SE}	Sector Erase Time		30	600	ms
t_{BE1}	Block Erase Time (32K Bytes)		0.12	1.5	s
t_{BE2}	Block Erase Time (64K Bytes)		0.15	2	s
t_{CE}	Chip Erase Time (GD25F128F)		35	150	s

Note:

1. Typical value at T_A = 25℃.
2. Value guaranteed by design and/or characterization, not 100% tested in production.
3. Minimum timing must be observed before issuing the next suspend command, and a period equal to or longer than the minimum timing is required in order for the program or erase operation to make progress, but the operation time may exceed the maximum value.

(T_A = -40℃~105℃, VCC=2.7~3.6V)

Symbol	Parameter	Min.	Typ.	Max.	Unit.
f_{C1}	Serial Clock Frequency For: all commands except 03h, EDh			166	MHz
f_{C2}	Serial Clock Frequency For: DTR Quad I/O Fast Read (EDh)			104	MHz
f_R	Serial Clock Frequency For: Read (03h)			80	MHz
t_{CLH}	Serial Clock High Time	45% (1/Fc_{Max})			ns
t_{CLL}	Serial Clock Low Time	45% (1/Fc_{Max})			ns
t_{CLCH}	Serial Clock Rise Time (Slew Rate)	0.2			V/ns
t_{CHCL}	Serial Clock Fall Time (Slew Rate)	0.2			V/ns
t_{SLCH}	CS# Active Setup Time	5			ns
t_{CHSH} t_{CLSH}	CS# Active Hold Time	5			ns
t_{SHCH}	CS# Not Active Setup Time	5			ns
t_{CHSL}	CS# Not Active Hold Time	5			ns
t_{SHSL}	CS# High Time (Read/Write)	20			ns
t_{SHQZ}	Output Disable Time			6	ns
t_{CLQX} t_{CHQX}	Output Hold Time	1.2			ns
t_{DVCH} t_{DVCL}	Data In Setup Time	2			ns
t_{CHDX} t_{CLDX}	Data In Hold Time	2			ns
t_{CLQV}	Clock Low To Output Valid (30pF)			7	ns
t_{CHQV}	Clock Low To Output Valid (10pF)			5	ns
t_{ECSV}	ECS# Setup Time			10	ns
t_{DP}	CS# High To Deep Power-Down Mode			3	μs
t_{RES1}	CS# High To Standby Mode Without Electronic Signature Read			30	μs
t_{RES2}	CS# High To Standby Mode With Electronic Signature Read			30	μs
t_{SUS}	CS# High To Next Command After Suspend			20	μs
t_{RS}(3)	Latency Between Resume And Next Suspend	100			μs
t_{RST}	CS# High To Next Command After Reset (Except From Erase)			30	μs
t_{RST_E}	CS# High To Next Command After Reset (From Erase)			12	ms
t_W	Write Status Register Cycle Time		5	25	ms
t_{BP}	Byte Program Time (First Byte)		40	200	μs
t_{PP}	Page Programming Time		0.25	4	ms

t_{SE}	Sector Erase Time		30	800	ms
t_{BE1}	Block Erase Time (32K Bytes)		0.12	2	s
t_{BE2}	Block Erase Time (64K Bytes)		0.15	4	s
t_{CE}	Chip Erase Time (GD25F128F)		35	300	s

Note:

1. Typical value at T_A = 25℃.
2. Value guaranteed by design and/or characterization, not 100% tested in production.
3. Minimum timing must be observed before issuing the next suspend command, and a period equal to or longer than the minimum timing is required in order for the program or erase operation to make progress, but the operation time may exceed the maximum value.

(T_A = -40℃~125℃, VCC=2.7~3.6V)

Symbol	Parameter	Min.	Typ.	Max.	Unit.
f_{C1}	Serial Clock Frequency For: all commands except 03h, EDh			133	MHz
f_{C2}	Serial Clock Frequency For: DTR Quad I/O Fast Read (EDh)			84	MHz
f_R	Serial Clock Frequency For: Read (03h)			80	MHz
t_{CLH}	Serial Clock High Time	45% (1/Fc_{Max})			ns
t_{CLL}	Serial Clock Low Time	45% (1/Fc_{Max})			ns
t_{CLCH}	Serial Clock Rise Time (Slew Rate)	0.2			V/ns
t_{CHCL}	Serial Clock Fall Time (Slew Rate)	0.2			V/ns
t_{SLCH}	CS# Active Setup Time	5			ns
t_{CHSH} t_{CLSH}	CS# Active Hold Time	5			ns
t_{SHCH}	CS# Not Active Setup Time	5			ns
t_{CHSL}	CS# Not Active Hold Time	5			ns
t_{SHSL}	CS# High Time (Read/Write)	20			ns
t_{SHQZ}	Output Disable Time			6	ns
t_{CLQX} t_{CHQX}	Output Hold Time	1.2			ns
t_{DVCH} t_{DVCL}	Data In Setup Time	2			ns
t_{CHDX} t_{CLDX}	Data In Hold Time	2			ns
t_{CLQV}	Clock Low To Output Valid (30pF)			7	ns
t_{CHQV}	Clock Low To Output Valid (10pF)			6	ns
t_{ECSV}	ECS# Setup Time			10	ns
t_{DP}	CS# High To Deep Power-Down Mode			3	μs
t_{RES1}	CS# High To Standby Mode Without Electronic Signature Read			30	μs
t_{RES2}	CS# High To Standby Mode With Electronic Signature Read			30	μs
t_{SUS}	CS# High To Next Command After Suspend			20	μs
t_{RS}(3)	Latency Between Resume And Next Suspend	100			μs
t_{RST}	CS# High To Next Command After Reset (Except From Erase)			30	μs
t_{RST_E}	CS# High To Next Command After Reset (From Erase)			12	ms
t_W	Write Status Register Cycle Time		5	25	ms
t_{BP}	Byte Program Time (First Byte)		40	200	μs
t_{PP}	Page Programming Time		0.25	4	ms

t_{SE}	Sector Erase Time		30	1000	ms
t_{BE1}	Block Erase Time (32K Bytes)		0.12	2	s
t_{BE2}	Block Erase Time (64K Bytes)		0.15	4	s
t_{CE}	Chip Erase Time (GD25F128F)		35	300	s

Note:

1. Typical value at T_A = 25℃.
2. Value guaranteed by design and/or characterization, not 100% tested in production.
3. Minimum timing must be observed before issuing the next suspend command, and a period equal to or longer than the minimum timing is required in order for the program or erase operation to make progress, but the operation time may exceed the maximum value.

Figure 49. Input Timing

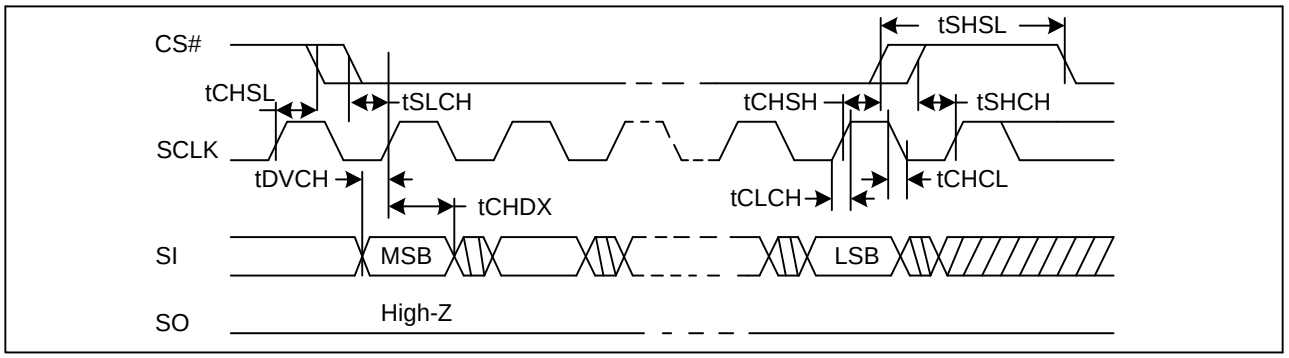


Figure 50. Output Timing

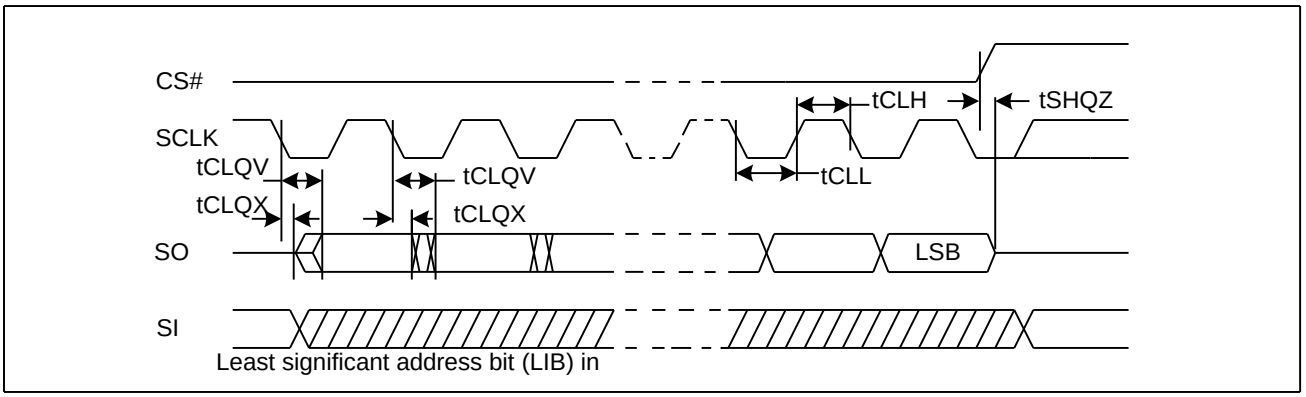


Figure 51. Serial Input Timing (DTR)

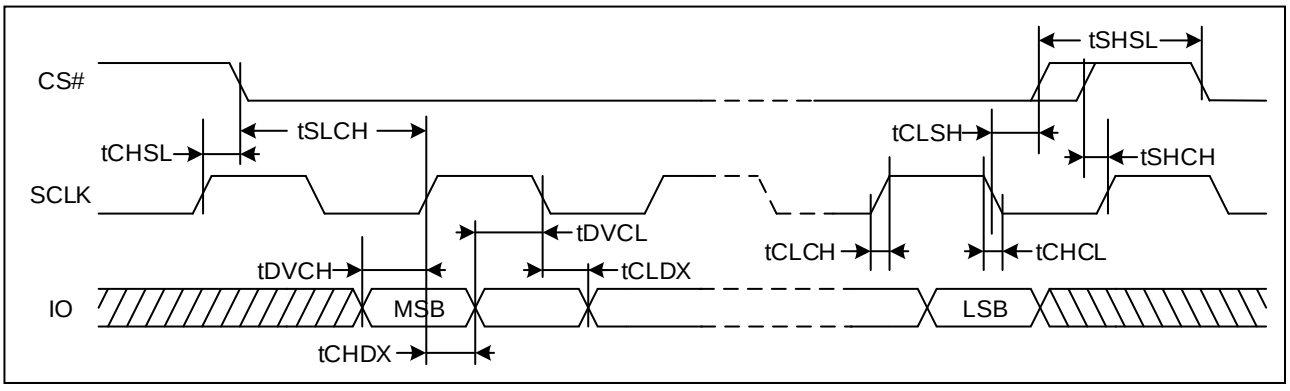


Figure 52. Serial Output Timing (DTR)

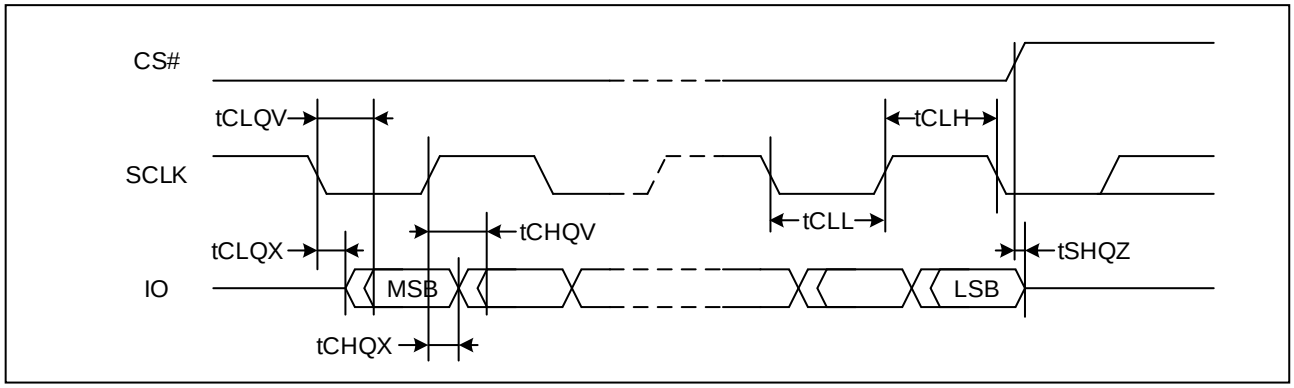


Figure 53. Resume to Suspend Timing Diagram

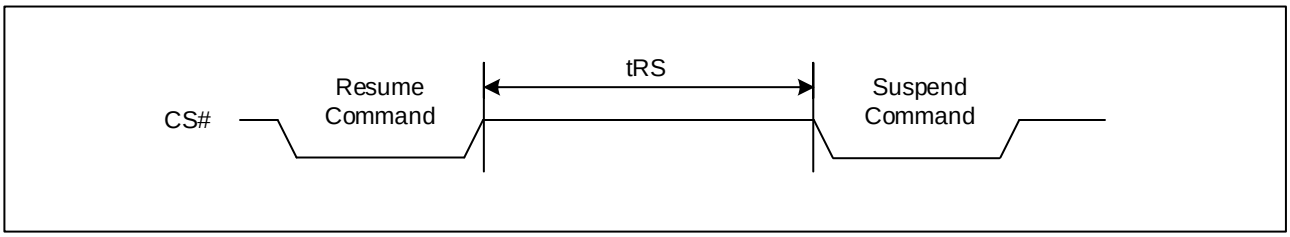


Figure 54 RESET# Timing

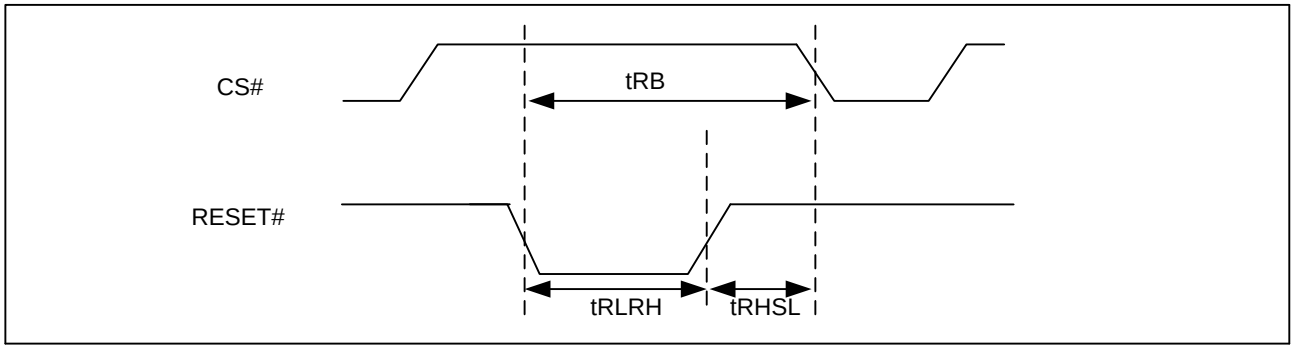


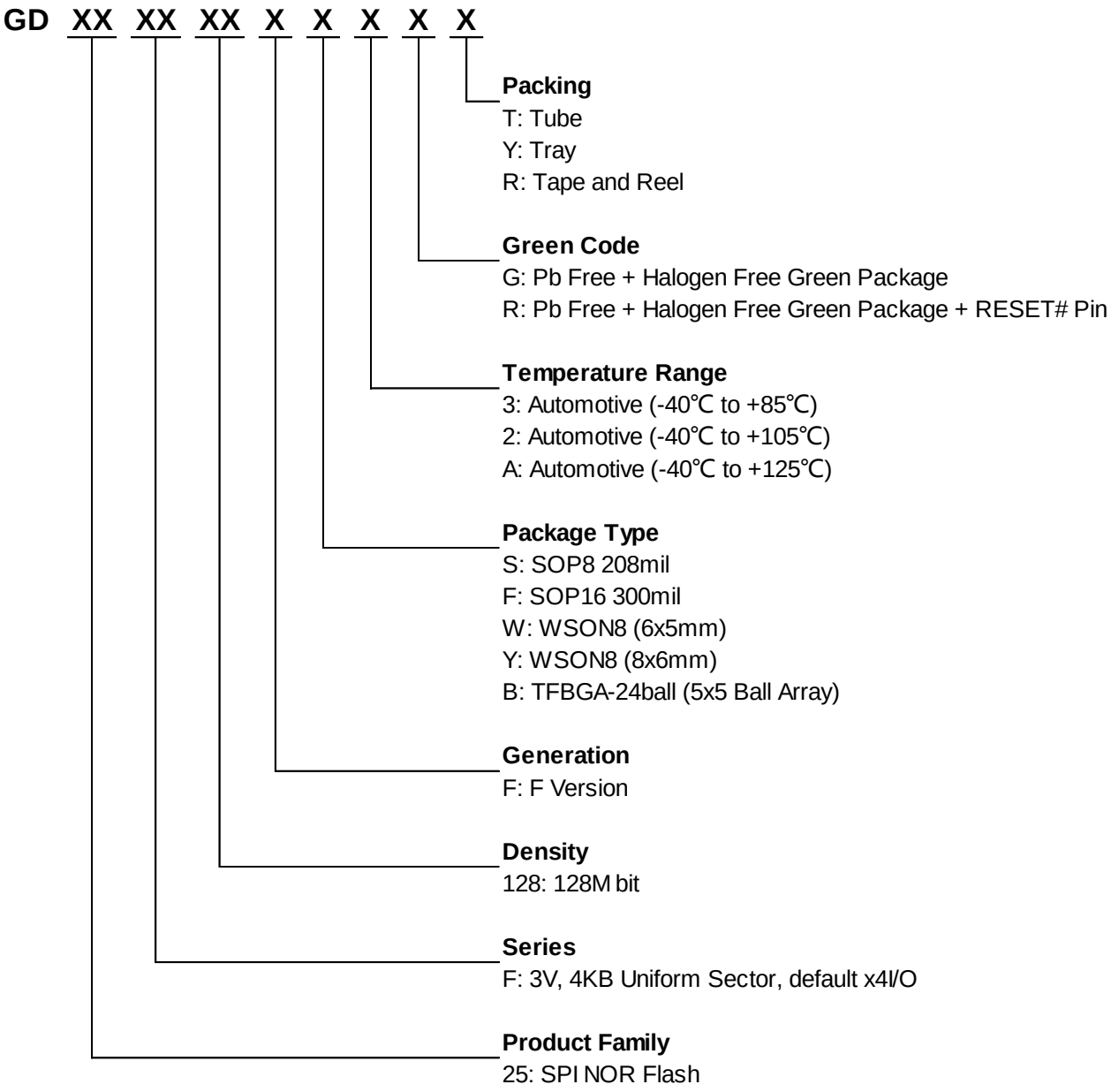
Table 14 Reset Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit.
tRLRH	Reset Pulse Width	1			μs
tRHSL	Reset Hold time before next Operation	50			ns
tRB	Reset Recovery Time			12	ms

Note:

1. The device need tRB (max) at most to get ready for all commands after RESET# low.

10 ORDERING INFORMATION



10.1 Valid Part Numbers

Please contact GigaDevice regional sales for the latest product selection and available form factors.

Temperature Range 3: Automotive (-40℃ to +85℃)

Product Number	Density	Package Type	Packing Options
GD25F128FS3G	128Mbit	SOP8 208mil	T/Y/R
GD25F128FF3R	128Mbit	SOP16 300mil	T/Y/R
GD25F128FW3G	128Mbit	WSON8 (6x5mm)	Y/R
GD25F128FY3G	128Mbit	WSON8 (8x6mm)	Y/R
GD25F128FB3R	128Mbit	TFBGA-24ball (5x5 Ball Array)	Y/R

Temperature Range 2: Automotive (-40℃ to +105℃)

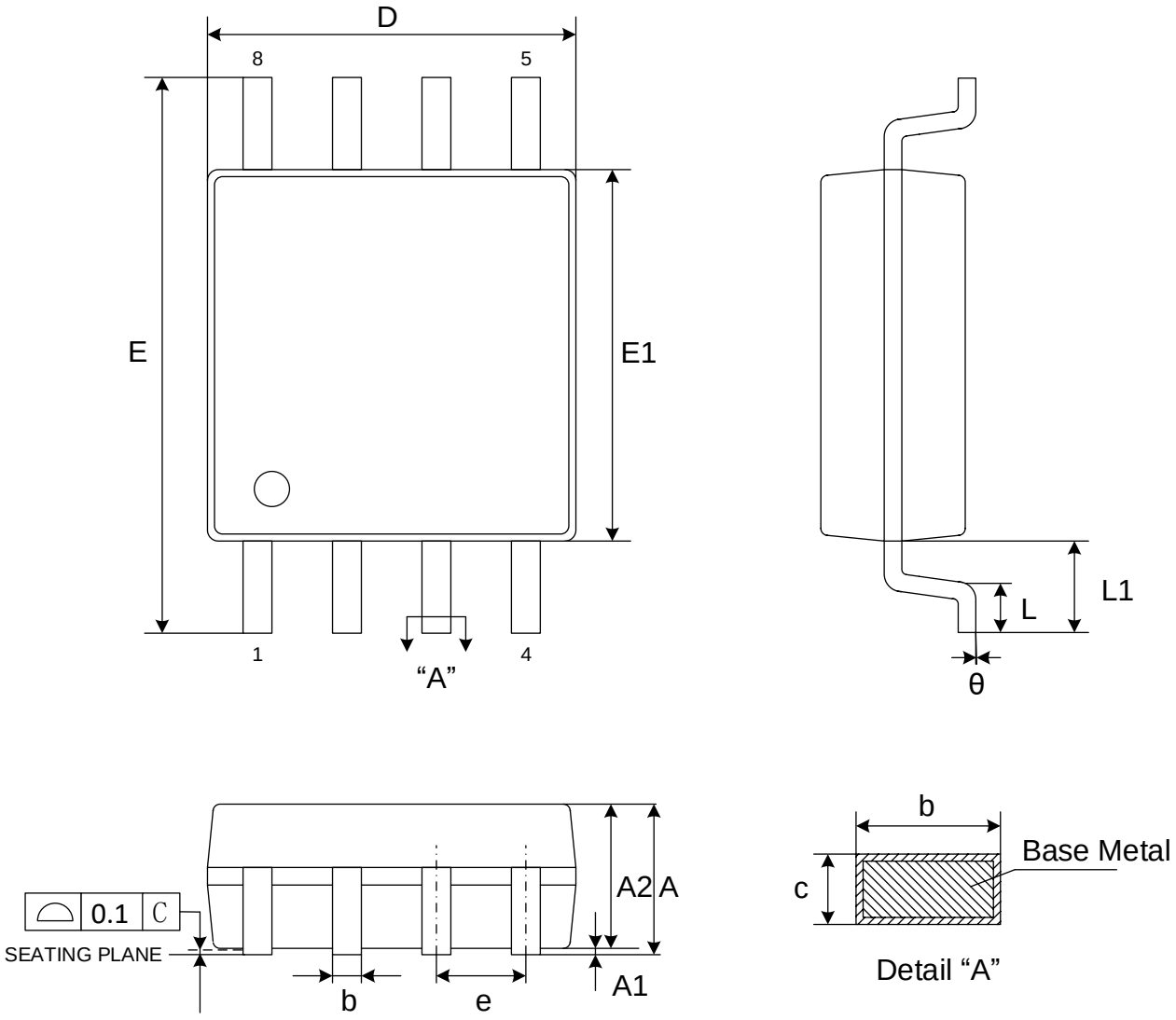
Product Number	Density	Package Type	Packing Options
GD25F128FS2G	128Mbit	SOP8 208mil	T/Y/R
GD25F128FF2R	128Mbit	SOP16 300mil	T/Y/R
GD25F128FW2G	128Mbit	WSON8 (6x5mm)	Y/R
GD25F128FY2G	128Mbit	WSON8 (8x6mm)	Y/R
GD25F128FB2R	128Mbit	TFBGA-24ball (5x5 Ball Array)	Y/R

Temperature Range A: Automotive (-40℃ to +125℃)

Product Number	Density	Package Type	Packing Options
GD25F128FSAG	128Mbit	SOP8 208mil	T/Y/R
GD25F128FFAR	128Mbit	SOP16 300mil	T/Y/R
GD25F128FWAG	128Mbit	WSON8 (6x5mm)	Y/R
GD25F128FYAG	128Mbit	WSON8 (8x6mm)	Y/R
GD25F128FBAR	128Mbit	TFBGA-24ball (5x5 Ball Array)	Y/R

11 PACKAGE INFORMATION

11.1 Package SOP8 208MIL



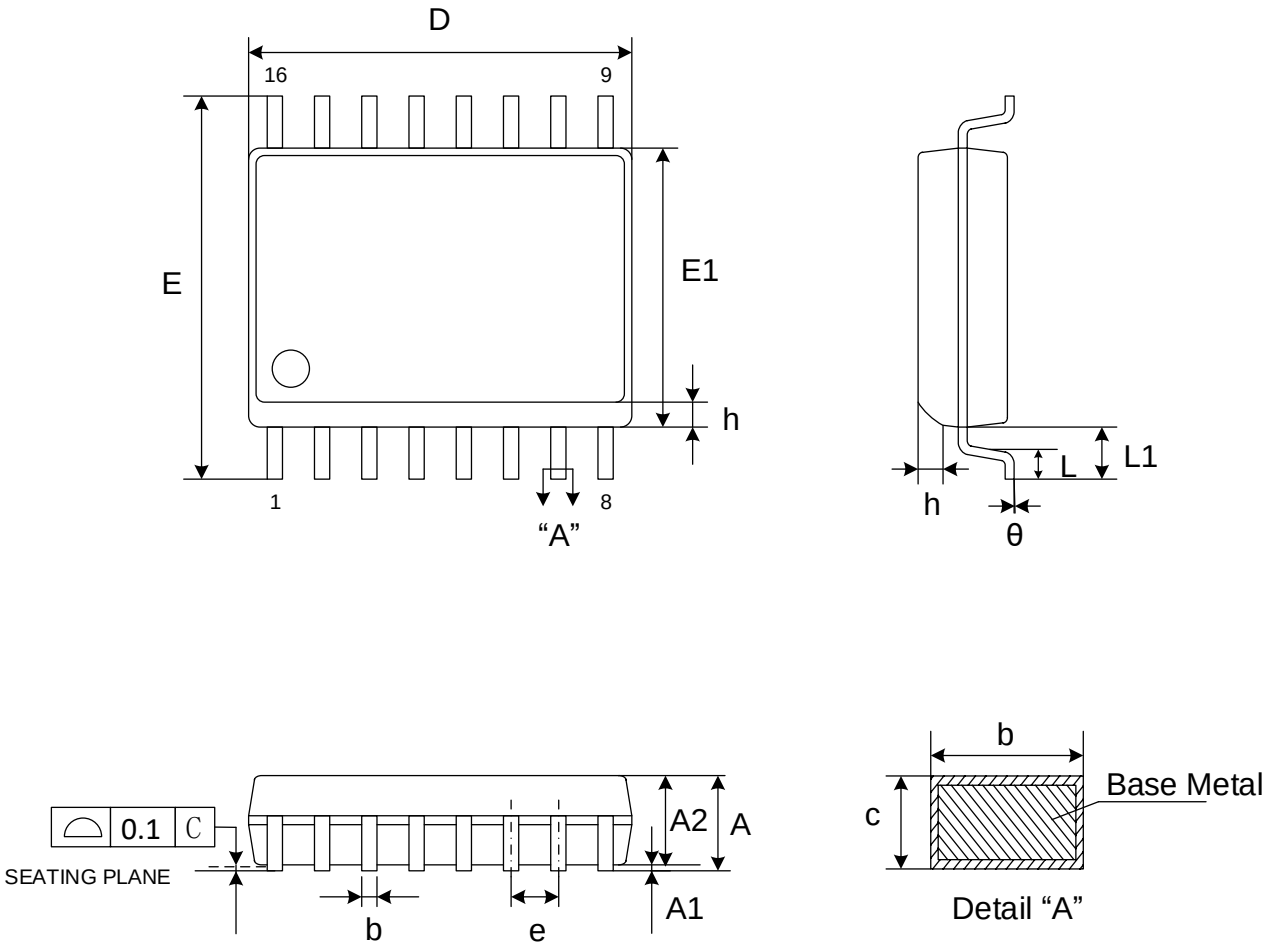
Dimensions

Symbol / Unit		A	A1	A2	b	c	D	E	E1	e	L	L1	θ
mm	Min	-	0.05	1.70	0.31	0.15	5.13	7.70	5.18	1.27	0.50	1.31	0°
	Nom	-	0.15	1.80	0.41	0.20	5.23	7.90	5.28		-		-
	Max	2.16	0.25	1.90	0.51	0.25	5.33	8.10	5.38		0.85		8°

Note:

1. Both the package length and width do not include the mold flash.

11.2 Package SOP16 300MIL



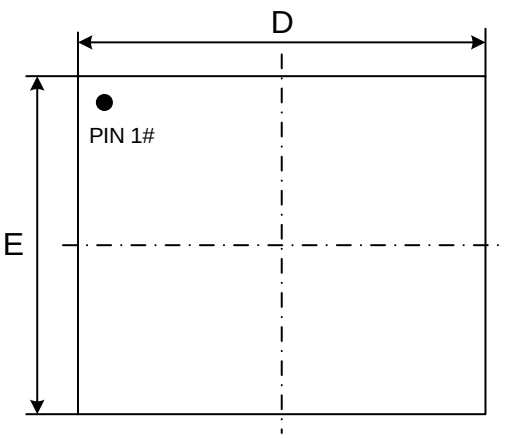
Dimensions

Symbol / Unit		A	A1	A2	b	c	D	E	E1	e	L	L1	h	θ
mm	Min	-	0.10	2.05	0.31	0.10	10.20	10.10	7.40	1.27	0.40	1.40	0.25	0
	Nom	-	0.20	-	0.41	0.25	10.30	10.30	7.50		-		-	-
	Max	2.65	0.30	2.55	0.51	0.33	10.40	10.50	7.60		1.27		0.75	8

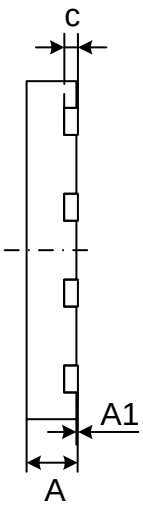
Note:

1. Both the package length and width do not include the mold flash.

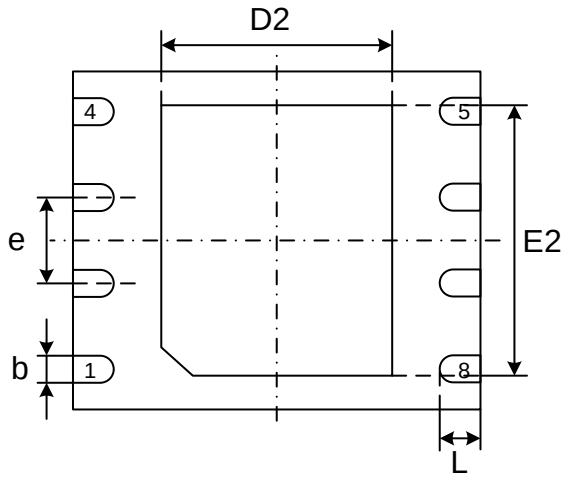
11.3 Package WSON8 (6x5mm)



Top View



Side View



Bottom View

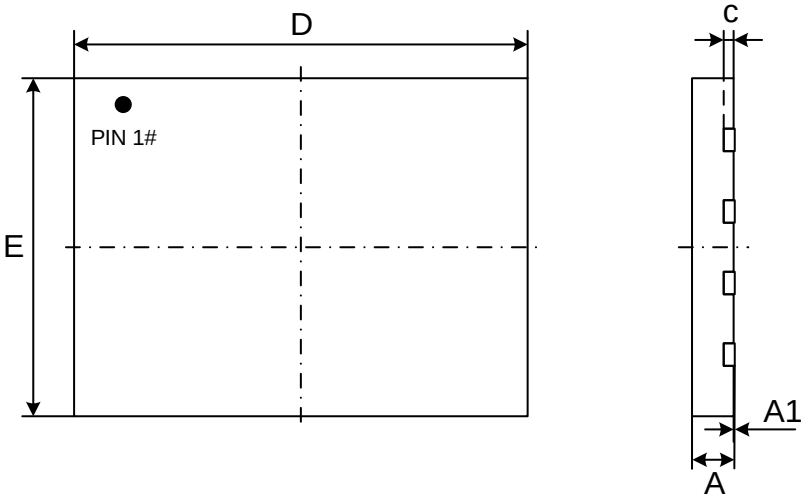
Dimensions

Symbol / Unit		A	A1	c	b	D	D2	E	E2	e	L
mm	Min	0.70	0.00	0.180	0.35	5.90	3.30	4.90	3.90	1.27	0.50
	Nom	0.75	0.02	0.203	0.40	6.00	3.40	5.00	4.00		0.60
	Max	0.80	0.05	0.250	0.50	6.10	3.50	5.10	4.10		0.75

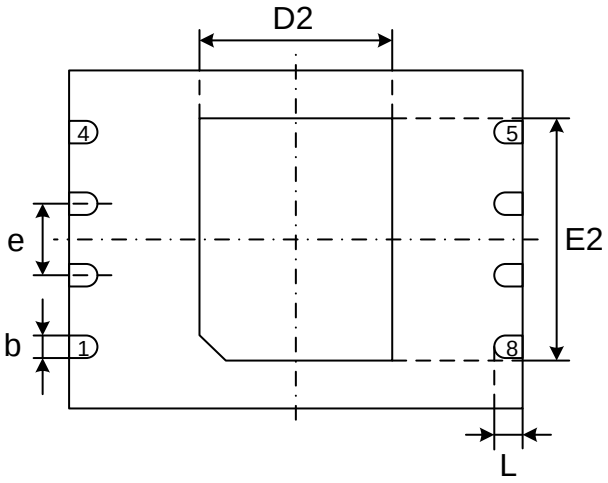
Note:

1. The exposed metal pad area on the bottom of the package is not connected to any internal signal. It is OK to connect it to the system ground (GND) or leave it floating.
2. Coplanarity ≤0.08mm. Package edge tolerance≤0.10mm.
3. The lead shape may be of little difference according to different package lead frames. These lead shapes are compatible with each other.

11.4 Package WSON8 (8x6mm)



Top View Side View



Bottom View

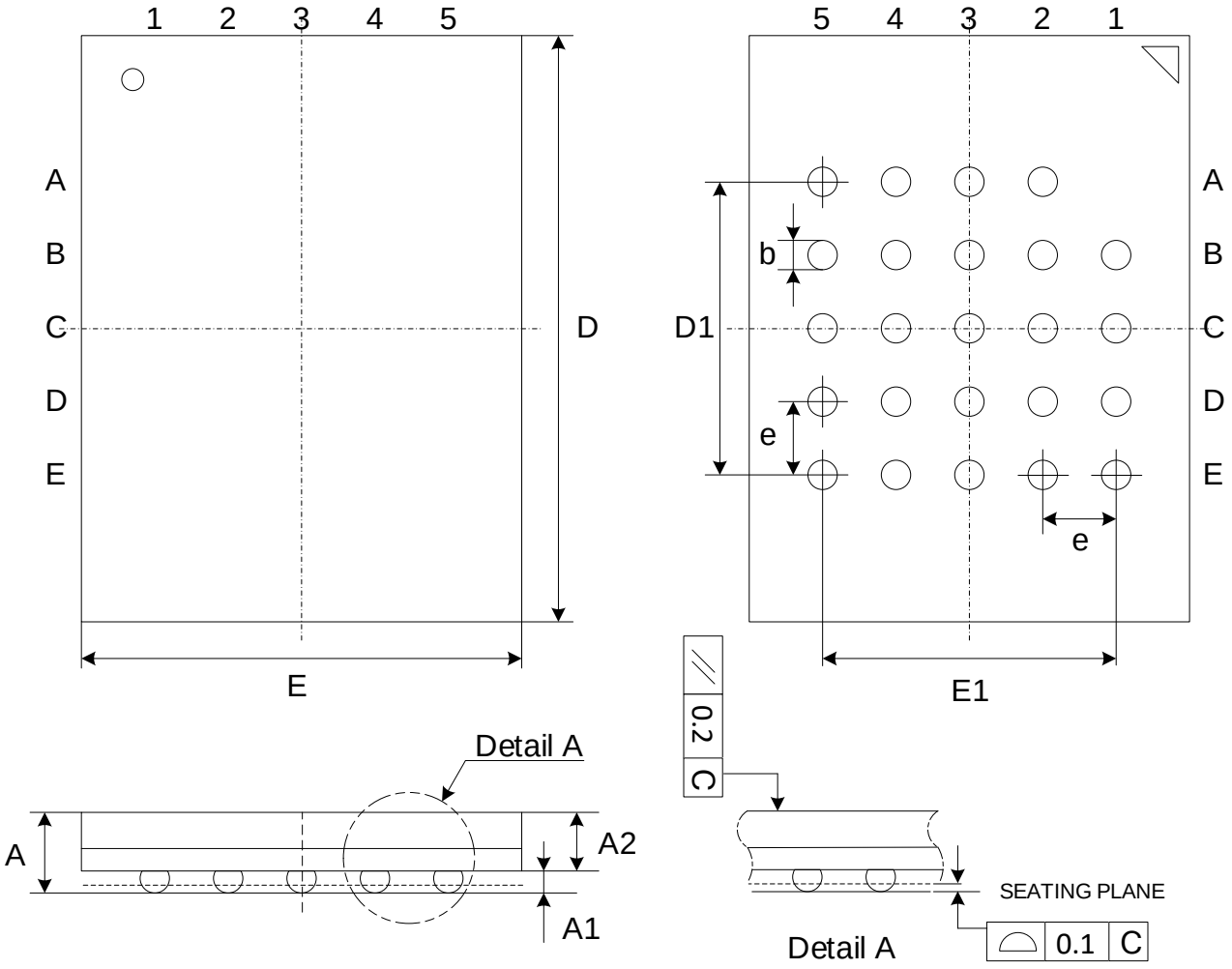
Dimensions

Symbol / Unit		A	A1	c	b	D	D2	E	E2	e	L
mm	Min	0.70	0.00	0.180	0.35	7.90	3.30	5.90	4.20	1.27	0.45
	Nom	0.75	0.02	0.203	0.40	8.00	3.40	6.00	4.30		0.50
	Max	0.80	0.05	0.250	0.45	8.10	3.50	6.10	4.40		0.55

Note:

1. The exposed metal pad area on the bottom of the package is not connected to any internal signal. It is OK to connect it to the system ground (GND) or leave it floating.
2. Coplanarity ≤0.08mm. Package edge tolerance≤0.10mm.
3. The lead shape may be of little difference according to different package lead frames. These lead shapes are compatible with each other.

11.5 Package TFBGA-24BALL (5x5 ball array)



Dimensions

Symbol / Unit		A	A1	A2	b	E	E1	D	D1	e
mm	Min	-	0.25	-	0.35	5.90	4.00	7.90	4.00	1.00
	Nom	-	0.30	0.80	0.40	6.00		8.00		
	Max	1.20	0.35	-	0.45	6.10		8.10		

12 REVISION HISTORY

Version No	Description	Page	Date
1.0	Initial release	All	2022-2-15
1.1	Update description of 56h Update DTR Quad I/O Fast Read Sequence Diagram Update note of WSON8 (6x5) and WSON8 (8x6) Remove min/max value of BGA(Dimensions) A2, remove Note of BGA	P27 P33 P63, 64 P65	2023-3-29
1.2	Add Note of IO2 and IO3 Modify ECS bit Description Add t_{CLSH}/t_{CHQX}/t_{DVCL}/t_{CLDX} in AC Characteristics Remove t_{BP2} from AC Characteristics	P5-8 P19 P52-56 P52-56	2023-8-23
1.3	Modify Description of Data Protection Modify Description of ECC Operation Add Description of ECS# Pin Modify Description of SUS bits Modify Power-On Timing and Add VPWD and tPWD Add t_{ECSV} in AC Characteristics Update Note1 of WSON8 Package Add “Detail A” of TFBGA-24Ball Package POD	P13 P14 P15 P17 P48 P53, 55, 57 P65-66 P67	2024-7-19

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