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Motorcomm

Motorcomm YT8531(D)H-CA / YT8531(D)C-CA/ YT8531P-CA Datasheet

INTEGRATED 10/100/1000 GIGABIT ETHERNET TRANSCEIVER

VERSION V1.01
DATE 2023-06-14

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Revision History

Revision	Release Date	Summary
V1.00	2023/04/03	First version.
V1.01	2023/06/14	Modify the description of power noise in chapter 8.6.

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1. General Description

The YT8531H / YT8531C / YT8531DH / YT8531DC / YT8531P is a highly integrated Ethernet transceiver that complies with 10BASE-Te, 100BASE-TX, and 1000BASE-T IEEE 802.3 standards. It provides all the necessary physical layer functions to transmit and receive Ethernet packets over CAT.5E UTP cable.

The YT8531(D)(P) uses state-of-the-art DSP technology and an Analog Front End (AFE) to enable high-speed data transmission and reception over UTP cable. Functions such as Crossover Detection & Auto-Correction, polarity correction, adaptive equalization, cross-talk cancellation, echo cancellation, timing recovery, and error correction are implemented in the YT8531(D)(P) to provide robust transmission and reception capabilities at 10Mbps, 100Mbps, or 1000Mbps.

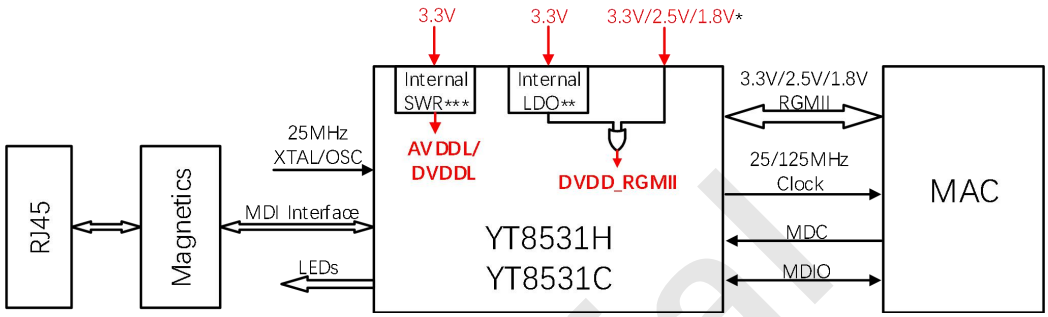
Data transfer between MAC and PHY is via the Reduced Gigabit Media Independent Interface (RGMII) for 1000BASE-T, 100BASE-TX and 10BASE-Te. The YT8531(D)(P) supports various RGMII signaling voltages, including 3.3V, 2.5V, and 1.8V.

The YT8531D/YT8531P features a Motorcomm proprietary feature called LRE100-4, which enables the device to auto-negotiate and link up with LRE100-4 compliant link partners in extended cable reach applications up to 400 meter at 100Mbps over CAT.5E cable.

1.1. TARGET APPLICATIONS

- DTV (Digital TV)
- MAU (Media Access Unit)
- CNR (Communication and Network Riser)
- Game Console
- Printer and Office Machine
- DVD Player and Recorder
- Ethernet Hub
- Ethernet Switch
- Base Stations and Controllers
- Routers, DSLAMs, PON Equipment
- Test and Measurement Systems
- Industrial and Factory Automation Equipment
- Multimedia synchronization and Real Time Networking
- Any embedded system with an Ethernet MAC that needs a UTP physical connection.

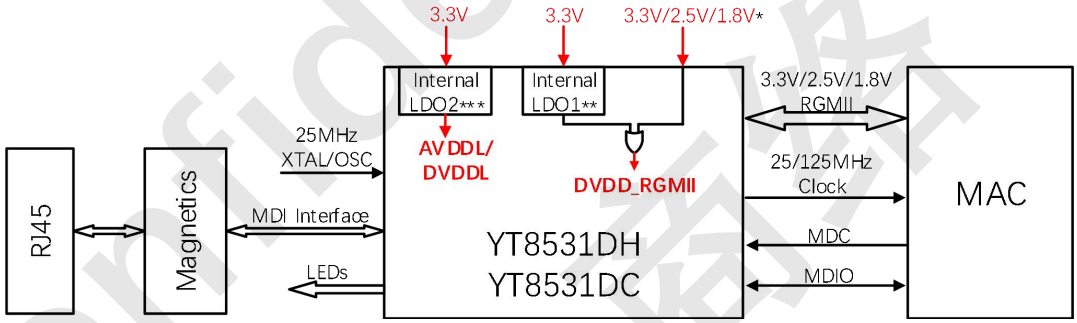
1.2. Application Diagram - YT8531H/YT8531C



**Note: 3.3V/2.5V/1.8V power here means I/O power sourced from external power, not from the internal LDO.*
***Note: I/O power only support 2.5V/1.8V when sourced from the internal LDO.*
****Note: Internal SWR is for YT8531H/YT8531C.*

Figure 1. Application Diagram - YT8531H/YT8531C

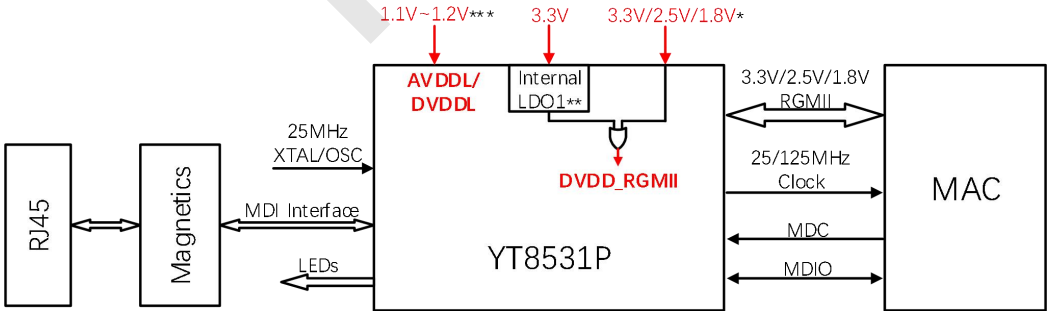
1.3. Application Diagram - YT8531DH/YT8531DC



**Note: 3.3V/2.5V/1.8V power here means I/O power sourced from external power, not from the internal LDO.*
***Note: I/O power only support 2.5V/1.8V when sourced from the internal LDO.*
****Note: Internal LDO2 is for YT8531DH/YT8531DC.*

Figure 2. Application Diagram - YT8531DH/YT8531DC

1.4. Application Diagram - YT8531P



**Note: 3.3V/2.5V/1.8V power here means I/O power sourced from external power, not from the internal LDO.*
***Note: I/O power only support 2.5V/1.8V when sourced from the internal LDO.*
****Note: 1.1V~1.2V means core power sourced from external power for YT8531P.*

Figure 3. Application Diagram - YT8531P

2. Features

- 1000BASE-T IEEE 802.3ab Compliant
- 100BASE-TX IEEE 802.3u Compliant
- 10BASE-Te IEEE 802.3 Compliant
- Support LRE100-4 for YT8531D/YT8531P
  - Long Reach Ethernet up to 400 meter @100Mbps by 4-pairs in the CAT.5E UTP cable
- Supports RGMII
- Supports IEEE 802.3az-2010 (Energy Efficient Ethernet)
- Supports Synchronous Ethernet (Sync-E)
- Built-in Wake-on-LAN (WOL) over UTP
- Supports interrupt function over UTP
- Supports Parallel Detection
- Crossover Detection & Auto-Correction
- Automatic polarity correction
- Baseline Wander Correction
- Supports 120m for CAT.5E cable in 1000BASE-T
- Selectable 3.3V/2.5V/1.8V signaling for RGMII.
- Supports 25MHz external crystal or OSC
- Provides 25MHz/125MHz clock source for MAC
- Provides 3 network status LEDs
- Supports Link Down Power Saving (Sleep Mode)
- Built-in Switching Regulator or LDO
- Supports 18k bytes jumbo frame for 1000BASE-T and 100BASE-TX, and 10k bytes for 10BASE-Te
- Industrial grade manufacturing process for YT8531H and YT8531DH
- 40-pin QFN Green Package

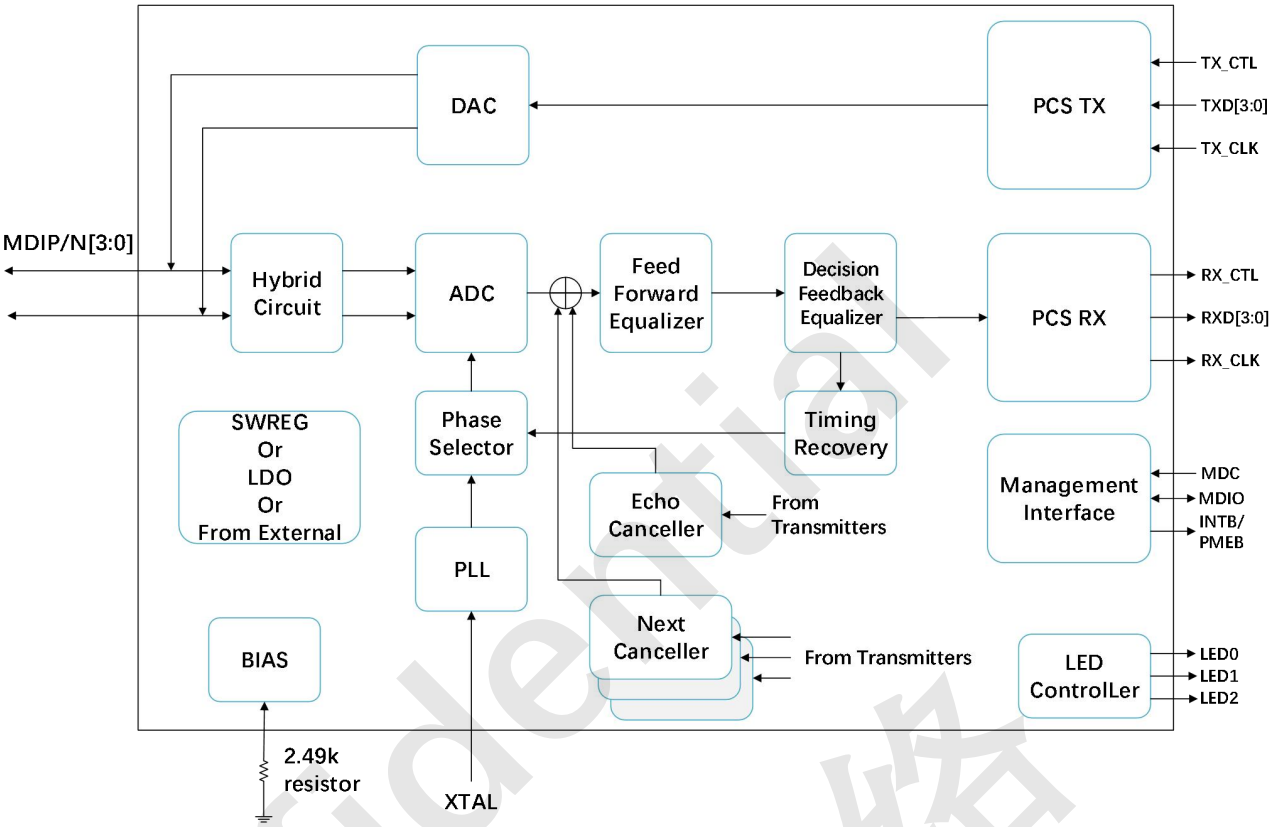
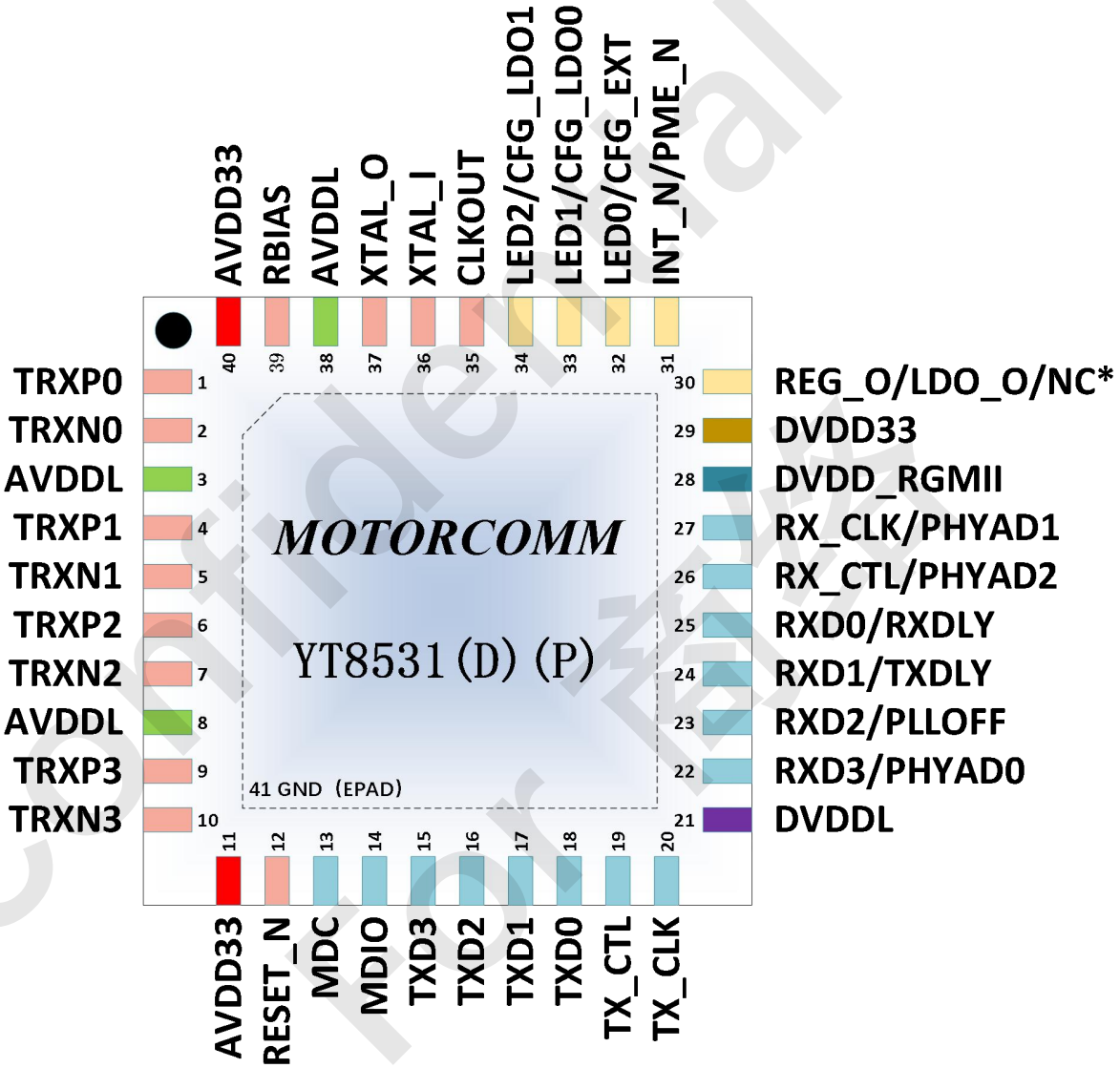


Figure 4. Block Diagram

3. Pin Assignment

3.1. YT8531(D)(P) QFN40



**Note:*
For YT8531H/YT8531C, pin 30 is REG_O, which means switch regulator output.
For YT8531DH/YT8531DC, pin 30 is LDO_O, which means LDO output.
For YT8531P, pin 30 is NC, which means no connection.

Figure 5. Pin Assignment Diagram

3.2. Pin Assignment

Some pins have multiple functions.
Refer to the Pin Assignment figures for a graphical representation.

- I: Input
- O: Output
- IO: Bidirectional Input and Output
- LI: Latched Input During Power UP
- P: Power
- PU: Internal pull up
- PD: Internal pull down
- G: Ground
- OD: Open Drain
- XT: Crystal Related

Table 1. Pin Assignment

No.	Pin Name	Type
1	TRXP0	IO
2	TRXN0	IO
3	AVDDL	P
4	TRXP1	IO
5	TRXN1	IO
6	TRXP2	IO
7	TRXN2	IO
8	AVDDL	P
9	TRXP3	IO
10	TRXN3	IO
11	AVDD33	P
12	RESET_N	I/PU
13	MDC	I/PD
14	MDIO	IO/PU
15	TXD3	I/PD
16	TXD2	I/PD
17	TXD1	I/PD
18	TXD0	I/PD
19	TX_CTL	I/PD
20	TX_CLK	I/PD

No.	Pin Name	Type
21	DVDDL	P
22	RXD3/PHYAD0	O/LI/PD
23	RXD2/PLLOFF	O/LI/PD
24	RXD1/TXDLY	O/LI/PD
25	RXD0/RXDLY	O/LI/PU
26	RX_CTL/PHYAD2	O/LI/PD
27	RX_CLK/PHYAD1	O/LI/PD
28	DVDD_RGMII	P
29	DVDD33	P
30	REG_O/LDO_O/NC	P
31	INT_N/PME_N	O/OD
32	LED0/CFG_EXT	O/LI/PU
33	LED1/CFG_LDO0	O/LI/PU
34	LED2/CFG_LDO1	O/LI/PD
35	CLKOUT	O
36	XTAL_I	XT
37	XTAL_O	XT
38	AVDDL	P
39	RBIAS	O
40	AVDD33	P
41	GND	G

3.3. Transceiver Interface

Table 2. Transceiver Interface

No.	Pin Name	Type	Description
1	TRXP0	IO	Media-dependent interface 0, 100Ω transmission line
2	TRXN0	IO	Media-dependent interface 0, 100Ω transmission line
4	TRXP1	IO	Media-dependent interface 1, 100Ω transmission line
5	TRXN1	IO	Media-dependent interface 1, 100Ω transmission line
6	TRXP2	IO	Media-dependent interface 2, 100Ω transmission line
7	TRXN2	IO	Media-dependent interface 2, 100Ω transmission line
9	TRXP3	IO	Media-dependent interface 3, 100Ω transmission line
10	TRXN3	IO	Media-dependent interface 3, 100Ω transmission line

3.4. Clock

Table 3. Clock

No.	Pin Name	Type	Description
35	CLKOUT	O	1. Reference Clock Generated from Internal PLL. This pin should be kept floating if the clock is not used by the MAC. 2. UTP recovery receive clock for Sync Ethernet. 3. 25MHz reference clock.
36	XTAL_I	XT	This pin is XTAL_I, means 25MHz Crystal Input pin. If use external oscillator or clock from another device. 1. When connect an external 25MHz oscillator or clock from another device to XTAL_O pin, XTAL_I must be shorted to GND. 2. When connect an external 25MHz oscillator or clock from another device to XTAL_I pin, keep the XTAL_O floating.
37	XTAL_O	XT	This pin is XTAL_O, means 25MHz Crystal Output pin. If use external oscillator or clock from another device. 1. When connect an external 25MHz oscillator or clock from another device to XTAL_O pin, XTAL_I must be shorted to GND. 2. When connect an external 25MHz oscillator or clock from another device to XTAL_I pin, keep the XTAL_O floating.

3.5. RGMII

Table 4. RGMII

No.	Pin Name	Type	Description
15	TXD3	I/PD	Transmit Data. Data is transmitted from MAC to PHY via TXD[3:0].
16	TXD2	I/PD	
17	TXD1	I/PD	
18	TXD0	I/PD	
19	TX_CTL	I/PD	Transmit Control Signal from the MAC.
20	TX_CLK	I/PD	The transmit reference clock will be 125Mhz, 25MHz, or 2.5MHz depending on speed.
22	RXD3	O/LI/PD	Receive Data. Data is transmitted from PHY to MAC via RXD[3:0].
23	RXD2	O/LI/PD	
24	RXD1	O/LI/PD	
25	RXD0	O/LI/PU	
26	RX_CTL	O/LI/PD	Receive Control Signal to the MAC.

27	RX_CLK	O/LI/PD	The continuous receive reference clock will be 125MHz, 25MHz, or 2.5MHz, and is derived from the received data stream.

3.6. Reset

Table 5. Reset

No.	Pin Name	Type	Description
12	RESET_N	I/PU	Hardware reset, active low. Requires an external pull-up resistor

3.7. Mode Selection

Table 6. Mode Selection

No.	Name	Type	Description
22	PHYAD0	O/LI/PD	PHYAD[2:0]. PHY address configuration.
27	PHYAD1	O/LI/PD	
26	PHYAD2	O/LI/PD	
23	PLLOFF	O/LI/PD	In sleep mode, PLL off configuration.
24	TXDLY	O/LI/PD	RGMII Transmit clock timing control. Pull up to add delay to TXC for TXD latching.
25	RXDLY	O/LI/PU	RGMII receiver clock timing control Pull-up to add 2ns delay on RX_CLK when RX_CLK is 125MHz or, to add 8ns delay on RX_CLK when RX_CLK is 25MHz/2.5MHz, which shall be used to latch RXD.
32	CFG_EXT	O/LI/PU	I/O Pad. External Power Source Mode Configuration. Pull up to use the external power source for the I/O pad. Pull down to use the integrated LDO to transform the desired voltage for the I/O pad.
33	CFG_LDO0	O/LI/PU	CFG_LDO[1:0]. When pulling down CFG_EXT pin, CFG_LDO[1:0] represent internal LDO output voltage setting for I/O pad: 2'b00: Reserved 2'b01: 2.5V 2'b10 or 2b'11: 1.8V When pulling up CFG_EXT pin, CFG_LDO[1:0] stand for input voltage selection of external power for I/O pad: 2'b00: 3.3V 2'b01: 2.5V 2'b10 or 2b'11: 1.8V
34	CFG_LDO1	O/LI/PD	

3.8. LED Default Settings

Table 7. LED Default Settings

No.	Pin Name	Type	Description
32	LED0	O/LI/PU	Light = Link up at 10Mbps Blinking = Transiting or Receiving
33	LED1	O/LI/PU	Light = Link up at 100Mbps Blinking = Transiting or Receiving

34	LED2	O/LI/PD	Light = Link up at 1000Mbps Blinking = Transiting or Receiving

3.9. Regulator and Reference

Table 8. Regulator and Reference

No.	Pin Name	Type	Description
39	RBIAS	O	Bias Resistor. An external 2.49 kΩ±1% resistor must be connected between the RBIAS pin and GND
30	REG_O	P/O	Switch regulator 1.1V output.Connect to an external 2.2 uH power inductor directly. Only for YT8531H/YT8531C.
	LDO_O	P/O	Low-dropout regulator 1.1V output. Only for YT8531DH/YT8531DC.
	NC	-	No connection. Only for YT8531P.

3.10. Power Related

Table 9. Power Related

No.	Pin Name	Type	Description
29	DVDD33	P	3.3V Power Digital non-RGMII I/O power
28	DVDD_RGMII	P	Digital RGMII I/O, MDC/MDIO power, adjusted by CFG_EXT and CFG_LDO[1:0]. *Note: When CFG_EXT = 0 and CFG_LDO[1:0] = 2b'01 or 2b'10 or 2b'11, the I/O pad power is supplied from the internal LDO. Otherwise, it is supplied from the external power connected to DVDD_RGMII pin. No matter whether the I/O pad power form external or internal, a bulk capacitor and a decoupling capacitor should be connected to this pin.*
21	DVDDL	P	Digital power 1.1V/1.2V
11, 40	AVDD33	P	Analog Power 3.3V
3, 8, 38	AVDDL	P	Analog power 1.1V/1.2V
41	GND	G	Exposed PAD

3.11. Management

Table 10. Management

No.	Pin Name	Type	Description
13	MDC	I/PD	Management Data Clock.
14	MDIO	IO/PU	Input/Output of Management Data. Pull up 3.3V/2.5V/1.8V for 3.3V/2.5V/1.8V I/O respectively
31	INT_N/PME_N	O/OD	This pin is shared by two functions, the default pin setting is INT_N. Keep this pin floating if either of the functions is not used. The pin type depends on function selected: 1. Interrupt (should be 3.3V pulled up). Set low if the specified events occurred; active low. 2. Power Management Event (should be 3.3V pulled up). Set low if received a magic packet; active low.

			Note 1: The behavior of INT_N is level-triggered, the behavior of PME_N is level-triggered or pulse-triggered which is controled by EXT 0xA00A bit[0]. *Note 2: The function of INT_N/PME_N can be assigned by Ext 0xa00a bit[6].* *1: Pin 31 functions as PME_N.* *0: Pin 31 functions as INT_N (default).*

4. Function Description

4.1. UTP<->RGMII Application

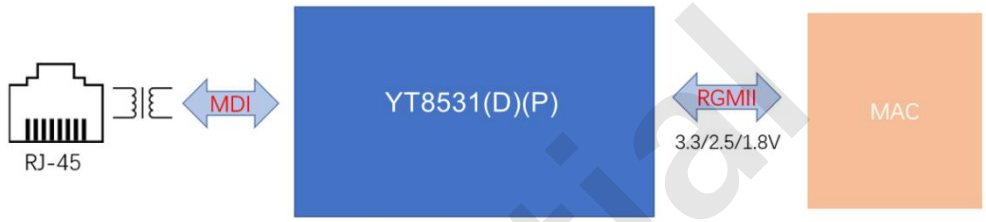


Figure 6. UTP<->RGMII ApplicationTransmit Functions

4.2. Transmit Functions

4.2.1. Transmit Encoder Modes

4.2.1.1. 1000BASE-T

In 1000BASE-T mode, the YT8531(D)(P) scrambles transmit data bytes from the MAC interfaces to 9-bit symbols and encodes them into 4D five-level PAM signals over the four pairs of CAT.5E UTP cable.

4.2.1.2. 100BASE-TX

In 100BASE-TX mode, 4-bit data from the MII is 4B/5B serialized, scrambled, and encoded to a three-level MLT3 sequence transmitted by the PMA.

4.2.1.3. 10BASE-Te

In 10BASE-Te mode, the YT8531(D)(P) transmits and receives Manchester-encoded data.

4.3. Receive Functions

4.3.1. Receive Decoder Modes

4.3.1.1. 1000BASE-T

In 1000BASE-T mode, the PMA recovers the 4D PAM signals after accounting for the cabling conditions such as skew among the four pairs, the pair swap order, and the polarity of the pairs. The resulting code group is decoded into 8-bit data values. Data stream delimiters are translated appropriately and data is output to the MAC interfaces.

4.3.1.2. 100BASE-TX

In 100BASE-TX mode, the receive data stream is recovered and descrambled to align to the symbol boundaries. The aligned data is then parallelized and 5B/ 4B decoded to 4-bit data. This output runs to MAC interfaces after data stream delimiters have been translated.

4.3.1.3. 10BASE-Te

In 10BASE-Te mode, the recovered 10BASE-Te signal is decoded from Manchester then aligned.

4.4. LRE100-4

YT8531D/YT8531P supports a Motorcomm proprietary feature called LRE100-4, the long reach Ethernet application up to 400m at 100Mbps data rate by 4-pairs in the CAT.5E UTP cable.

4.5. Echo Canceller

A hybrid circuit is used to transmit and receive simultaneously on each pair. A signal reflects back as an echo if the transmitter is not perfectly matched to the line. Other connector or cable imperfections, such as patch panel discontinuity and variations in cable impedance along the twisted pair cable, also result in drastic SNR degradation on the receive signal. The YT8531(D)(P) device implements a digital echo canceller to adjust for echo and is adaptive to compensate for the varied channel conditions.

4.6. NEXT Canceller

The 1000BASE-T physical layer uses all four pairs of wires to transmit data. Because the four twisted pairs are bundled together, significant high frequency crosstalk occurs between adjacent pairs in the bundle. The YT8531(D)(P) device uses three parallel NEXT cancellers on each receive channel to cancel high frequency crosstalk. The YT8531(D)(P) cancels NEXT by subtracting an estimate of these signals from the equalizer output.

4.7. Baseline Wander Canceller

Baseline wander results from Ethernet links that AC-couple to the transceivers and from AC coupling that cannot maintain voltage levels for longer than a short time. As a result, transmitted pulses are distorted, resulting in erroneous sampled values for affected pulses. Baseline wander is more problematic in the 1000BASE-T environment than in 100BASE-TX due to the DC baseline shift in the transmit and receive signals. The YT8531(D)(P) device uses an advanced baseline wander cancellation circuit that continuously monitors and compensates for this effect, minimizing the impact of DC baseline shift on the overall error rate.

4.8. Digital Adaptive Equalizer

The digital adaptive equalizer removes inter- symbol interference at the receiver. The digital adaptive equalizer takes unequalized signals from ADC output and uses a combination of feedforward equalizer (FFE) and decision feedback equalizer (DFE) for the best optimized signal-to-noise (SNR) ratio.

4.9. Management Interface

The Status and Control registers of the device are accessible through the MDIO and MDC serial interface. The functional and electrical properties of this management interface comply with IEEE 802.3, Section 22 and also support MDC clock rates up to 12.5 MHz.

4.10. Auto-Negoitation

The YT8531(D)(P) negotiates its operation mode using the auto negotiation mechanism according to IEEE 802.3 clause 28 over the copper media. Auto negotiation supports choosing the mode of operation automatically by comparing its own abilities and received abilities from link partner. The advertised abilities include:

- Speed: 10/100/1000Mbps
- Duplex mode: full duplex and/or half duplex

Auto negotiation is initialized when the following scenarios happen:

- Power-up/Hardware/Software reset
- Auto negotiation restart
- Transition from power down to power up
- Link down

Auto negotiation is enabled for YT8531(D)(P) by default, and can be disabled by software control.

4.11. LDS (Link Discover Signaling)

YT8531D/YT8531P supports long range ethernet (LRE), which uses link discoverr signaling (LDS) instead of auto negotiation since the extended cable reach attenuates the auto negotiation link pulses. LDS is an extended reach signaling scheme and protocol, which is used to:

- Master/Slave assignment
- Estimate cable length
- Confirm pair number and pair connectivity ordering
- Choose highest common operation mode

IEEE-compliant PHYs will ignore LDS signal since its frequency is less than 2MHz according to IEEE802.3 clause 14. If the link partner is an IEEE legacy ethernet PHY, YT8531D/YT8531P can detect the standard NLP, FLP, or MLT-3 IDLE signal, and then transits LDS mode into Clause 28 auto negotiation mode.

Forcing pair number and speed mode is also supported. The same forcing must be done at both ends of the link. By default the LDS is disabled, and should be enabled before using this feature.

4.12. Polarity Detection and Auto Correction

YT8531(D)(P) can detect and correct two types of cable errors: swapping of pairs within the UTP cable (swapping between pair 0 and pair 1, and(or) swapping between pair 2 and pair 3) and swapping of wires within a pair.

4.13. Loopback Mode

There are three loopback modes in YT8531(D)(P)

4.13.1. Digital Loopback

Digital loopback provides the ability to loop transmitted data back to the receiver using digital circuitry in YT8531(D)(P).

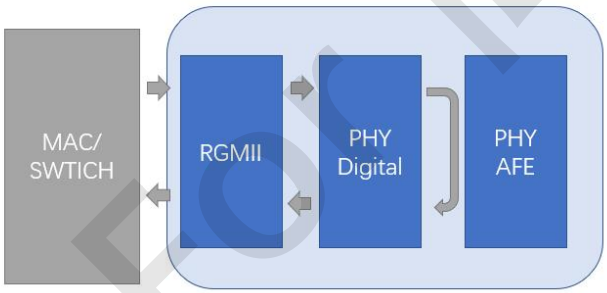


Figure 7. Digital Loopback

4.13.2. External loopback

External cable loopback loops Tx to Rx through a complete digital and analog path and an external cable, thus testing all the digital data paths and all the analog circuits. Figure shows a block diagram of external cable loopback.

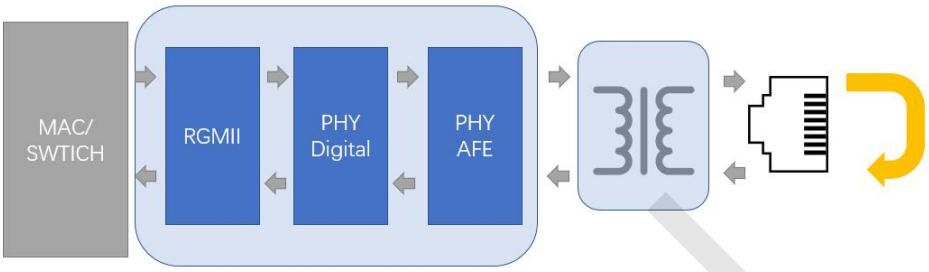


Figure 8. External Loopback

4.13.3. Remote PHY loopback

The Remote loopback connects the MDI receive path to the MDI transmit path, near the RGMII interface, thus the remote link partner can detect the connectivity in the resulting loop. Figure below, shows the path of the remote loopback.

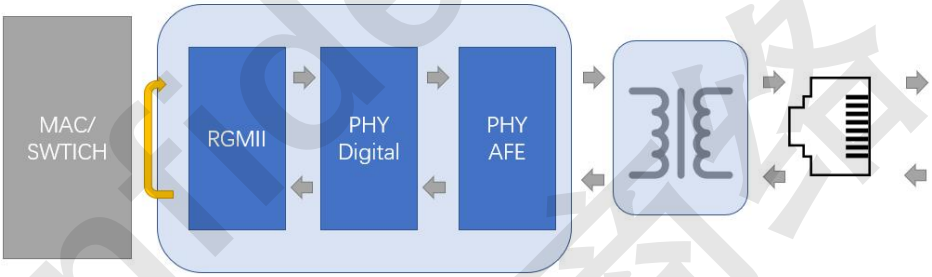


Figure 9. Remote PHY Loopback

4.14. Energy Efficient Ethernet (EEE)

EEE is IEEE 802.3az, an extension of the IEEE 802.3 standard. EEE defines support for the PHY to operate in Low Power Idle (LPI) mode which, when enabled, supports QUIET times during low link utilization allowing both link partners to disable portions of each PHY's circuitry and save power.

4.15. Synchronous Ethernet (Sync-E)

YT8531(D)(P) provides Synchronous Ethernet (Sync-E) support when the device is operating in 1000BASE-T, 100BASE-TX, 1000BASE-X and 100BASE-FX on the transmission media. The CLKOUT pin can be assigned to output the recovered clock.

The recovery clock for Sync-E can be either a 125MHz or 25MHz clock.

If the CLKOUT pin is assigned to output the recovered clock from PHY and PHY is working at 1000BASE-T mode, when the PHY is in SLAVE mode, the CLKOUT will output the recoverd clock from the MDI. If the device is in MASTER mode, the CLKOUT will output the clock based on the local free run PLL.

4.16. Wake-On-LAN (WOL)

Wake-on-LAN (WOL) is a mechanism to manage and regulate the total network power consumption. YT8531(D)(P) supports automatic detection of a specific frame and notification via dedicated hardware interrupt pin. The specific frame contains a specific data sequence located anywhere inside the packet. The data sequence consists of 6 bytes of consecutive 1 (0xFFFFFFFFFFFF), followed by 16 repetitions of the MAC address of the computer to be waked up. The 48-bit MAC address can be set in *MAC_Address_Cfg1~3* common registers.

4.17. Link Down Power Saving (Sleep Mode)

YT8531(D)(P) supports link down power saving, also called sleep mode. When UTP port link down and no signals over UTP cable for 40 seconds, YT8531(D)(P) will enter sleep mode.

For most of time in sleep mode, YT8531(D)(P) will disable almost all the circuits except crystal clock and comparators for channel 0/1 of 10BASE-Te. Access by MDC/MDIO interface is available.

At a time interval in sleep mode, YT8531(D)(P) will wake to transmit signals over TRXP1/TRXN1. The time interval is a random value around 2.7s.

Once detecting signals over UTP cable, YT8531(D)(P) will exit sleep mode.

4.18. Interrupt

YT8531(D)(P) provides an active low interrupt output pin (INT_N) based on change of the PHY status. Every interrupt condition is represented by the read-only general interrupt status register (section 6.2.18. Interrupt Status Register (UTP MII register 0x13)).

The interrupts can be individually enable or disable by setting or clearing bits in the interrupt enable register (section 6.2.17. Interrupt Mask Register (UTP MII register 0x12)).

Note 1: The interrupt of the YT8531(D)(P) is a level-triggered mechanism.

Note 2: The INT_N and PME_N functions share the same pin (pin 31). Refer to section 5.5. INT_N/PME_N Pin Usage.

5. Operational Description

5.1. Reset

YT8531(D)(P) have a hardware reset pin(RESET_N) which is low active. RESET_N should be active for at least 10ms to make sure all internal logic is reset to a known state. Hardware reset should be applied after power up.
RESET_N is also used for power on strapping. After RESET_N is released, YT8531(D)(P) latches input value on strapping pins which are used as configuration information to provide flexibility in application without mdio access.
YT8531(D)(P) also provides one software reset control registers which used to reset all UTP internal logic except some mdio configuration registers, by setting bit 15 of UTP mii register (address 0x0). This bit is self-clear after reset process is done. For detailed information about which register will be reset by software reset, please refer to register table.
YT8531D/YT8531P have another software reset control registers by setting bit 15 of LDS mii register (address 0x0), with the same effect as bit 15 of UTP mii register described above.

Table 11. Reset Timing Characteristics

Symbol	Description	Min	Typ	Max	Units
T1	The duration from all powers steady to reset signal release to high	10	-	-	ms
T2	The duration of reset signal remain low timing	10	-	-	ms

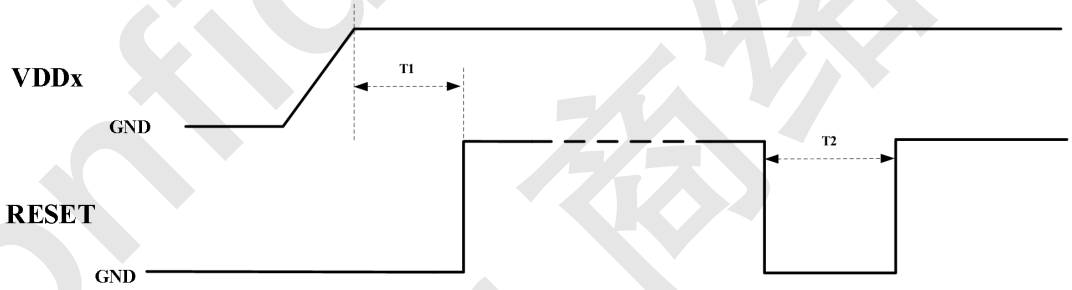


Figure 10. Reset Timing Diagram

5.2. PHY Address

For YT8531(D)(P), Strapping PHYAD[2:0] is used to generate phy address.
YT8531(D)(P) always responses to phy address 0. It can be disabled by configure bit[6] to 1'b0 of extended register(address 0xa005). It also has another broadcast phy address which is configurable through mdio. Bit[4:0] of extended register(address 0xa005) is broadcast phy address and its default value is 5'b11111. Bit[5] of extended register(address 0xa005) is enable control for broadcast phy address and its default value is 1'b0.

5.3. RGMII Interface

Reduced gigabit media independent interface is a subset of GMII which is used for gigabit Ethernet. For 100M/10M application, RGMII is similar to MII. The only difference is that tx_er/rx_er is transmitted by TX_CTL/RX_CTL on the falling edge of clock. TXD[3:0] and RXD[3:0] will be duplicated on both rising and falling edge of clock.
For 100M application, TX_CLK and RX_CLK are 25MHz.
For 10M application, TX_CLK and RX_CLK are 2.5MHz.

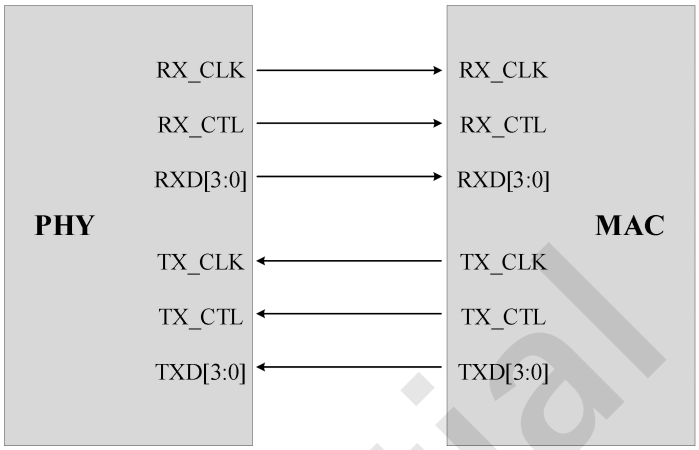


Figure 11. Connection Diagram of RGMII

5.4. LED

The LED interface can either be controlled by the PHY or controlled manually, independent of the state of the PHY. Three status LEDs are available. They can be used to indicate operation speed, duplex mode, and link status. The LEDs can be programmed to different status functions from their default value. They can also be controlled directly from the register interface.

5.5. INT_N/PME_N Pin Usage

The INT_N/PME_N pin (pin 31) is designed to notify both interrupt and WOL events. The default mode of this pin is INT_N (Ext_0xa00a, bit[6]=0). For general use, indication of a WOL event is also integrated into one of the interrupt events which is triggered when any specified WOL event occurs. However, the 'Pulse Low' waveform format is not supported during this mode; only the Active Low, level-triggered waveform is provided.
If PME_N mode is selected (Ext_0xa00a, bit[6]=1), pin 31 becomes a fully functional PME_N pin. Note that the interrupt function is disabled in this mode.

5.6. Power Supplies

The YT8531(D) device requires only one external power supply: 3.3 V. Inside the chip there is a 3.3V rail, 1.1V rail, 2.5V or 1.8V rail.
The YT8531P device requires two external power supply: 3.3 V and 1.1V~1.2V.

5.6.1. Internal Switch Regulator For Core Power

YT8531 integrates a switch regulator which converts 3.3V to 1.1V at a high-efficiency for core power rail.
It is optional for an external regulator to provide this core voltage.

5.6.2. Internal LDO For Core Power

YT8531D integrates a LDO which converts 3.3V to 1.1V.It is optional for an external regulator to provide this core voltage.

5.6.3. Internal LDO For RGMII IO

YT8531(D)(P) also integrates a LDO which converts 3.3V to 2.5V or 1.8V for RGMII I/O power rail and configured by CFG_LDO[1:0].

Table 12. CFG_LDO[1:0] Configuration

Configuration	Description
2'b01	LDO is set to 2.5V
2'b10 or 2'b11	LDO is set to 1.8V

2’b00	Use external 3.3V to supply to DVDD_RGMII pin. LDO is disabled

6. Register Overview

Table 13. Register Access Types

Type	Description
RW	Read and write
SC	Self-clear. If default value is '0' ('1'), writing a '1' ('0') to this register field causes the function to be activated immediately, and then the field will be automatically cleared to '0' ('1').
RO	Read only.
LH	Latch high.
LL	Latch Low.
RC	Read clear.
SWC	Software reset to 0.
SWS	Software reset to 1.
POS	Default value depends on power on strapping.

6.1. Common Register

6.1.1. Chip_Config (EXT_0xA001)

Table 14. chip cfg (0xA001)

Bit	Symbol	Access	Default	Description
15	Sw_rst_n_mode	RW SC	0x1	chip mode change reset, low active, self clear
14:12	Reserved	RW	0x0	Reserved
11	Iddq_mode	RW	0x0	Iddq test mode
10	Reserved	RO	0x0	Reserved
9	En_gate_rx_clk_rgmii	RW	0x0	1=to close RXC when PHY link down; 0=do not close RXC when PHY link down.
8	Rxc_dly_en	RW POS	0x1	rgmii clk 2ns delay control, depend on strapping
7	Reserved	RO	0x0	Reserved
6	En_ldo	RW	0x1	rgmii ldo enable, default is 0 and will be set to 1 after power strapping is done
5:4	Cfg_ldo	RW	0x0	Rgmii ldo voltage and RGMII/MDC/MDIO PAD's level shifter control. Depends on strapping. 2'b11: 1.8v 2'b10: 1.8v 2'b01: 2.5v 2'b00: 3.3v
3:0	Reserved	RO	0x0	Reserved

6.1.2. RGMII_Config1 (EXT_0xA003)

Table 15. RGMII_Config1 (EXT_0xA003)

Bit	Symbol	Access	Default	Description
15	Reserved	RW	0x0	Reserved
14	Tx_clk_sel	RW	0x0	0: use original RGMII TX_CLK to drive the RGMII TX_CLK delay train;

				1: use inverted RGMII TX_CLK to drive the RGMII TX_CLK delay train. Used for debug
13:10	Rx_delay_sel	RW	0x0	RGMII RX_CLK delay train configuration, about 150ps per step
9	En_rgmii_fd_crs	RW	0x0	See EXT 0xA003 bit[8].
8	En_rgmii_crs	RW	0x0	0: to not encode GMII/MII CRS into RGMII OOB; 1: to encode GMII/MII CRS into RGMII OOB when it's half duplex mode or EXT 0xA003 bit[9] is 1.
7:4	Tx_delay_sel_fe	RW	0xf	RGMII TX_CLK delay train configuration when speed is 100Mbps or 10Mbps, it's 150ps per step typically.
3:0	Tx_delay_sel	RW	0x1	RGMII TX_CLK delay train configuration when speed is 1000Mbps, it's150ps per step typically.

6.1.3. RGMII_Config2 (EXT_0xA004)

Table 16. rgmii cfg2 (0xA004)

Bit	Symbol	Access	Default	Description
15:14	Speed_rgphy	RO	0x0	RGMII's speed information when it works as RGMII PHY. It's also the source of RGMII OOB.
13	Duplex_rgphy	RO	0x0	RGMII's duplex information when it works as RGMII PHY. It's also the source of RGMII OOB.
12	Link_up_rgphy	RO	0x0	RGMII's linkup information when it works as RGMII PHY. It's also the source of RGMII OOB.
11:10	Pause_rgphy	RO	0x0	RGMII's pause information when it works as RGMII PHY.
9	Eee_cap_rgphy	RO	0x0	RGMII's EEE capability information when it works as RGMII PHY.
8	Eee_clkstp_cap_rgphy	RO	0x0	RGMII's EEE clock stopable capability information when it works as RGMII PHY.
7:0	Reserved	RO	0x0	Reserved

6.1.4. MDIO_Cfg_And_RGMII_OOB_Mon (EXT_0xA005)

Table 17. MDIO_Cfg_And_RGMII_OOB_Mon (EXT_0xA005)

Bit	Symbol	Access	Default	Description
15:11	Reserved	RO	0x0	Reserved
10	Bypass_mdio_watchdog	RW	0x0	bypass mdio watch dog
9:8	Reserved	RO	0x0	Reserved
7	En_mdc_la	RW	0x1	enable mdc latch for read data
6	En_phyaddr0	RW	0x1	1: to always respond to MDIO command whose PHYAD field is 0; 0: to only respond to MDIO command whose PHYAD filed equals to PHY address strapping.
5	En_bdcst_addr	RW	0x0	enable broadcast address

4:0	Bdcst_addr	RW	0x0	broadcast address

6.1.5. Misc_Config (EXT_0xA006)

Table 18. Misc_Config (EXT_0xA006)

Bit	Symbol	Access	Default	Description
15:8	Reserved	RW	0x0	Reserved
7	Jumbo_enable	RW	0x0	enable jumbo frame
6	Reserved	RW	0x0	Reserved
5	Rem_lpbk_phy	RW	0x0	set remote loopback for UTP
4	Uldata_rloopback	RW	0x0	1=remain upload data when rem lpbk is set for phy
3	Bp_gmii_fatal_rst	RW	0x1	bypass gmii fifo overflow and underflow rst
2:0	Reserved	RW	0x5	Reserved

6.1.6. MAC_Address_Cfg1 (EXT_0xA007)

Table 19. MAC_Address_Cfg1 (EXT_0xA007)

Bit	Symbol	Access	Default	Description
15:0	mac_addr_loc_47_32	RW	0x0	highest 16 bits of MAC address used for WOL

6.1.7. MAC_Address_Cfg2 (EXT_0xA008)

Table 20. MAC_Address_Cfg2 (EXT_0xA008)

Bit	Symbol	Access	Default	Description
15:0	mac_addr_loc_31_16	RW	0x0	middle 16 bits of MAC address used for WOL

6.1.8. MAC_Address_Cfg3 (EXT_0xA009)

Table 21. MAC_Address_Cfg3 (EXT_0xA009)

Bit	Symbol	Access	Default	Description
15:0	mac_addr_loc_15_0	RW	0x0	lowest 16 bits of MAC address used for WOL

6.1.9. WOL_Cfg (EXT_0xA00A)

Table 22. WOL_Cfg (EXT_0xA00A)

Bit	Symbol	Access	Default	Description
15:8	Reserved	RO	0x0	Reserved
7	Sw_close_rgmii	RW	0x0	1.disable rgmii interface 0.enable rgmii interface
6	Pmeb_intb_sel	RW	0x0	1: Pin 31 functions as PME_N. 0: Pin 31 functions as INT_N.
5:4	Reserved	RW	0x0	Reserved
3	Wol_en	RW	0x0	enable WOL.
2:0	Wol_lth_sel	RW	0x2	wol_lth_sel[0], 1: PME_N is pulse triggered and active LOW, the pusel width is controlled by wol_lth_sel[2:1]. 0:PME_N is level triggerd and active LOW; When PME_N is LOW, EXT 0xA00A bit3

				wol_en should be set to 0 to clear the PME_N. Wol_lth_sel[2:1]: 00: 84ms; 01: 168ms; 10: 336ms; 11: 672ms.

6.1.10. LED_GENERAL_CFG (EXT_0xA00B)

Table 23. LED_GENERAL_CFG (EXT_0xA00B)

Bit	Symbol	Access	Default	Description
15	Col_blk_sel	RW	0x1	1 = when collision happens, and related LEDn cfg (n is 0/1/2) register's bit3 led_col_blk_en is 1, LED blink at Blink Mode2; 0 = when collision happens, and related LEDn cfg (n is 0/1/2) register's bit3 led_col_blk_en is 0, LED blink at Blink Mode1. LED could blinks at different frequency in Blink Mode1 and Blink Mode2. Refer to EXT A00F[3:0] for the Blink Mode2 and Blink Mode1.
14	Jabber_led_dis	RW	0x1	1 = when 10Mb/s Jabber happens, LED will not blink;
13	Lpbk_led_dis	RW	0x1	1 = In internal loopback mode, LED will not blink;
12	Dis_led_an_try	RW	0x0	1: LED will be ON when auto-negotiation is at LINK_GOOD_CHECK status, in which status, the link is not up already.
11:9	Reserved	RO	0x0	Reserved
8	Led_2_force_en	RW	0x0	1 = enable LED2 force mode.
7:6	Led_2_force_mode	RW	0x0	Valid when bit8 is set. 00: force LED OFF; 01: force LED ON; 10: force LED Blink at Blink Mode2; 11: force LED Blink at Blink Mode1. LED could blinks at different frequency in Blink Mode1 and Blink Mode2. Refer to EXT A00F[3:0] for the Blink Mode2 and Blink Mode1.
5	Led_1_force_en	RW	0x0	1 = enable LED1 force mode.
4:3	Led_1_force_mode	RW	0x0	Valid when bit5 is set. Refer EXT A00B[7:6] for the force mode description.
2	Led_0_force_en	RW	0x0	1 = enable LED0 force mode.
1:0	Led_0_force_mode	RW	0x0	Valid when bit2 is set. Refer EXT A00B[7:6] for the force mode description.

6.1.11. LED0_CFG (EXT_0xA00C)

Table 24. LED0_CFG (EXT_0xA00C)

Bit	Symbol	Access	Default	Description
15:14	Reserved	RW	0x0	Reserved
13	Led_act_blk_ind_0	RW	0x0	When traffic is present, make LED0 BLINK no matter the previous LED0 status is ON or OFF, or make LED0 blink only when the previous LED0 is ON.
12	Led_fdx_on_en_0	RW	0x0	1: If BLINK status is not activated, when PHY link up and duplex mode is full duplex, LED0 will be ON.
11	Led_hdx_on_en_0	RW	0x0	1: If BLINK status is not activated, when PHY link up and duplex mode is half duplex, LED0 will be ON.
10	Led_txact_blk_en_0	RW	0x1	1: If bit[13] is 1, or bit[13] is 0 and ON at certain speed or duplex more is/are activated, when PHY link up and TX is active, make LED0 blink at mode2.
9	Led_rxact_blk_en_0	RW	0x1	1: If bit[13] is 1, or bit[13] is 0 and ON at certain speed or duplex more is/are activated, when PHY link up and RX is active, make LED0 blink at mode2.
8	Led_txact_on_en_0	RW	0x0	1: if BLINK status is not activated, when PHY link up and TX is active, make LED0 ON at least 10ms.
7	Led_rxact_on_en_0	RW	0x0	1: if BLINK status is not activated, when PHY link up and RX is active, make LED0 ON at least 10ms.
6	Led_gt_on_en_0	RW	0x0	1: if BLINK status is not activated, when PHY link up and speed mode is 1000Mbps, make LED0 ON.
5	Led_ht_on_en_0	RW	0x0	1: if BLINK status is not activated, when PHY link up and speed mode is 100Mbps, make LED0 ON;
4	Led_bt_on_en_0	RW	0x1	1: if BLINK status is not activated, when PHY link up and speed mode is 10Mbps, make LED0 ON;
3	Led_col_blk_en_0	RW	0x0	1: if PHY link up and collision happen, make LED0 BLINK;
2	Led_gt_blk_en_0	RW	0x0	1: if PHY link up and speed mode is 1000Mbps, make LED0 BLINK;
1	Led_ht_blk_en_0	RW	0x0	1: if PHY link up and speed mode is 100Mbps, make LED0 BLINK;
0	Led_bt_blk_en_0	RW	0x0	1: if PHY link up and speed mode is 10Mbps, make LED0 BLINK;

6.1.12. LED1_CFG (EXT_0xA00D)

Table 25. LED1_CFG (EXT_0xA00D)

Bit	Symbol	Access	Default	Description
15:14	Reserved	RW	0x0	Reserved
13	Led_act_blk_ind_1	RW	0x0	Same logic as LED0 control.
12	Led_fdx_on_en_1	RW	0x0	Same logic as LED0 control.
11	Led_hdx_on_en_1	RW	0x0	Same logic as LED0 control.
10	Led_txact_blk_en_1	RW	0x1	Same logic as LED0 control.

9	Led_rxact_blk_en_1	RW	0x1	Same logic as LED0 control.
8	Led_txact_on_en_1	RW	0x0	Same logic as LED0 control.
7	Led_rxact_on_en_1	RW	0x0	Same logic as LED0 control.
6	Led_gt_on_en_1	RW	0x0	Same logic as LED0 control.
5	Led_ht_on_en_1	RW	0x1	Same logic as LED0 control.
4	Led_bt_on_en_1	RW	0x0	Same logic as LED0 control.
3	Led_col_blk_en_1	RW	0x0	Same logic as LED0 control.
2	Led_gt_blk_en_1	RW	0x0	Same logic as LED0 control.
1	Led_ht_blk_en_1	RW	0x0	Same logic as LED0 control.
0	Led_bt_blk_en_1	RW	0x0	Same logic as LED0 control.

6.1.13. LED2_CFG (EXT_0xA00E)

Table 26. LED2_CFG (EXT_0xA00E)

Bit	Symbol	Access	Default	Description
15:14	Reserved	RW	0x0	Reserved
13	Led_act_blk_ind_2	RW	0x0	Same logic as LED0 control.
12	Led_fdx_on_en_2	RW	0x0	Same logic as LED0 control.
11	Led_hdx_on_en_2	RW	0x0	Same logic as LED0 control.
10	Led_txact_blk_en_2	RW	0x1	Same logic as LED0 control.
9	Led_rxact_blk_en_2	RW	0x1	Same logic as LED0 control.
8	Led_txact_on_en_2	RW	0x0	Same logic as LED0 control.
7	Led_rxact_on_en_2	RW	0x0	Same logic as LED0 control.
6	Led_gt_on_en_2	RW	0x1	Same logic as LED0 control.
5	Led_ht_on_en_2	RW	0x0	Same logic as LED0 control.
4	Led_bt_on_en_2	RW	0x0	Same logic as LED0 control.
3	Led_col_blk_en_2	RW	0x0	Same logic as LED0 control.
2	Led_gt_blk_en_2	RW	0x0	Same logic as LED0 control.
1	Led_ht_blk_en_2	RW	0x0	Same logic as LED0 control.
0	Led_bt_blk_en_2	RW	0x0	Same logic as LED0 control.

6.1.14. LED_BLINK_CFG (EXT_0xA00F)

Table 27. LED_BLINK_CFG (EXT_0xA00F)

Bit	Symbol	Access	Default	Description
15:7	Reserved	RO	0x0	Reserved
6:4	Led_duty	RW	0x0	Select duty cycle of Blink: 000: 50% ON and 50% OFF; 001: 67% ON and 33% OFF; 010: 75% ON and 25% OFF; 011: 83% ON and 17% OFF; 100: 50% ON and 50% OFF; 101: 33% ON and 67% OFF; 110: 25% ON and 75% OFF; 111: 17% ON and 83% OFF.
3:2	Freq_sel_2	RW	0x1	Select frequency of Blink Mode2: 00: 2Hz; 01: 4Hz; 10: 8Hz; 11: 16Hz.

1:0	Freq_sel_1	RW	0x2	Select frequency of Blink Mode1: 00: 2Hz; 01: 4Hz; 10: 8Hz; 11: 16Hz.

6.1.15. Pad Drive Strength Cfg (EXT_0xA010)

Table 28. Pad Drive Strength Cfg (EXT_0xA010)

Bit	Symbol	Access	Default	Description
15:13	Rgmii_sw_dr_rxc	RW	0x3	Drive strength of rx_clk pad. 3'b111: strongest; 3'b000: weakest.
12	Rgmii_sw_dr[2]	RW	0x0	Bit 2 of Rgmii_sw_dr[2:0], refer to ext A010 [5:4]
11	Int_od_en	RW	0x1	1'b1: Interrupt pin acts as a open drain pad 1'b0: Interrupt pin acts as a normal output pad
10	Int_act_hi	RW	0x0	1'b1: Interrupt acts as high active 1'b0: Interrupt acts as low active
9:8	Dr_sync_e	RW	0x3	Drive strength of SyncE pad. 2'b11: strongest; 2'b00: weakest
7:6	Dr_mdio	RW	0x3	Drive strength of mdio pad. 2'b11: strongest; 2'b00: weakest
5:4	Rgmii_sw_dr[1:0]	RW POS	0x3	Bit 1 and 0 of Rgmii_sw_dr, Drive strength of rxd/rx_ctl rgmii pad. 3'b111: strongest; 3'b000: weakest
3:2	Dr_int_io	RW	0x3	Drive strength of interrupt pad. 2'b11: strongest; 2'b00: weakest
1:0	Dr_led	RW	0x3	Drive strength of led pad. 2'b11: strongest; 2'b00: weakest

6.1.16. SyncE_CFG (EXT_0xA012)

Table 29. SyncE_CFG (EXT_0xA012)

Bit	Symbol	Access	Default	Description
15:8	Reserved	RO	0x0	Reserved
7	Reserved	RW	0x1	Reserved
6	En_sync_e	RW	0x1	enable sync e clock output
5	En_sync_e_during_lnkdn	RW	0x0	always output sync e clock even when link is down
4	Clk_fre_sel	RW	0x0	1'b1: output 125m clock; 1'b0: output 25m clock
3:1	Clk_src_sel	RW	0x4	select clock source of synce. 3'b000: internal 125MHz PLL output clock 3'b001: UTP recovered RX clock (when {en_adc_1, en_adc_0}==2'b10, output adc1; ==2'b01 or 2'b11 output adc0 clock, else disable output) 3'b010: Reserved. 3'b011: clock from digital (RGMII TX delayed clock, or debug clock out) 3'b100: reference 25MHz clock (default) 3'b101: 25MHz SSC.

				Source of 3'b000 and 3'b001 can be controled by clk_fre_sel.
0	Reserved	RO	0x0	Reserved

6.2. UTP MII Register

6.2.1. Basic Control Register (0x00)

Table 30. Basic Control Register (0x00)

Bit	Symbol	Access	Default	Description
15	Reset	RW SC	0x0	PHY Software Reset. Writing 1 to this bit causes immediate PHY reset. Once the operation is done, this bit is cleared automatically. 0: Normal operation 1: PHY reset
14	Loopback	RW SWC	0x0	Internal loopback control 1'b0: disable loopback 1'b1: enable loopback
13	Speed_Selection(LSB)	RW	0x0	LSB of speed_selection[1:0]. Link speed can be selected via either the Auto-Negotiation process, or manual speed selection speed_selection[1:0]. Speed_selection[1:0] is valid when Auto-Negotiation is disabled by clearing bit 0.12 to zero. Bit6 bit13 1 1 = Reserved 1 0 = 1000Mb/s 0 1 = 100Mb/s 0 0 = 10Mb/s
12	Autoneg_En	RW	0x1	1: to enable auto-negotiation; 0: auto-negotiation is disabled.
11	Power_down	RW SWC	0x0	1 = Power down 0 = Normal operation When the port is switched from power down to normal operation, software reset and Auto-Negotiation are performed even bit[15] RESET and bit[9] RESTART_AUTO_NEGOTIATION are not set by the user.
10	Isolate	RW SWC	0x0	Isolate phy from RGMII. 1'b0: Normal mode 1'b1: Isolate mode
9	Re_Autoneg	RW SC SWS	0x0	Auto-Negotiation automatically restarts after hardware or software reset regardless of bit[9] RESTART. 1 = Restart Auto-Negotiation Process 0 = Normal operation
8	Duplex_Mode	RW	0x1	The duplex mode can be selected via either the Auto-Negotiation process or manual duplex selection. Manual duplex selection is allowed when Auto-Negotiation is disabled by setting bit[12] AUTO_NEGOTIATION to 0. 1 = Full Duplex 0 = Half Duplex
7	Collision_Test	RW SWC	0x0	Setting this bit to 1 makes the COL signal

				asserted whenever the TX_EN signal is asserted. 1 = Enable COL signal test 0 = Disable COL signal test
6	Speed_ Selection(MSB)	RW	0x1	See bit13.
5:0	Reserved	RO	0x0	Reserved. Write as 0, ignore on read

6.2.2. Basic Status Register (0x01)

Table 31. Basic Status Register (0x01)

Bit	Symbol	Access	Default	Description
15	100BASE-T4	RO	0x0	PHY doesn't support 100BASE-T4
14	100BASE-X_Fd	RO	0x1	PHY supports 100BASE-X_FD
13	100BASE-X_Hd	RO	0x1	PHY supports 100BASE-X_HD
12	10Mbps_Fd	RO	0x1	PHY supports 10Mbps_Fd
11	10Mbps_Hd	RO	0x1	PHY supports 10Mbps_Hd
10	100BASE-T2_Fd	RO	0x0	PHY doesn't support 100BASE-T2_Fd
9	100BASE-T2_Hd	RO	0x0	PHY doesn't support 100BASE-T2_Hd
8	Extended_Status	RO	0x1	Whether support Extended status register in MII 0xF 0: Not supported 1: Supported
7	Unidirect_Ability	RO	0x0	1'b0: PHY able to transmit from MII only when the PHY has determined that a valid link has been established 1’b1: PHY able to transmit from MII regardless of whether the PHY has determined that a valid link has been established
6	Mf_Preamble_Suppression	RO	0x1	1'b0: PHY will not accept management frames with preamble suppressed 1’b1: PHY will accept management frames with preamble suppressed
5	Autoneg_Complete	RO SWC	0x0	1'b0: Auto-negotiation process not completed 1’b1: Auto-negotiation process completed
4	Remote_Fault	RO RC SWC LH	0x0	1'b0: no remote fault condition detected 1’b1: remote fault condition detected
3	Autoneg_Ability	RO	0x1	1'b0: PHY not able to perform Auto-negotiation 1’b1: PHY able to perform Auto-negotiation
2	Link_Status	RO LL SWC	0x0	Link status 1’b0: Link is down 1’b1: Link is up
1	Jabber_Detect	RO RC SWC LH	0x0	10BASE-Te jabber detected. It would assert if TX activity lasts longer than 42ms. 1’b0: no jabber condition detected 1’b1: Jabber condition detected.
0	Extended_Capability	RO	0x1	To indicate whether support Extended registers, to access from address register 0x1E and data register 0x1F 1’b0: Not supported 1’b1: Supported

6.2.3. PHY Identification Register1 (0x02)

Table 32. PHY Identification Register1 (0x02)

Bit	Symbol	Access	Default	Description
15:0	Phy_Id	RO	0x4f51	Bits 3 to 18 of the Organizationally Unique Identifier

6.2.4. PHY Identification Register2 (0x03)

Table 33. PHY Identification Register2 (0x03)

Bit	Symbol	Access	Default	Description
15:10	Phy_Id	RO	0x3a	Bits 19 to 24 of the Organizationally Unique Identifier
9:4	Type_No	RO	0x11	6 bits manufacturer's type number
3:0	Revision_No	RO	0xb	4 bits manufacturer's revision number

6.2.5. Auto-Negotiation Advertisement (0x04)

Table 34. Auto-Negotiation Advertisement (0x04)

Bit	Symbol	Access	Default	Description
15	NEXT_Page	RW	0x0	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down If 1000BASE-T is advertised, the required next pages are automatically transmitted. This bit must be set to 0 if no additional next page is needed. 1 = Advertise 0 = Not advertised
14	Ack	RO	0x0	Always 0.
13	Remote_Fault	RW	0x0	1 = Set Remote Fault bit 0 = Do not set Remote Fault bit
12	Extended_NEXT_Page	RW	0x1	Extended EXT page enable control bit 1 = Local device supports transmission of extended next pages 0 = Local device does not support transmission of extended next pages.
11	Asymmetric_Pause	RW	0x0	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to

				normal operation by writing register 0x0 bit[11] • Link goes down 1 = Asymmetric Pause 0 = No asymmetric Pause
10	Pause	RW	0x0	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down 1 = MAC PAUSE implemented 0 = MAC PAUSE not implemented
9	100BASE-T4	RO	0x0	1 = Able to perform 100BASE-T4 0 = Not able to perform 100BASE-T4 Always 0
8	100BASE-TX_Full_Duplex	RW	0x1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down 1 = Advertise 0 = Not advertised
7	100BASE-TX_Half_Duplex	RW	0x1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down 1 = Advertise 0 = Not advertised
6	10BASE-Te_Full_Duplex	RW	0x1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to

				normal operation by writing register 0x0 bit[11] • Link goes down 1 = Advertise 0 = Not advertised
5	10BASE-Te_Half_Duplex	RW	0x1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down 1 = Advertise 0 = Not advertised
4:0	Selector_Field	RW	0x1	Selector Field mode. 00001 = IEEE 802.3

6.2.6. Auto-Negotiation Link Partner Ability (0x05)

Table 35. Auto-Negotiation Link Partner Ability (0x05)

Bit	Symbol	Access	Default	Description
15	1000BASE-X_Fd	RO SWC	0x0	Received Code Word Bit 15 1 = Link partner is capable of next page 0 = Link partner is not capable of next page
14	ACK	RO SWC	0x0	Acknowledge. Received Code Word Bit 14 1 = Link partner has received link code word 0 = Link partner has not received link code word
13	REMOTE_FAULT	RO SWC	0x0	Remote Fault. Received Code Word Bit 13 1 = Link partner has detected remote fault 0 = Link partner has not detected remote fault
12	RESERVED	RO SWC	0x0	Technology Ability Field. Received Code Word Bit 12
11	ASYMMETRIC_PAUSE	RO SWC	0x0	Technology Ability Field. Received Code Word Bit 11 1 = Link partner requests asymmetric pause 0 = Link partner does not request asymmetric pause
10	PAUSE	RO SWC	0x0	Technology Ability Field. Received Code Word Bit 10 1 = Link partner supports pause operation 0 = Link partner does not support pause operation
9	100BASE-T4	RO SWC	0x0	Technology Ability Field. Received Code Word Bit 9 1 = Link partner supports 100BASE-T4 0 = Link partner does not support100BASE-T4
8	100BASE-TX_FULL_DUPLEX	RO SWC	0x0	Technology Ability Field. Received Code Word Bit 8 1 = Link partner supports 100BASE-TX full-duplex 0 = Link partner does not support 100BASE-TX full-duplex

7	100BASE-TX_HALF_DUPLEX	RO SWC	0x0	Technology Ability Field. Received Code Word Bit 7 1 = Link partner supports 100BASE-TX half-duplex 0 = Link partner does not support 100BASE-TX half-duplex
6	10BASE-Te_FULL_DUPLEX	RO SWC	0x0	Technology Ability Field. Received Code Word Bit 6 1 = Link partner supports 10BASE-Te full-duplex 0 = Link partner does not support 10BASE-Te full-duplex
5	10BASE-Te_HALF_DUPLEX	RO SWC	0x0	Technology Ability Field. Received Code Word Bit 5 1 = Link partner supports 10BASE-Te half-duplex 0 = Link partner does not support 10BASE-Te half-duplex
4:0	SELECTOR_FIELD	RO SWC	0x0	Selector Field Received Code Word Bit 4:0

6.2.7. Auto-Negotiation Expansion Register (0x06)

Table 36. Auto-Negotiation Expansion Register (0x06)

Bit	Symbol	Access	Default	Description
15:5	Reserved	RO	0x0	Reserved
4	Parallel Detection fault	RO RC LH SWC	0x0	1 = Fault is detected 0 = No fault is detected
3	Link partner EXT page able	RO LH SWC	0x0	1 = Link partner supports NEXT page 0 = Link partner does not support next page
2	Local NEXT Page able	RO	0x1	1 = Local Device supports NEXT Page 0 = Local Device does not support Next Page
1	Page received	RO RC LH	0x0	1 = A new page is received 0 = No new page is received
0	Link Partner Auto negotiation able	RO	0x0	1 = Link partner supports auto-negotiation 0 = Link partner does not support auto-negotiation

6.2.8. Auto-Negotiation NEXT Page Register (0x07)

Table 37. Auto-Negotiation NEXT Page Register (0x07)

Bit	Symbol	Access	Default	Description
15	NEXT Page	RW	0x0	Transmit Code Word Bit 15 1 = The page is not the last page 0 = The page is the last page
14	Reserved	RO	0x0	Reserved
13	Message page mode	RW	0x1	Transmit Code Word Bit 13 1 = Message Page 0 = Unformatted Page
12	Ack2	RW	0x0	Transmit Code Word Bit 12 1 = Comply with message 0 = Cannot comply with message
11	Toggle	RO	0x0	Transmit Code Word Bit 11 1 = This bit in the previously exchanged Code Word is logic 0

				0 = The Toggle bit in the previously exchanged Code Word is logic 1
10:0	Message/Unformatte	RW	0x1	Transmit Code Word Bits [10:0]. These bits are encoded as Message Code Field when bit[13] is set to 1, or as Unformatted Code Field when bit[13] is set to 0.

6.2.9. Auto-Negotiation Link Partner Received NEXT Page Register (0x08)

Table 38. Auto-Negotiation Link Partner Received NEXT Page Register (0x08)

Bit	Symbol	Access	Default	Description
15	NEXT Page	RO	0x0	Received Code Word Bit 15 1 = This page is not the last page 0 = This page is the last page
14	Ack	RO	0x0	Received Code Word Bit 14 1 = successfully received its Link Partner's ack 0 = didn't receive its Link Partner's ack
13	Message page mode	RO	0x0	Received Code Word Bit 13 1 = Message Page 0 = Unformatted Page
12	Ack2	RO	0x0	Received Code Word Bit 12 1 = Comply with message 0 = Cannot comply with message
11	Toggle	RO	0x0	Received Code Word Bit 11 1 = This bit in the previously exchanged Code Word is logic 0 0 = The Toggle bit in the previously exchanged Code Word is logic 1
10:0	Message/Unformatte	RO	0x0	Received Code Word Bit 10:0 These bits are encoded as Message Code Field when bit[13] is set to 1, or as Unformatted Code Field when bit[13] is set to 0.

6.2.10. MASTER-SLAVE control register (0x09)

Table 39. MASTER-SLAVE control register (0x09)

Bit	Symbol	Access	Default	Description
15:13	Test mode	RW	0x0	The TX_TCLK signals from the RX_CLK pin is for jitter testing in test modes 2 and 3. When exiting the test mode, hardware reset or software reset through writing MII register 0x0 bit[15] must be performed to ensure normal operation. 000 = Normal Mode 001 = Test Mode 1 - Transmit Waveform Test 010 = Test Mode 2 - Transmit Jitter Test (MASTER mode) 011 = Test Mode 3 - Transmit Jitter Test (SLAVE mode) 100 = Test Mode 4 - Transmit Distortion Test 110, 111 = Reserved, normal operation.
12	Master/Slave Manual configuration Enable	RW	0x0	This bit is updated immediately after the writing operation; however the configuration does not

				take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down 1 = Manual MASTER/SLAVE configuration 0 = Automatic MASTER/SLAVE configuration.
11	Master/Slave configuration	RW	0x0	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down This bit is ignored if bit[12] is 0. 1 = Manual configuration as MASTER 0 = Manual configuration as SLAVE.
10	Port Type	RW	0x0	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down This bit is ignored if bit[12] is 1. 1 = Prefer multi-port device (MASTER) 0 = Prefer single port device (SLAVE)
9	1000BASE-T Full	RW	0x1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down 1 = Advertise 0 = Not advertised
8	1000BASE-T Half-	RW	0x0	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11]

				• Link goes down 1 = Advertise 0 = Not advertised (default)
7:0	Reserved	RW	0x0	Write as 0, ignore on read.

6.2.11. MASTER-SLAVE Status Register (0x0A)

Table 40. MASTER-SLAVE Status Register (0x0A)

Bit	Symbol	Access	Default	Description
15	Master/Slave_cfg_error	RO RC SWC LH	0x0	This register bit will clear on read, rising of MII 0.12 and rising of AN complete. 1 = Master/Slave configuration fault detected 0 = No fault detected
14	Master/Slave	RO	0x0	This bit is not valid unless register 0x1 bit5 is 1. 1 = Local PHY configuration resolved to Master 0 = Local PHY configuration resolved to Slave
13	Local Receiver Status	RO	0x0	1 = Local Receiver OK 0 = Local Receiver not OK
12	Remote Receiver	RO	0x0	1 = Remote Receiver OK 0 = Remote Receiver not OK
11	Link Partner 1000T FD	RO	0x0	This bit is not valid unless register 0x1 bit5 is 1. 1 = Link Partner supports 1000BASE-T full duplex 0 = Link Partner does not support 1000BASE-T full duplex
10	Link Partner 1000T HD	RO	0x0	This bit is not valid unless register 0x1 bit5 is 1. 1 = Link Partner supports 1000BASE-T half duplex 0 = Link Partner does not support 1000BASE-T half duplex
9:8	Reserved	RO	0x0	Reserved
7:0	Idle Error Count	RO RC	0x0	MSB of Idle Error Counter. The register indicates the idle error count since the last read operation performed to this register. The counter pegs at 11111111 and does not roll over.

6.2.12. MMD Access Control Register (0x0D)

Table 41. MMD Access Control Register (0x0D)

Bit	Symbol	Access	Default	Description
15:14	Function	RW	0x0	00 = Address 01 = Data, no post increment 10 = Data, post increment on reads and writes 11 = Data, post increment on writes only
13:5	Reserved	RO	0x0	Reserved
4:0	DEVAD	RW	0x0	MMD register device address. 00001 = MMD1 00011 = MMD3 00111 = MMD7

6.2.13. MMD Access Data Register (0x0E)

Table 42. MMD Access Data Register (0x0E)

Bit	Symbol	Access	Default	Description
15:0	Address data	RW	0x0	If register 0xD bits [15:14] are 00, this register is used as MMD DEVAD address register. Otherwise, this register is used as MMD DEVAD data register as indicated by its address register.

6.2.14. Extended status register (0x0F)

Table 43. Extended status register (0x0F)

Bit	Symbol	Access	Default	Description
15	1000BASE-X Full Duplex	RO	0x0	1 = PHY supports 1000BASE-X Full Duplex 0 = PHY does not supports 1000BASE-X Full Duplex Always 0.
14	1000BASE-X Half Duplex	RO	0x0	1 = PHY supports 1000BASE-X Half Duplex. 0 = PHY does not support 1000BASE-X Half Duplex. Always 0
13	1000BASE-T Full Duplex	RO	0x1	1 = PHY supports 1000BASE-T Full Duplex 0 = PHY does not supports 1000BASE-T Full Duplex Always 1
12	1000BASE-T Half Duplex	RO	0x0	1 = PHY supports 1000BASE-T Half Duplex 0 = PHY does not support 1000BASE-T Half Duplex Always 0.
11:0	Reserved	RO	0x0	Reserved

6.2.15. PHY Specific Function Control Register (0x10)

Table 44. PHY Specific Function Control Register (0x10)

Bit	Symbol	Access	Default	Description
15:7	Reserved	RO	0x0	Reserved
6:5	Cross_md	RW	0x3	Changes made to these bits disrupt normal operation, thus a software reset is mandatory after the change. And the configuration does not take effect until software reset. 00 = Manual MDI configuration 01 = Manual MDIX configuration 10 = Reserved 11 = Enable automatic crossover for all modes
4	Reserved	RO	0x0	Reserved
3	Crs_on_tx	RW	0x0	This bit is effective in 10BASE-Te half-duplex mode and 100BASE-TX mode: 1 = Assert CRS on transmitting or receiving 0 = Never assert CRS on transmitting, only assert it on receiving.
2	En_sqe_test	RW	0x0	1 = SQE test enabled, 0 = SQE test disabled Note: SQE Test is automatically disabled in full-duplex mode regardless the setting in this

				bit.
1	En_pol_inv	RW	0x1	If polarity reversal is disabled, the polarity is forced to be normal in 10BASE-Te. 1 = Polarity Reversal Enabled 0 = Polarity Reversal Disabled
0	Dis_jab	RW	0x0	1 = Disable 10BASE-Te jabber detection function 0 = Enable 10BASE-Te jabber detection function

6.2.16. PHY Specific Status Register (0x11)

Table 45. PHY Specific Status Register (0x11)

Bit	Symbol	Access	Default	Description
15:14	Speed_mode	RO	0x0	These status bits are valid only when bit11 is 1. Bit11 is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps
13	Duplex	RO	0x0	This status bit is valid only when bit11 is 1. Bit11 is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Full-duplex 0 = Half-duplex
12	Page Received real-time	RO	0x0	1 = Page received 0 = Page not received
11	Speed and Duplex Resolved	RO	0x0	When Auto-Negotiation is disabled, this bit is set to 1 for force speed mode. 1 = Resolved 0 = Not resolved
10	Link status real-time	RO	0x0	1 = Link up 0 = Link down
9:7	Reserved	RO	0x0	Reserved
6	MDI Crossover Status	RO	0x0	This status bit is valid only when bit11 is 1. Bit11 is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. The bit value depends on register 0x10 “PHY specific function control register” bits6~bit5 configurations. Register 0x10 configurations take effect after software reset. 1 = MDIX 0 = MDI
5	Wirespeed downgrade	RO	0x0	1 = Downgrade 0 = No Downgrade
4	Reserved	RO	0x0	Reserved
3	Transmit Pause	RO	0x0	This status bit is valid only when bit11 is 1. Bit11 is set when Auto-Negotiation is completed. This bit indicates MAC pause resolution. This bit is for information purposes only and is not used by the device. When in force mode, this bit is set to be 0.

				1 = Transmit pause enabled 0 = Transmit pause disabled
2	Receive Pause	RO	0x0	This status bit is valid only when bit[11] is 1. Bit[11] is set when Auto-Negotiation is completed. This bit indicates MAC pause resolution. This bit is for information purposes only and is not used by the device. When in force mode, this bit is set to be 0. 1 = Receive pause enabled 0 = Receive pause disabled
1	Polarity Real Time	RO	0x0	1 = Reverted polarity 0 = Normal polarity
0	Jabber Real Time	RO	0x0	1 = Jabber 0 = No jabber

6.2.17. Interrupt Mask Register (0x12)

Table 46. Interrupt Mask Register (0x12)

Bit	Symbol	Access	Default	Description
15	Auto-Negotiation Error INT mask	RW	0x0	1 = Interrupt enable 0 = Interrupt disable
14	Speed Changed INT mask	RW	0x0	same as bit 15
13	Duplex changed INT mask	RW	0x0	same as bit 15
12	Page Received INT mask	RW	0x0	same as bit 15
11	Link Failed INT mask	RW	0x0	same as bit 15
10	Link Succeed INT mask	RW	0x0	same as bit 15
9:7	reserved	RW	0x0	No used.
6	WOL INT mask	RW	0x0	same as bit 15
5	Wirespeed downgraded INT mask	RW	0x0	same as bit 15
4:2	Reserved	RW	0x0	No used.
1	Polarity changed INT mask	RW	0x0	same as bit 15
0	Jabber Happened INT mask	RW	0x0	same as bit 15

6.2.18. Interrupt Status Register (0x13)

Table 47. Interrupt Status Register (0x13)

Bit	Symbol	Access	Default	Description
15	Auto-Negotiation Error INT	RO RC	0x0	Error can take place when any of the following happens: • MASTER/SLAVE does not resolve correctly • Parallel detect fault • No common HCD • Link does not come up after negotiation is complete • Selector Field is not equal • flp_receive_idle=true while Autoneg Arbitration FSM is in NEXT PAGE WAIT state 1 = Auto-Negotiation Error takes place 0 = No Auto-Negotiation Error takes place
14	Speed Changed INT	RO RC	0x0	1 = Speed changed 0 = Speed not changed

13	Duplex changed INT	RO RC	0x0	1 = duplex changed 0 = duplex not changed
12	Page Received INT	RO RC	0x0	1 = Page received 0 = Page not received
11	Link Failed INT	RO RC	0x0	1 = Phy link down takes place 0 = No link down takes place
10	Link Succeed INT	RO RC	0x0	1 = Phy link up takes place 0 = No link up takes place
9:7	reserved	RO RC	0x0	No used.
6	WOL INT	RO RC	0x0	1 = PHY received WOL magic frame. 0 = PHY didn't receive WOL magic frame
5	Wirespeed downgraded INT	RO RC	0x0	1 = speed downgraded. 0 = Speed didn't downgrade.
4:2	Reserved	RO	0x0	Reserved
1	Polarity changed INT	RO RC	0x0	1 = PHY revered MDI polarity 0 = PHY didn't revert MDI polarity
0	Jabber Happened INT	RO RC	0x0	1 = 10BASE-Te TX jabber happened 0 = 10BASE-Te TX jabber didn't happen Please refer to UTP MII Register 0x1 bit[1] Jabber_Detect.

6.2.19. Speed Auto Downgrade Control Register (0x14)

Table 48. Speed Auto Downgrade Control Register (0x14)

Bit	Symbol	Access	Default	Description
15:12	Reserved	RO	0x0	Reserved
11:6	Reserved	RW	0x20	Reserved
5	En_speed_downgrade	RW POS	0x1	When this bit is set to 1, the PHY enables smart-speed function. Writing this bit requires a software reset to update.
4:2	Autoneg retry limit pre-downgrade	RW	0x3	If these bits are set to 3, the PHY attempts five times (set value 3 + additional 2) before downgrading. The number of attempts can be changed by these bits. Only take effect after software reset
1	Reserved	RW	0x0	Reserved
0	Reserved	RO	0x0	Reserved

6.2.20. Rx Error Counter Register (0x15)

Table 49. Rx Error Counter Register (0x15)

Bit	Symbol	Access	Default	Description
15:0	Rx_err_counter	RO SWC	0x0	This counter increase by 1 at the 1st rising of RX_ER when RX_DV is 1. The counter will hold at maximum 16'hFFFF and not roll over.

6.2.21. Extended Register's Address Offset Register (0x1E)

Table 50. Extended Register's Address Offset Register (0x1E)

Bit	Symbol	Access	Default	Description
15:8	Reserved	RO	0x0	Reserved

7:0	Extended Register Address Offset	RW	0x0	It's the address offset of the extended register that will be Write or Read

6.2.22. Extended Register's Data Register (0x1F)

Table 51. Extended Register's Data Register (0x1F)

Bit	Symbol	Access	Default	Description
15:0	Extended Register Data	RW	0x0	It's the data to be written to the extended register indicated by the address offset in register 0x1E, or the data read out from that extended register.

6.3. UTP MMD Register

6.3.1. PCS Control 1 Register (MMD3, 0x0)

Table 52. PCS Control 1 Register (MMD3, 0x0)

Bit	Symbol	Access	Default	Description
15	Pcs_rst	RW SC	0x0	Setting this bit will set all PCS registers to their default states. This action also initiate a software reset as setting MII 0x0 bit15 and a reset as setting MMD1 0x0 bit15 and MMD7 0x0 bit15.
14:11	Reserved	RO	0x0	Reserved
10	Clock_stoppable	RW SWC	0x0	Not used.
9:0	Reserved	RO	0x0	Reserved

6.3.2. PCS Status 1 Register (MMD3, 0x1)

Table 53. PCS Status 1 Register (MMD3, 0x1)

Bit	Symbol	Access	Default	Description
15:12	Reserved	RO	0x0	Reserved
11	Tx_lpi_rxed	RO LH	0x0	When read as 1, it indicates that the transmit PCS has received low power idle signaling one or more times since the register was last read. Latch High.
10	Rx_lpi_rxed	RO LH	0x0	When read as 1, it indicates that the receive PCS has received low power idle signaling one or more times since the register was last read. Latch High.
9	Tx_lpi_indic	RO	0x0	When read as 1, it indicates that the transmit PCS is currently receiving low power idle signals.
8	Rx_lpi_indic	RO	0x0	When read as 1, it indicates that the receive PCS is currently receiving low power idle signals.
7:3	Reserved	RO	0x0	Reserved
2	Pcsrx_lnk_status	RO LL	0x0	PCS status, latch low.
1:0	Reserved	RO	0x0	Reserved

6.3.3. EEE Control and Capability Register (MMD3, 0x14)

Table 54. EEE Control and Capability Register (MMD3, 0x14)

Bit	Symbol	Access	Default	Description
15:3	Reserved	RO	0x0	Reserved
2	1000BASE-T EEE	RO	0x1	Always 1. EEE is supported for 1000BASE-T
1	100BASE-TX EEE	RO	0x1	Always 1. EEE is supported for 100BASE-TX
0	Reserved	RO	0x0	Reserved

6.3.4. EEE Wake Error Counter (MMD3, 0x16)

Table 55. EEE Wake Error Counter (MMD3, 0x16)

Bit	Symbol	Access	Default	Description
15:0	Lpi_wake_err_cnt	RO RC SWC	0x0	Count wake time faults where the PHY fails to complete its normal wake sequence within the time required for the specific PHY type.

6.3.5. Local Device EEE Ability (MMD7, 0x3C)

Table 56. Local Device EEE Ability (MMD7, 0x3C)

Bit	Symbol	Access	Default	Description
15:3	Reserved	RO	0x0	Reserved
2	EEE_1000BT	RW	0x0	PHY's 1000BASE-T EEE ability.
1	EEE_100BT	RW	0x0	PHY's 100BASE-TX EEE ability.
0	Reserved	RO	0x0	Reserved

6.3.6. Link Partner EEE Ability (MMD7, 0x3D)

Table 57. Link Partner EEE Ability (MMD7, 0x3D)

Bit	Symbol	Access	Default	Description
15:3	Reserved	RO	0x0	Reserved
2	LP_ge_eee_ability	RO	0x0	Link partner's 1000BASE-T EEE ability.
1	LP_ge_eee_ability	RO	0x0	Link partner's 100BASE-TX EEE ability.
0	Reserved	RO	0x0	Reserved

6.4. UTP LDS Register For YT8531D/YT8531P

6.4.1. LRE Control (0x00)

Table 58. LRE Control (0x00)

Bit	Symbol	Access	Default	Description
15	Reset	RW SC	0x0	PHY Software Reset. Writing 1 to this bit causes immediate PHY reset. Once the operation is done, this bit is cleared automatically. 1'b0: Normal operation; 1'b1: PHY reset
14	Reserved	RW	0x0	Reserved
13	Restart_LDS	RW SC	0x0	1'b1: restart LDS process
12	LDS_Enable	RW	0x0	1'b1: LDS enabled; 1'b0: LDS disabled
11	Reserved	RW	0x0	Reserved
10	Reserved	RW	0x0	Reserved
9:6	Speed_selection	RW	0x0	4'b0000: 10Mbps; 4'b1000: 100Mbps; Others:

				reserved
5:4	Pair_selection	RW	0x0	2'b00: 1 pair connection; 2'b01: 2 pair connections; 2'b10: 4 pair connections; 2'b11: reserved
3	M/S_selection	RW	0x0	1'b1: manually force local device to master, when reg0.12 = 0; 1'b0: manually force local device to slave, when reg0.12 = 0
2	Reserved	RW	0x0	Reserved
1:0	Reserved	RO	0x0	Reserved. Write as 0, ignore on read

6.4.2. LRE Status (0x01)

Table 59. LRE Status (0x01)

Bit	Symbol	Access	Default	Description
15:14	Reserved	RO	0x0	Ignore on read
13	100Mbps_1-pair capable	RO	0x0	1'b1: 100Mbps 1-pair capable; 1'b0: Not 100Mbps 1-pair capable
12	100Mbps_4-pair capable	RO	0x1	1'b1: 100Mbps 4-pair capable; 1'b0: Not 100Mbps 4-pair capable
11	100Mbps_2-pair capable	RO	0x0	1'b1: 100Mbps 2-pair capable; 1'b0: Not 100Mbps 2-pair capable
10	10Mbps_2-pair capable	RO	0x0	1'b1: 10Mbps 2-pair capable; 1'b0: Not 10Mbps 2-pair capable
9	10Mbps_1-pair capable	RO	0x0	1'b1: 10Mbps 1-pair capable; 1'b0: Not 10Mbps 1-pair capable
8:6	Reserved	RO	0x7	Reserved
5	LDS_Complete	RO SWC	0x0	1'b1: LDS auto-negotiation complete; 1'b0: LDS auto-negotiation not complete
4	Support_IEEE_802.3 _PHY	RO	0x1	1'b1: Support IEEE 802.3 PHY operation; 1'b0: Not Support IEEE 802.3 PHY operation
3	LDS_Ability	RO	0x1	1'b1: LDS auto-negotiation capable; 1'b0: Not LDS auto-negotiation capable
2	Link_Status	RO LL SWC	0x0	Link status; 1'b0: Link is down; 1'b1: Link is up
1	Reserved	RO	0x0	Reserved
0	Reserved	RO	0x1	Reserved

6.4.3. PHY ID Register1 (0x02)

Table 60. PHY ID Register1 (0x02)

Bit	Symbol	Access	Default	Description
15:0	PHY_ID	RO	0x4F51	Bits 3 to 18 of the Organizationally Unique Identifier.

6.4.4. PHY ID Register2 (0x03)

Table 61. PHY ID Register2 (0x03)

Bit	Symbol	Access	Default	Description

15:10	Phy_Id	RO	0x3a	Bits 19 to 24 of the Organizationally Unique Identifier
9:4	Type_No	RO	0x11	6 bits manufacturer's type number
3:0	Revision_No	RO	0xb	4 bits manufacturer's revision number

6.4.5. LDS Auto-Negotiation Advertised Ability (0x04)

Table 62. LDS Auto-Negotiation Advertised Ability (0x04)

Bit	Symbol	Access	Default	Description
15:6	Reserved	RO	0x0	reserved
5	100Mbps_1-pair capable	RW	0x0	1'b1: 100Mbps 1-pair capable; 1'b0: Not 100Mbps 1-pair capable
4	100Mbps_4-pair capable	RW	0x1	1'b1: 100Mbps 4-pair capable; 1'b0: Not 100Mbps 4-pair capable
3	100Mbps_2-pair capable	RW	0x0	1'b1: 100Mbps 2-pair capable; 1'b0: Not 100Mbps 2-pair capable
2	10Mbps_2-pair capable	RW	0x0	1'b1: 10Mbps 2-pair capable; 1'b0: Not 10Mbps 2-pair capable
1	10Mbps_1-pair capable	RW	0x0	1'b1: 10Mbps 1-pair capable; 1'b0: Not 10Mbps 1-pair capable
0	IEEE802.3 Auto negotiation capable	RW	0x1	1'b1: IEEE802.3 Auto negotiation capable; 1'b0: Not IEEE802.3 auto negotiation capable

6.4.6. LDS Link Partner Ability (0x07)

Table 63. LDS Link Partner Ability (0x07)

Bit	Symbol	Access	Default	Description
15:6	Reserved	RO	0x0	Reserved
5	LP_100Mbps_1-pair_capable	RO	0x0	1'b1: link partner 100Mbps 1-pair capable; 1'b0: link partner not 100Mbps 1-pair capable
4	LP_100Mbps_4-pair_capable	RO	0x0	1'b1: link partner 100Mbps 4-pair capable; 1'b0: link partner not 100Mbps 4-pair capable
3	LP_100Mbps_2-pair_capable	RO	0x0	1'b1: link partner 100Mbps 2-pair capable; 1'b0: link partner not 100Mbps 2-pair capable
2	LP_10Mbps_2-pair_capable	RO	0x0	1'b1: link partner 10Mbps 2-pair capable; 1'b0: link partner not 10Mbps 2-pair capable
1	LP_10Mbps_1-pair_capable	RO	0x0	1'b1: link partner 10Mbps 1-pair capable; 1'b0: link partner not 10Mbps 1-pair capable
0	Reserved	RO	0x0	Reserved

6.4.7. LDS Expansion (0x0A)

Table 64. LDS Expansion (0x0A)

Bit	Symbol	Access	Default	Description
15	Reserved	RO	0x0	Reserved
14	Master/Slave	RO	0x0	1 = Local PHY configuration resolved to Master; 0 = Local PHY configuration resolved to Slave
13:12	Connections_pairs	RO	0x0	Number of pairs; 2'b00: 1 pair;

				2'b01: 2 pairs; 2'b10: 4 pairs; 2'b11: reserved
11:0	Estimated_cable_length	RO	0x0	Cable length measured via LDS.

6.4.8. LDS Results (0x0B)

Table 65. LDS Results (0x0B)

Bit	Symbol	Access	Default	Description
15:6	Reserved	RO	0x0	Reserved
5	4-pair_100M	RO	0x0	1'b1: local PHY configuration resolved to 4-pair 100M, LRE100-4
4	Auto_negotiation	RO	0x0	1'b1: local PHY configuration resolved to IEEE802.3 auto-negotiation
3:0	Reserved	RO	0x0	Reserved

6.5. UTP EXT Register

6.5.1. Pkgen Cfg1 (EXT_0x38)

Table 66. Pkgen Cfg1 (EXT_0x38)

Bit	Symbol	Access	Default	Description
15:13	Reserved	RO	0x0	Reserved
12	En_pkgen_da_sa	RW	0x0	1: set the DA/SA of the packet generated by pkg_gen to a programmed value; For DA, if UTP EXT 0x38 bit[11] is 1, the DA is set to broadcast address FF-FF-FF-FF-FF-FF; else, the DA is set to fix value, the highest 5 Bytes are 00-00-00-00-00, and the lowest 1 Byte is programmed by UTP EXT 0x3A bit[15:8]. For SA, the highest 5 Bytes are 00-00-00-00-00, and the lowest 1 Byte is programmed by UTP EXT 0x3A bit[7:0]. 0: the DA/SA is not programmed value
11	Pkgen_brdcst	RW	0x0	Valid when UTP EXT 0x38 bit12 is 1. 1: set the DA to broadcast address FF-FF-FF-FF-FF-FF 0: set the DA to a fixed programmed value.
10	Pkgchk_txsrc_sel	RW	0x0	1'b1: the package checker on TX side will check the tx data generated by pkg_gen; 1'b0: the package checker on TX side will check the tx data of UTP GMII/MII.
9	Pkgen_en_az	RW	0x0	1: to enable send LPI pattern during the IPG of the packages sent by pkg_gen.
8:0	Pkgen_in_az_t	RW	0x1ff	The time how long LPI pattern is sent, unit is us.

6.5.2. Pkgen Cfg2 (0x39)

Table 67. Pkgen Cfg2 (EXT_0x39)

Bit	Symbol	Access	Default	Description
15:8	Pkgen_pre_az_t	RW	0x20	The time from the end of last package to the

				beginning of LPI pattern, unit is us.
7:0	Pkgen_aft_az_t	RW	0x19	The time from the end of LPI pattern to the beginning of next package, unit is us.

6.5.3. Pkgen Cfg3 (EXT_0x3A)

Table 68. Pkgen Cfg3 (EXT_0x3A)

Bit	Symbol	Access	Default	Description
15:8	Pkgen_da	RW	0x0	Lowest 8 bits of DA, others is zero. Refer to UTP EXT 0x38 bit[12] for detail.
7:0	Pkgen_sa	RW	0x0	Lowest 8 bits of SA, others is zero. Refer to UTP EXT 0x38 bit[12] for detail.

6.5.4. Pkgen Cfg4 (0x3B)

Table 69. Pkgen Cfg4 (EXT_0x3B)

Bit	Symbol	Access	Default	Description
15:8	Reserved	RO	0x0	Reserved
7:0	Pkg_data_fix	RW	0x0	Valid when EXT 0xA0 bit1:0 is 11. The fixed GMII data pattern that will be sent.

6.5.5. Pkg Cfg0 (EXT_0xA0)

Table 70. Pkg Cfg0 (EXT_0xA0)

Bit	**Symbol**	**Access**	**Default**	**Description**
15	Pkg_chk_en	RW	0x0	1: to enable UTP RX/TX package checker. RX checker checks the UTP GMII/MII RX data; TX checker checks the UTP GMII/MII TX data.
14	Pkg_en_gate	RW	0x1	1: to enable gate all the clocks to package self-test module when bit15 pkg_chk_en is 0, bit13 bp_pkg_gen is 1 and bit12 pkg_gen_en is 0; 0: not gate the clocks.
13	Bp_pkg_gen	RW	0x1	1: normal mode, to send GMII/MII TX data from RGMII; 0: test mode, to send out the GMII/MII data generated by UTP pkg_gen module.
12	Pkg_gen_en	RW SC	0x0	1: to enable pkg_gen generating GMII/MII packages. But, the data will only be sent to transceiver when Bit13 bp_pkg_gen is 1'b0. If pkg_burst_size is 0, continuous packages will be generated and will be stopped only when pkg_gen_en is set to 0; Otherwise, after the expected packages are generated, pkg_gen will stop, pkg_gen_en will be self-cleared.
11:8	Pkg_prm_lth	RW	0x8	The preamble length of the generated packages, in Byte unit. Pkg_gen function only support >=2 Byte preamble length. Values smaller than 2 will be ignored by the pkg_gen module.
7:4	Pkg_ipg_lth	RW	0xd	The IPG of the generated packages, in Byte unit for setting smaller than 12. For setting 13, ipg is 2ms; for setting 14, ipg is 20ms; for 15, ipg is 400ms; Pkg_gen function only support >=2

				Byte preamble length. Values smaller than 2 will be ignored by the pkg_gen module.
3	Reserved	RW	0x0	Reserved
2	Pkg_corrupt_crc	RW	0x0	1: to make pkg_gen to send out CRC error packages. 0: pkg_gen sends out CRC good packages.
1:0	Pkg_payload	RW	0x0	Control the payload of the generated packages. 00: increased Byte payload; 01: random payload; 10: fix pattern 0x5AA55AA5… 11: fix pattern set by EXT 0x3B bit7:0.

6.5.6. Pkg Cfg1 (EXT_0xA1)

Table 71. Pkg Cfg1 (EXT_0xA1)

Bit	Symbol	Access	Default	Description
15:0	Pkg_length	RW	0x40	To set the length of the generated packages.

6.5.7. Pkg Cfg2 (EXT_0xA2)

Table 72. Pkg Cfg2 (EXT_0xA2)

Bit	Symbol	Access	Default	Description
15:0	Pkg_burst_size	RW	0x0	To set the number of packages in a burst of package generation.

6.5.8. Pkg Rx Valid0 (EXT_0xA3)

Table 73. Pkg Rx Valid0 (EXT_0xA3)

Bit	Symbol	Access	Default	Description
15:0	Pkg_ib_valid_high	RO RC	0x0	Pkg_ib_valid[31:16], pkg_ib_valid is the number of RX packages from wire whose CRC are good and length are >=64Byte and <=1518Byte.

6.5.9. Pkg Rx Valid1 (EXT_0xA4)

Table 74. Pkg Rx Valid1 (EXT_0xA4)

Bit	Symbol	Access	Default	Description
15:0	Pkg_ib_valid_low	RO RC	0x0	Pkg_ib_valid[15:0], pkg_ib_valid is the number of RX packages from wire whose CRC are good and length are >=64Byte and <=1518Byte.

6.5.10. Pkg Rx Os0 (EXT_0xA5)

Table 75. Pkg Rx Os0 (EXT_0xA5)

Bit	Symbol	Access	Default	Description
15:0	Pkg_ib_os_good_high	RO RC	0x0	Pkg_ib_os_good[31:16], pkg_ib_os_good is the number of RX packages from wire whose CRC are good and length are >1518Byte.

6.5.11. Pkg Rx Os1 (EXT_0xA6)

Table 76. Pkg Rx Os1 (EXT_0xA6)

Bit	Symbol	Access	Default	Description
15:0	Pkg_ib_os_good_low	RO RC	0x0	Pkg_ib_os_good[15:0], pkg_ib_os_good is the number of RX packages from wire whose CRC are good and length are >1518Byte.

6.5.12. Pkg Rx Us0 (EXT_0xA7)

Table 77. Pkg Rx Us0 (EXT_0xA7)

Bit	Symbol	Access	Default	Description
15:0	Pkg_ib_us_good_high	RO RC	0x0	Pkg_ib_us_good[31:16], pkg_ib_us_good is the number of RX packages from wire whose CRC are good and length are <64Byte.

6.5.13. Pkg Rx Us1 (EXT_0xA8)

Table 78. Pkg Rx Us1 (EXT_0xA8)

Bit	Symbol	Access	Default	Description
15:0	Pkg_ib_us_good_low	RO RC	0x0	Pkg_ib_us_good[15:0], pkg_ib_us_good is the number of RX packages from wire whose CRC are good and length are <64Byte.

6.5.14. Pkg Rx Err (EXT_0xA9)

Table 79. Pkg Rx Err (EXT_0xA9)

Bit	Symbol	Access	Default	Description
15:0	Pkg_ib_err	RO RC	0x0	pkg_ib_err is the number of RX packages from wire whose CRC are wrong and length are >=64Byte, <=1518Byte.

6.5.15. Pkg Rx Os Bad (EXT_0xAA)

Table 80. Pkg Rx Os Bad (EXT_0xAA)

Bit	Symbol	Access	Default	Description
15:0	Pkg_ib_os_bad	RO RC	0x0	pkg_ib_os_bad is the number of RX packages from wire whose CRC are wrong and length are >1518Byte.

6.5.16. Pkg Rx Fragment (EXT_0xAB)

Table 81. Pkg Rx Fragment (EXT_0xAB)

Bit	Symbol	Access	Default	Description
15:0	Pkg_ib_frag	RO RC	0x0	pkg_ib_frag is the number of RX packages from wire whose length are <64Byte.

6.5.17. Pkg Rx Nosfd (EXT_0xAC)

Table 82. Pkg Rx Nosfd (EXT_0xAC)

Bit	Symbol	Access	Default	Description

15:0	Pkg_ib_nosfd	RO RC	0x0	pkg_ib_nosfd is the number of RX packages from wire whose SFD is missed.

6.5.18. Pkg Tx Valid0 (EXT_0xAD)

Table 83. Pkg Tx Valid0 (EXT_0xAD)

Bit	Symbol	Access	Default	Description
15:0	Pkg_ob_valid_high	RO RC	0x0	Pkg_ob_valid[31:16], pkg_ob_valid is the number of TX packages from MII whose CRC are good and length are >=64Byte and <=1518Byte.

6.5.19. Pkg Tx Valid1 (EXT_0xAE)

Table 84. Pkg Tx Valid1 (EXT_0xAE)

Bit	Symbol	Access	Default	Description
15:0	Pkg_ob_valid_low	RO RC	0x0	Pkg_ob_valid[15:0], pkg_ob_valid is the number of TX packages from MII whose CRC are good and length are >=64Byte and <=1518Byte.

6.5.20. Pkg Tx Os0 (EXT_0xAF)

Table 85. Pkg Tx Os0 (EXT_0xAF)

Bit	Symbol	Access	Default	Description
15:0	Pkg_ob_os_good_high	RO RC	0x0	Pkg_ob_os_good[31:0], pkg_ob_os_good is the number of TX packages from GMII whose CRC are good and length are >1518Byte.

6.5.21. Pkg Tx Os1 (EXT_0xB0)

Table 86. Pkg Tx Os1 (EXT_0xB0)

Bit	Symbol	Access	Default	Description
15:0	Pkg_ob_os_good_low	RO RC	0x0	Pkg_ob_os_good[15:0], pkg_ob_os_good is the number of TX packages from GMII whose CRC are good and length are >1518Byte.

6.5.22. Pkg Tx Us0 (EXT_0xB1)

Table 87. Pkg Tx Us0 (EXT_0xB1)

Bit	Symbol	Access	Default	Description
15:0	Pkg_ob_us_good_high	RO RC	0x0	Pkg_ob_us_good[31:0], pkg_ob_us_good is the number of TX packages from GMII whose CRC are good and length are <64Byte.

6.5.23. Pkg Tx Us1 (EXT_0xB2)

Table 88. Pkg Tx Us1 (EXT_0xB2)

Bit	Symbol	Access	Default	Description
15:0	Pkg_ob_us_good_low	RO RC	0x0	Pkg_ob_us_good[15:0], pkg_ob_us_good is the

				number of TX packages from GMII whose CRC are good and length are <64Byte..

6.5.24. Pkg Tx Err (EXT_0xB3)

Table 89. Pkg Tx Err (EXT_0xB3)

Bit	Symbol	Access	Default	Description
15:0	Pkg_ob_err	RO RC	0x0	pkg_ob_err is the number of TX packages from GMII whose CRC are wrong and length are >=64Byte, <=1518Byte.

6.5.25. Pkg Tx Os Bad (EXT_0xB4)

Table 90. Pkg Tx Os Bad (EXT_0xB4)

Bit	Symbol	Access	Default	Description
15:0	Pkg_ob_os_bad	RO RC	0x0	pkg_ob_os_bad is the number of TX packages from GMII whose CRC are wrong and length are >=1518Byte.

6.5.26. Pkg Tx Fragment (EXT_0xB5)

Table 91. Pkg Tx Fragment (EXT_0xB5)

Bit	Symbol	Access	Default	Description
15:0	Pkg_ob_frag	RO RC	0x0	pkg_ob_frag is the number of TX packages from GMII whose length are <64Byte.

6.5.27. Pkg Tx Nosfd (EXT_0xB6)

Table 92. Pkg Tx Nosfd (EXT_0xB6)

Bit	Symbol	Access	Default	Description
15:0	Pkg_ob_nosfd	RO RC	0x0	pkg_ob_nosfd is the number of TX packages from GMII whose SFD is missed.

7. Timing and AC/DC Characteristics

7.1. DC Characteristics

Table 93. DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
Voh (3.3V)	Minimum High Level Output Voltage	2.4	-	3.63	V
Vol (3.3V)	Maximum Low Level Output Voltage	-0.3	-	0.4	V
Voh (2.5V)	Minimum High Level Output Voltage	2	-	2.8	V
Vol (2.5V)	Maximum Low Level Output Voltage	-0.3	-	0.4	V
Voh (1.8V)	Minimum High Level Output Voltage	1.62	-	2.1	V
Vol (1.8V)	Maximum Low Level Output Voltage	-0.3	-	0.4	V
Vih (3.3V)	Minimum High Level Input Voltage	2	-	-	V
Vil (3.3V)	Maximum Low Level Input Voltage	-	-	0.8	V
Vih (2.5V)	Minimum High Level Input Voltage	1.7	-	-	V
Vil (2.5V)	Maximum Low Level Input Voltage	-	-	0.7	V
Vih (1.8V)	Minimum High Level Input Voltage	1.2	-	-	V
Vil (1.8V)	Maximum Low Level Input Voltage	-	-	0.5	V

7.2. AC Characteristics

7.2.1. RGMII Timing w/o delay

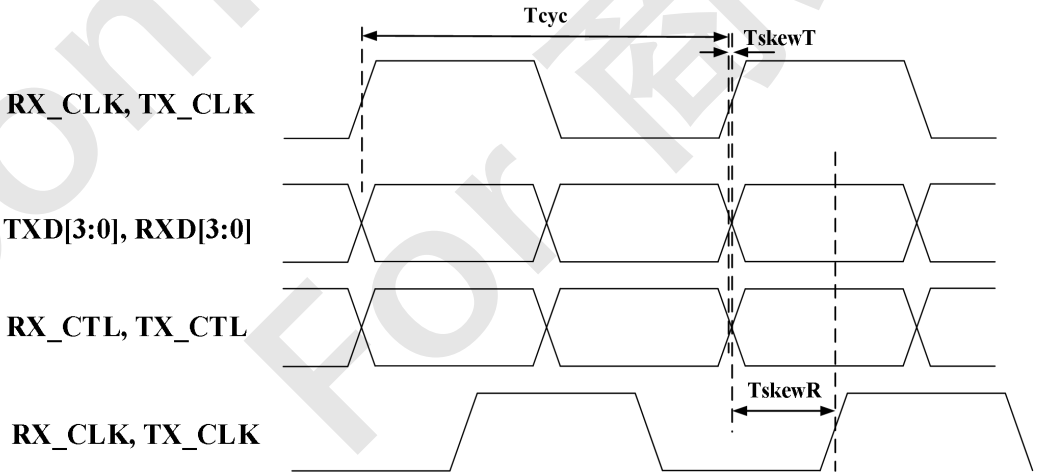


Figure 12. RGMII Timing w/o delay

Table 94. RGMII Timing w/o delay

Symbol	Parameter	Min	Typ	Max	Unit
TskewT	Data to clock output skew (at Transmitter)	-500	0	500	ps
TskewR	Data to clock output skew (at Receiver)	1	—	—	ns
Tcyc	Clock cycle duration	7.2	8.0	8.8	ns
Duty_G	Duty cycle for Gigabit	45	50	55	%
Duty_T	Duty cycle for 10/100T	40	50	60	%

7.2.2. RGMII Timing with internal delay

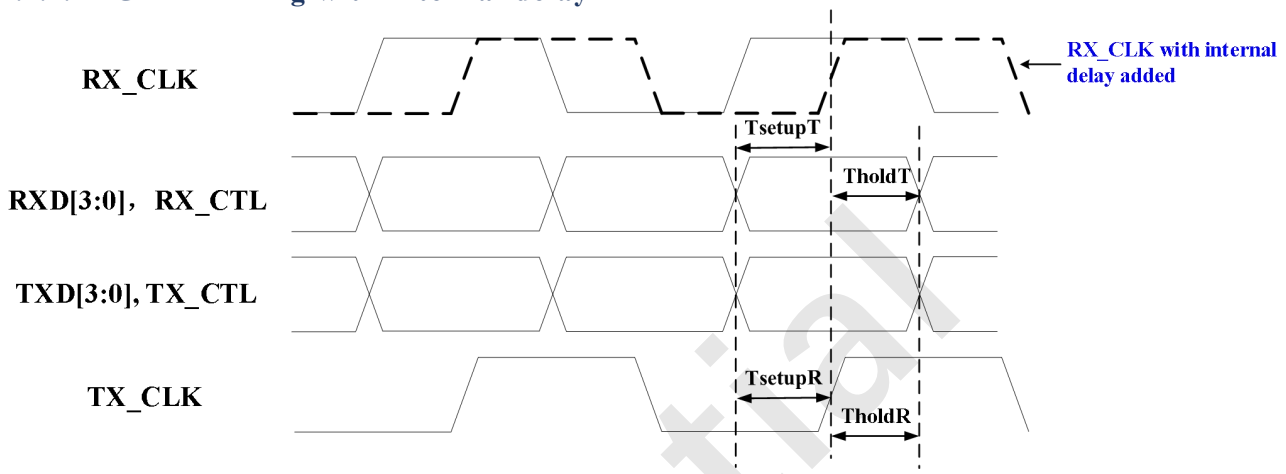


Figure 13. RGMII Timing with internal delay

Table 95. RGMII Timing with internal delay

Symbol	Parameter	Min	Typ	Max	Unit
TsetupT	Data to Clock output Setup Time (at Transmitter integrated delay)	1.0	2.0	-	ns
TholdT	Clock to Data output Hold Time (at Transmitter integrated delay)	1.0	2.0	-	ns
TsetupR	Data to Clock input Setup Time (at Receiver integrated delay)	1.0	2.0	-	ns
TholdR	Data to Clock input Hold Time (at Reciever integrated delay)	1.0	2.0	-	ns

7.2.3. SMI (MDC/MDIO) Interface Characteristics

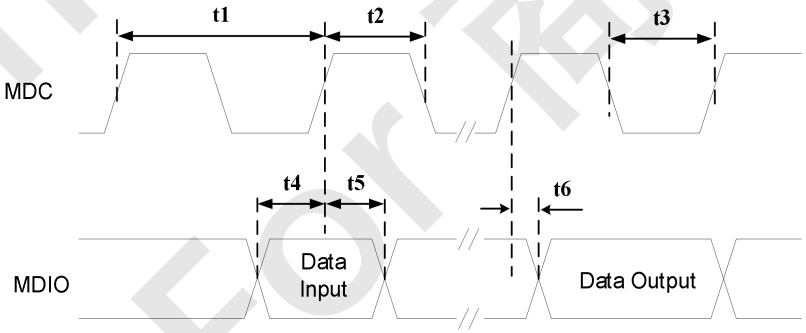


Figure 14. SMI (MDC/MDIO) Timing

Table 96. SMI (MDC/MDIO) Interface Characteristics

Symbol	Description	Min	Typ	Max	Units
t1	MDC Clock Period	80	-	-	ns
t2	MDC High Time	32	-	-	ns
t3	MDC Low Time	32	-	-	ns
t4	MDIO to MDC Rising Setup Time (Data Input)	10	-	-	ns
t5	MDIO to MDC Rising Hold Time (Data Input)	10	-	-	ns
t6	MDIO Valid from MDC rising edge (Data Output)	0	-	20	ns

7.3. Crystal Requirement

Table 97. Crystal Requirement

Symbol	Description	Min	Typ	Max	Unit
Fref	Parallel Resonant Crystal Reference Frequency	-	25	-	MHz
Fref Tolerance	Parallel Resonant Crystal Reference Frequency Tolerance	-50	-	50	ppm
Fref Duty Cycle	Reference Clock Input Duty Cycle	40	-	60	%
ESR	Equivalent Series Resistance	-	-	50	ohm
DL	Drive Level	-	-	0.5	mW
Vih	Crystal output high level	1.4	-	-	V
Vil	Crystal output low level	-	-	0.7	V

7.4. Oscillator/External Clock Requirement

Table 98. Oscillator/External Clock Requirement

Parameter	Min	Typ	Max	Unit
Frequency	-	25	-	MHz
Frequency tolerance	-50	-	50	PPM
Duty Cycle	40	-	60	%
Vih	1.4	-	AVDD33+0.3	V
Vil	-	-	0.7	V
Rise Time (10%~90%)	-	-	10	ns
Fall Time (10%~90%)	-	-	10	ns

8. Power Requirements

8.1. Absolute Maximum Ratings

Table 99. Absolute Maximum Ratings

Symbol	Description	Mini	Max	Unit
VDD33/AVDD33	Supply Voltage 3.3V	-0.3	3.7	V
AVDDL/DVDDL	Supply Voltage 1.1V	-0.2	1.4	V
2.5V RGMII	Supply Voltage 2.5V	-0.3	2.8	V
1.8V RGMII	Supply Voltage 1.8V	-0.3	2.3	V
3.3V DC input	Input Voltage	-0.3	3.7	V
VDDL DC input	Input Voltage	-0.3	1.4	V

8.2. Recommended Operating Conditions

Table 100. Recommended Operating Conditions

Description	Pins	Min	Typ	Max	Unit
Supply Voltage	DVDD33, AVDD33	3.14	3.3	3.63	V
	AVDDL, DVDDL	1.045	1.1	1.32	V
	2.5V RGMII	2.25	2.5	2.75	V
	1.8V RGMII	1.62	1.8	1.98	V
YT8531C Ambient Operating Temperature Ta		0	-	70	°C
YT8531H Ambient Operating Temperature Ta		-40	-	85	°C
YT8531DC Ambient Operating Temperature Ta		0	-	70	°C
YT8531DH Ambient Operating Temperature Ta		-40	-	85	°C
YT8531P Ambient Operating Temperature Ta		0	-	70	°C
Maximum Junction Temperature				125	°C

8.3. Power Sequence

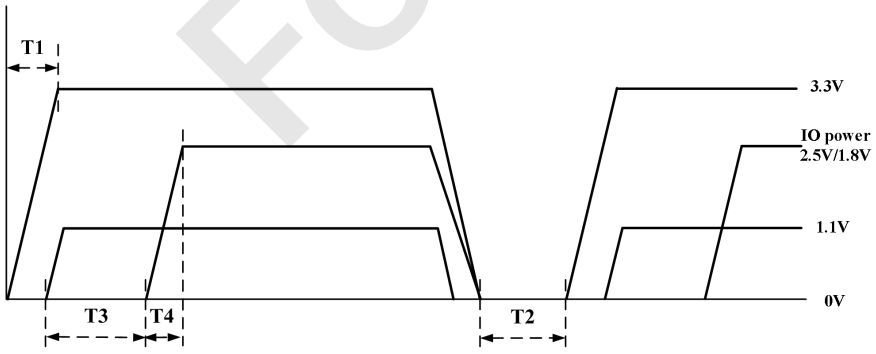


Figure 15. Power Sequence Diagram

Table 101. Power Sequence Timing Parameters

Symbol	Description	Min	Typ	Max	Units
T1	3.3V rising time	0.5	-	-	ms
T2	3.3V and 1.1V power down duration	100	-	-	ms
T3	Core power 1.1V ready time	-	-	2.5	ms

T4	Internal LDO ready time	-	-	100	us

8.4. Power Consumption

8.4.1. YT8531 Power Consumption

Table 102. YT8531 Power Consumption

Condition	DVDD_RGMII (mA)	DVDD33 + VDD33_LX (mA)	AVDD33 (mA)	Power Consumption (mW)
Link Down	1	7	21	95.7
Link Up @1000Mbps	13	51	61	412.5
Traffic @1000Mbps	28	57	61	481.8

Note: Test by YT8531C/YT8531H TT IC with DVDD_RGMII / DVDD33 / VDD33_LX / AVDD33 = 3.3V and VDDL = 1.1V (with inductor SWPA3012S2R2NT connected to REG_O (pin30)) at room temperature.

8.4.2. YT8531D Power Consumption

Table 103. YT8531D Power Consumption

Condition	DVDD_RGMII (mA)	DVDD33 + VDD33_LX (mA)	AVDD33 (mA)	Power Consumption (mW)
Link Down	1	21	21	95.7
Link Up @1000Mbps	13	127	61	663.3
Traffic @1000Mbps	28	137	61	745.8

Note: Test by YT8531DC/YT8531DH TT IC with DVDD_RGMII / DVDD33 / VDD33_LX / AVDD33 = 3.3V and VDDL = 1.1V (with 0ohm resistance connected to LDO_O (pin30)) at room temperature.

8.4.3. YT8531P Power Consumption

Table 104. YT8531P Power Consumption

Condition	DVDD_RGMII (mA)	DVDD33 (mA)	AVDD33 (mA)	VDDL (mA)	Power Consumption (mW)
Link Down	1	1	21	18	95.7
Link Up @1000Mbps	18	5	61	117	405.9
Traffic @1000Mbps	34	5	61	128	470.8

Note: Test by YT8531P TT IC with DVDD_RGMII / DVDD33 / VDD33_LX / AVDD33 = 3.3V and VDDL = 1.1V from external at room temperature.

8.5. Maximum Power Consumption

8.5.1. YT8531 Maximum Power Consumption

Table 105. YT8531 Maximum Power Consumption

Condition	DVDD_RGMII (mA)	DVDD33 + VDD33_LX (mA)	AVDD33 (mA)	Power Consumption (mW)
Traffic @1000Mbps	30.8	62.7	67.1	530.0

Note: Test by YT8531H FF IC with DVDD_RGMII / DVDD33 / VDD33_LX / AVDD33 = 3.3V and VDDL = 1.1V (with inductor SWPA3012S2R2NT connected to REG_O (pin30)) at high temperature 85℃.

8.5.2. YT8531D Maximum Power Consumption

Table 106. YT8531D Maximum Power Consumption

Condition	DVDD_RGMII (mA)	DVDD33 + VDD33_LX (mA)	AVDD33 (mA)	Power Consumption (mW)
Traffic @1000Mbps	30.8	150.7	67.1	820.4

Note: Test by YT8531DH FF IC with DVDD_RGMII / DVDD33 / VDD33_LX / AVDD33 = 3.3V and VDDL = 1.1V (with 0ohm resistance connected to LDO_O (pin30)) at high temperature 85℃.

8.5.3. YT8531P Maximum Power Consumption

Table 107. YT8531P Maximum Power Consumption

Condition	DVDD_RGMII (mA)	DVDD33 (mA)	AVDD33 (mA)	VDDL (mA)	Power Consumption (mW)
Traffic @1000Mbps	37.4	5.5	67.1	140.8	517.9

Note: Test by YT8531P FF IC with DVDD_RGMII / DVDD33 / VDD33_LX / AVDD33 = 3.3V and VDDL = 1.1V from external at high temperature 85℃.

8.6. Power Ripple

The max ripple of 3.3V should be under 100mV, that of DVDDL should be under 80mV, and that of AVDDL should be under 50mV.

9. Thermal Resistance

Table 108. Thermal Resistance

Symbol	Parameter	Conditon	Typ	Units
θ_{JA}	Thermal resistance - junction to ambient $\theta_{JA} = (T_J - T_A)/ P$ P = Total power dissipation	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow TA=25°C	33.4	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow TA=85°C	31	°C/W
θ_{JB}	Thermal resistance - junction to board $\theta_{JB} = (T_J - T_B)/ P_{bottom}$ P_{bottom} = Power dissipation from the bottom of the package to the PCB surface.	JEDEC with no air flow	12.3	°C/W
θ_{JC_Top}	Thermal resistance - junction to case $\theta_{JC} = (T_J - T_C)/ P_{top}$ P_{top} = Power dissipation from the top of the package	JEDEC with no air flow	28.4	°C/W

10. Mechanical Information

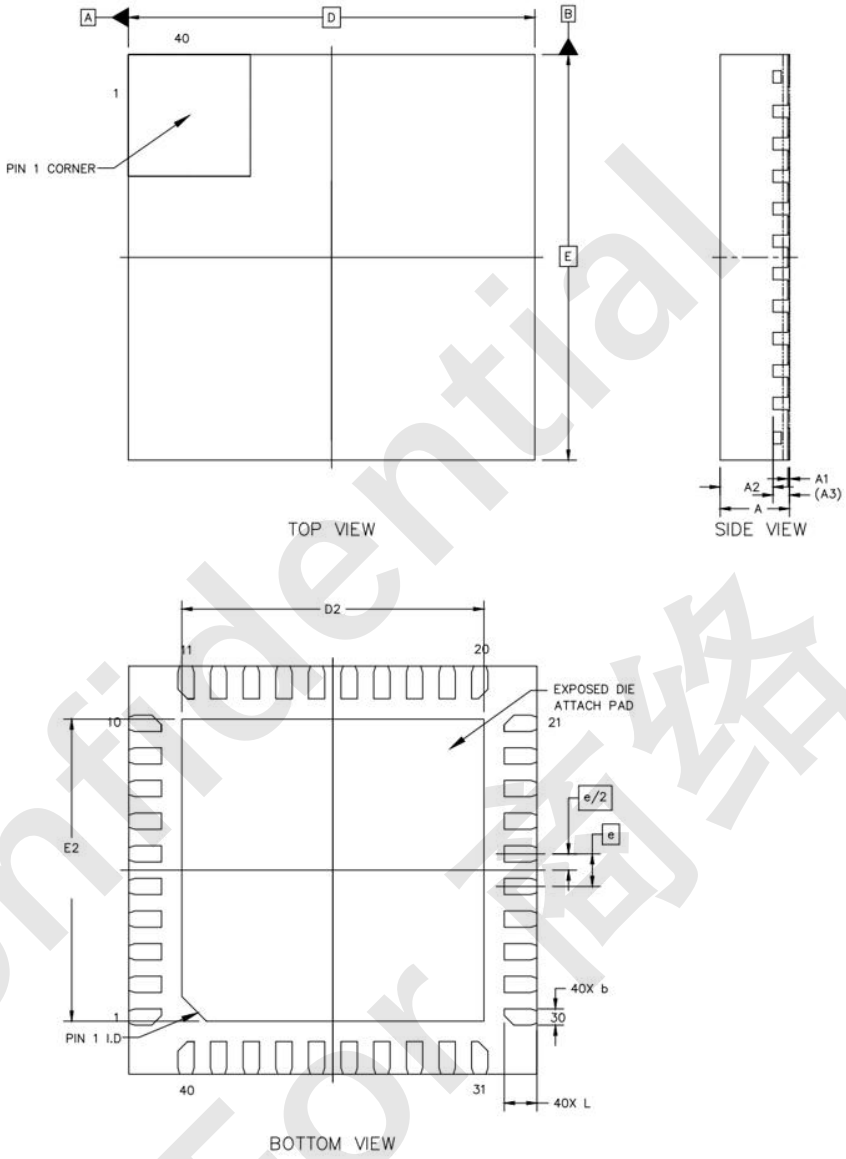


Table 109. Mechanical Dimensions

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.80	0.85	0.90
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3	0.203 REF		
LEAD WIDTH		b	0.15	0.20	0.25
BODY SIZE	X	D	5.00 BSC		
	Y	E	5.00 BSC		
LEAD PITCH		e	0.40 BSC		
EP SIZE	X	D2	3.50	3.70	3.90
	Y	E2	3.50	3.70	3.90
LEAD LENGTH		L	0.30	0.40	0.50

11. Ordering Information

Motorcomm offers a RoHS package that is compliant with RoHS.

Table 110. Ordering Information

Part Number	Grade	Package	Pack	Status	Operation Temp
YT8531C-CA	Consumer	QFN 40 5x5 mm	Tape Reel 3000ea		0 ~70°C
YT8531H-CA	Industrial	QFN 40 5x5 mm	Tape Reel 3000ea		-40 ~ 85°C
YT8531DC-CA	Consumer	QFN 40 5x5 mm	Tape Reel 3000ea		0 ~70°C
YT8531DH-CA	Industrial	QFN 40 5x5 mm	Tape Reel 3000ea		-40 ~ 85°C
YT8531P-CA	Consumer	QFN 40 5x5 mm	Tape Reel 3000ea		0 ~70°C