

B25NM50N-VB TO263 Datasheet

N-Channel 500-V (D-S) Super Junction MOSFET

| PRODUCT SUMMARY | |
|--|--------------------------------|
| V _{DS} (V) at T _J max. | 500 |
| R _{DS(on)} at 25 °C (Ω) | V _{GS} = 10 V 0.115 |
| Q _g (Max.) (nC) | 86 |
| Q _{gs} (nC) | 14 |
| Q _{gd} (nC) | 25 |
| Configuration | Single |

FEATURES

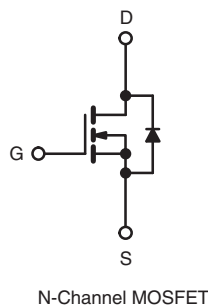
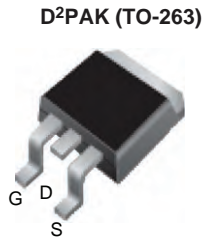
- Low figure-of-merit (FOM): R_{on} x Q_g
- Low input capacitance (C_{iss})
- Reduced switching and conduction losses
- Low gate charge (Q_g)
- Avalanche energy rated (UIS)



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APPLICATIONS

- Hard switched topologies
- Power factor correction power supplies (PFC)
- Switch mode power supplies (SMPS)
- Computing
 - PC silver box / ATX power supplies
- Lighting
 - Two stage LED lighting




| ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted) | | | | |
|---|---|-------------------------|-------------|------|
| PARAMETER | SYMBOL | | LIMIT | UNIT |
| Drain-Source Voltage | V _{DS} | | 500 | V |
| Gate-Source Voltage | V _{GS} | | ± 30 | |
| Continuous Drain Current (T _J = 150 °C) | V _{GS} at 10 V | T _C = 25 °C | 30 | A |
| | | T _C = 100 °C | 18 | |
| Pulsed Drain Current ^a | I _{DM} | | 105 | |
| Linear Derating Factor | | | 0.2 | W/°C |
| Single Pulse Avalanche Energy ^b | E _{AS} | | 273 | mJ |
| Maximum Power Dissipation | P _D | | 280 | W |
| Operating Junction and Storage Temperature Range | T _J , T _{stg} | | -55 to +150 | °C |
| Drain-Source Voltage Slope | V _{DS} = 0 V to 80 % V _{DS} | | 65 | V/ns |
| Reverse Diode dV/dt ^d | | | 25 | |
| Soldering Recommendations (Peak Temperature) ^c | for 10 s | | 300 | °C |

Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- V_{DD} = 50 V, starting T_J = 25 °C, L = 28.2 mH, R_g = 25 Ω, I_{AS} = 4.4 A.
- 1.6 mm from case.
- I_{SD} ≤ I_D, dI/dt = 100 A/μs, starting T_J = 25 °C.

| THERMAL RESISTANCE RATINGS | | | | |
|----------------------------------|-------------------|------|------|------|
| PARAMETER | SYMBOL | TYP. | MAX. | UNIT |
| Maximum Junction-to-Ambient | R _{thJA} | - | 40 | °C/W |
| Maximum Junction-to-Case (Drain) | R _{thJC} | - | 0.5 | |

| SPECIFICATIONS (T _J = 25 °C, unless otherwise noted) | | | | | | |
|---|----------------------------------|--|-----------------------|-------|-------|------|
| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
| Static | | | | | | |
| Drain-Source Breakdown Voltage | V _{DS} | V _{GS} = 0 V, I _D = 250 μA | 500 | - | - | V |
| V _{DS} Temperature Coefficient | ΔV _{DS} /T _J | Reference to 25 °C, I _D = 1 mA | - | 0.59 | - | V/°C |
| Gate-Source Threshold Voltage (N) | V _{GS(th)} | V _{DS} = V _{GS} , I _D = 250 μA | 2.0 | - | 4.0 | V |
| Gate-Source Leakage | I _{GSS} | V _{GS} = ± 20 V | - | - | ± 100 | nA |
| | | V _{GS} = ± 30 V | - | - | ± 1 | μA |
| Zero Gate Voltage Drain Current | I _{DSS} | V _{DS} = 500 V, V _{GS} = 0 V | - | - | 1 | μA |
| | | V _{DS} = 400 V, V _{GS} = 0 V, T _J = 125 °C | - | - | 25 | |
| Drain-Source On-State Resistance | R _{DS(on)} | V _{GS} = 10 V, I _D = 12 A | - | 0.115 | - | Ω |
| Forward Transconductance | g _{fs} | V _{DS} = 30 V, I _D = 12 A | - | 6.6 | - | S |
| Dynamic | | | | | | |
| Input Capacitance | C _{iss} | V _{GS} = 0 V, V _{DS} = 100 V, f = 1 MHz | - | 1980 | - | pF |
| Output Capacitance | C _{oss} | | - | 105 | - | |
| Reverse Transfer Capacitance | C _{rss} | | - | 8 | - | |
| Effective Output Capacitance, Energy Related ^a | C _{o(er)} | | - | 105 | - | |
| Effective Output Capacitance, Time Related ^b | C _{o(tr)} | V _{DS} = 0 V to 400 V, V _{GS} = 0 V | - | 285 | - | |
| Total Gate Charge | Q _g | V _{GS} = 10 V, I _D = 12 A, V _{DS} = 400 V | - | 57 | 86 | nC |
| Gate-Source Charge | Q _{gs} | | - | 14 | - | |
| Gate-Drain Charge | Q _{gd} | | - | 25 | - | |
| Turn-On Delay Time | t _{d(on)} | V _{DD} = 400 V, I _D = 12 A R _g = 9.1 Ω, V _{GS} = 10 V | - | 19 | 38 | ns |
| Rise Time | t _r | | - | 36 | 72 | |
| Turn-Off Delay Time | t _{d(off)} | | - | 57 | 86 | |
| Fall Time | t _f | | - | 29 | 58 | |
| Gate Input Resistance | R _g | | f = 1 MHz, open drain | - | 0.56 | |
| Drain-Source Body Diode Characteristics | | | | | | |
| Continuous Source-Drain Diode Current | I _S | MOSFET symbol showing the integral reverse p - n junction diode  | - | - | 12 | A |
| Pulsed Diode Forward Current | I _{SM} | | - | - | 50 | |
| Diode Forward Voltage | V _{SD} | T _J = 25 °C, I _S = 16.5 A, V _{GS} = 0 V | - | - | 1.2 | V |
| Reverse Recovery Time | t _{rr} | T _J = 25 °C, I _F = I _S , dI/dt = 100 A/μs, V _R = 25 V | - | 338 | - | ns |
| Reverse Recovery Charge | Q _{rr} | | - | 5.3 | - | μC |
| Reverse Recovery Current | I _{RRM} | | - | 29 | - | A |

Notes

- C_{oss(er)} is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}.
- C_{oss(tr)} is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

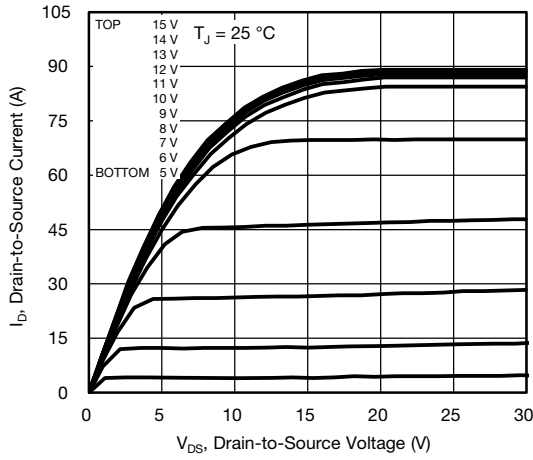


Fig. 1 - Typical Output Characteristics

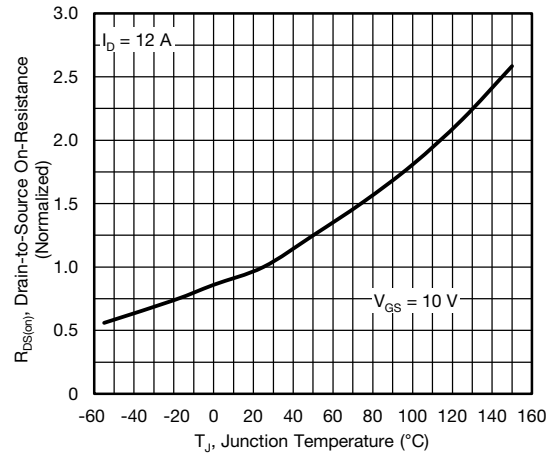


Fig. 4 - Normalized On-Resistance vs. Temperature

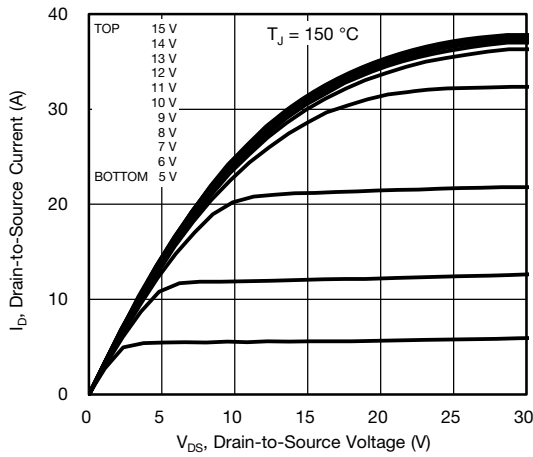


Fig. 2 - Typical Output Characteristics

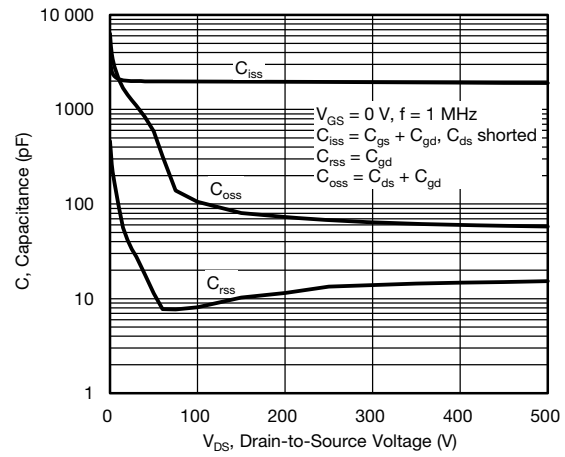


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

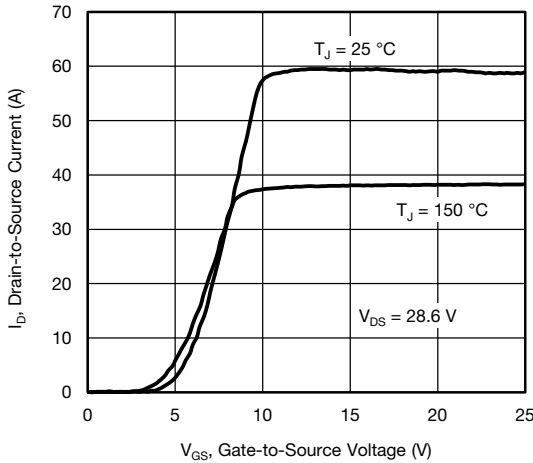


Fig. 3 - Typical Transfer Characteristics

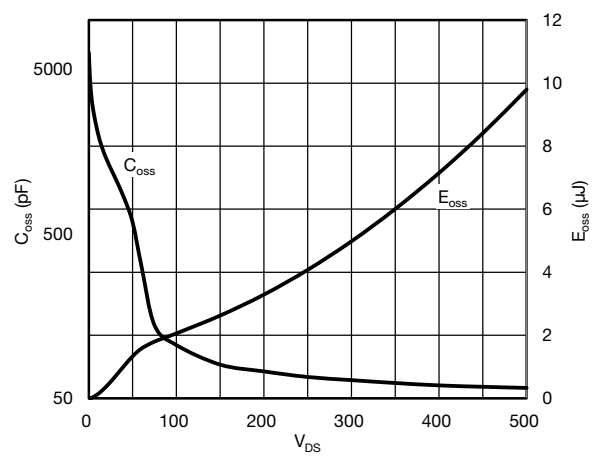


Fig. 6 - Coss and Eoss vs. Vds

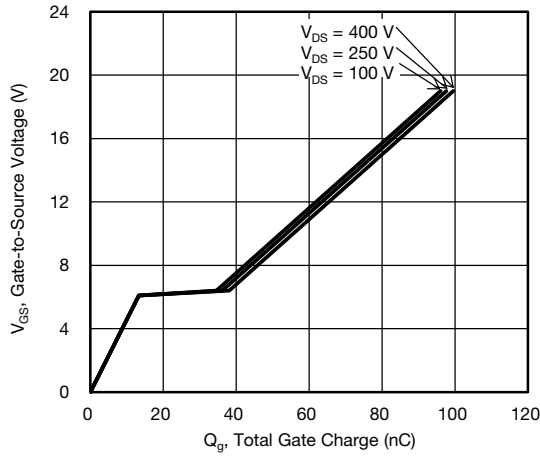


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

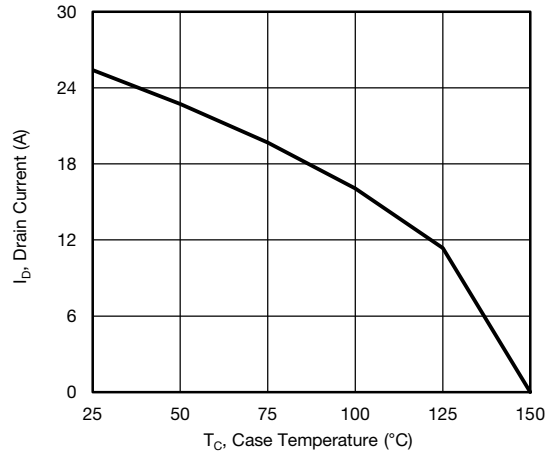


Fig. 10 - Maximum Drain Current vs. Case Temperature

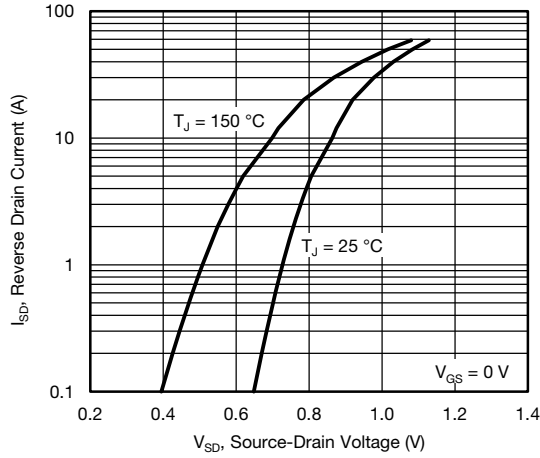


Fig. 8 - Typical Source-Drain Diode Forward Voltage

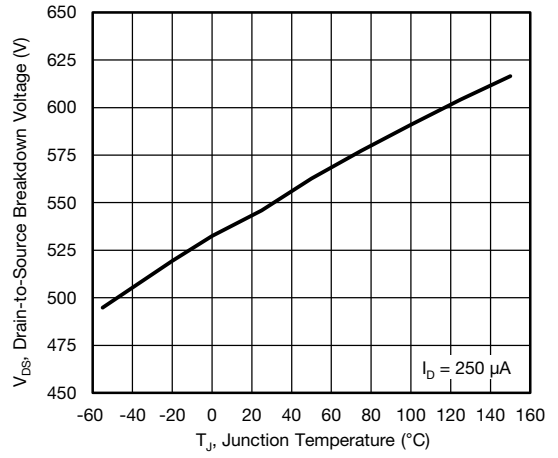


Fig. 11 - Typical Drain-to-Source Voltage vs. Temperature

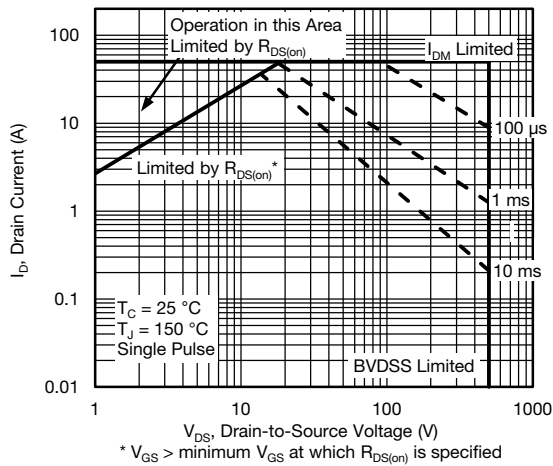


Fig. 9 - Maximum Safe Operating Area

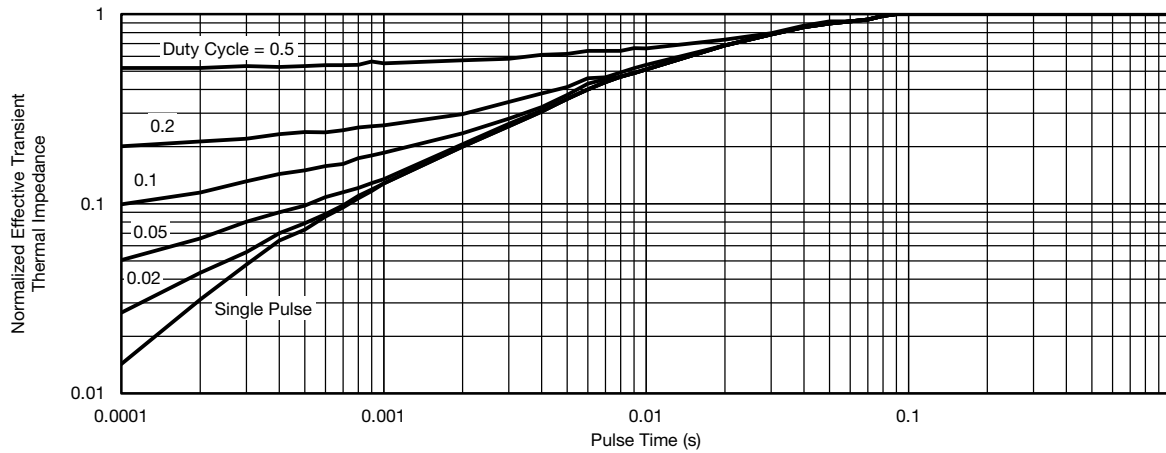


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

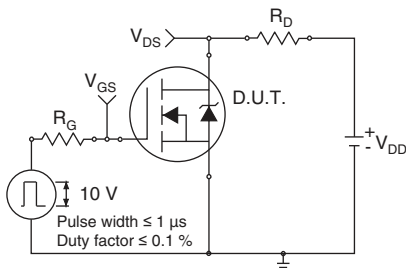


Fig. 13 - Switching Time Test Circuit

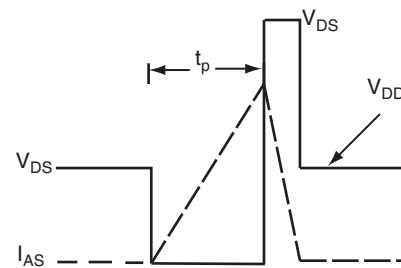


Fig. 16 - Unclamped Inductive Waveforms

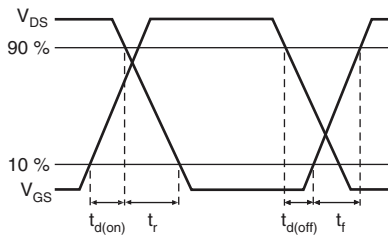


Fig. 14 - Switching Time Waveforms

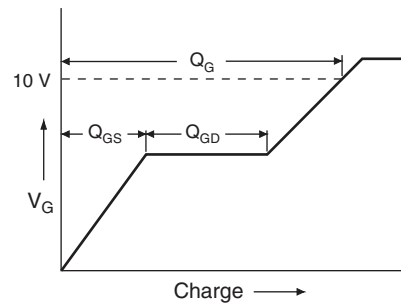


Fig. 17 - Basic Gate Charge Waveform

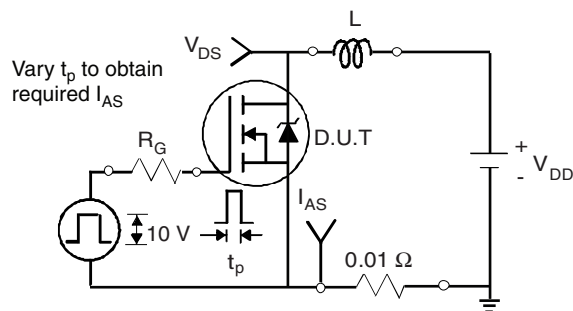


Fig. 15 - Unclamped Inductive Test Circuit

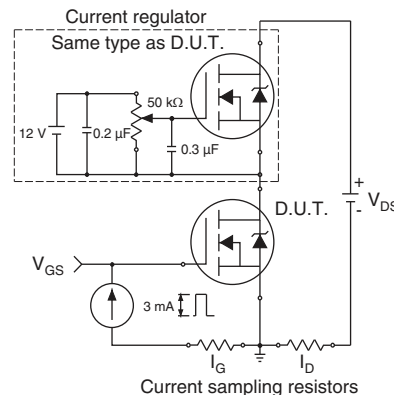
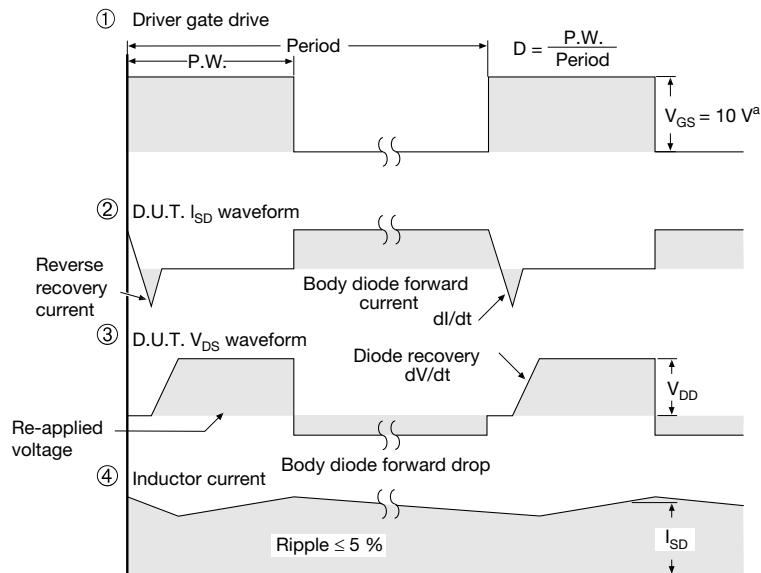
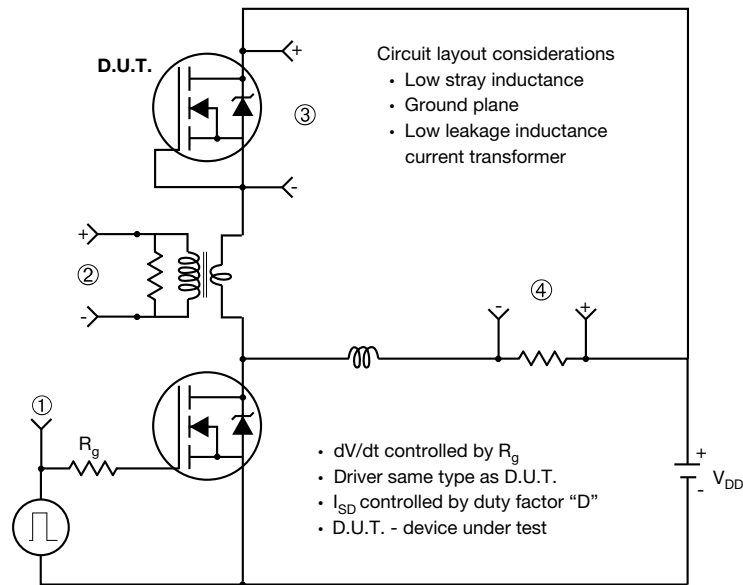


Fig. 18 - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit

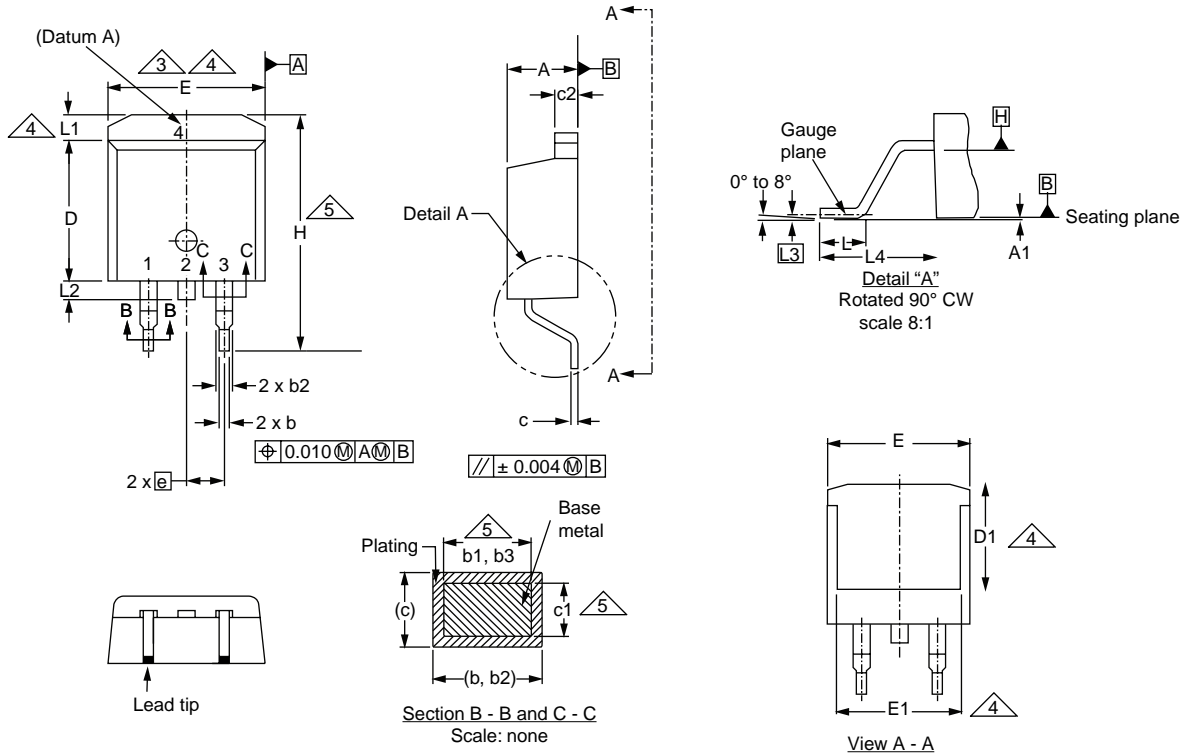


Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 19 - For N-Channel

TO-263AB (HIGH VOLTAGE)



| DIM. | MILLIMETERS | | INCHES | |
|------|-------------|------|--------|-------|
| | MIN. | MAX. | MIN. | MAX. |
| A | 4.06 | 4.83 | 0.160 | 0.190 |
| A1 | 0.00 | 0.25 | 0.000 | 0.010 |
| b | 0.51 | 0.99 | 0.020 | 0.039 |
| b1 | 0.51 | 0.89 | 0.020 | 0.035 |
| b2 | 1.14 | 1.78 | 0.045 | 0.070 |
| b3 | 1.14 | 1.73 | 0.045 | 0.068 |
| c | 0.38 | 0.74 | 0.015 | 0.029 |
| c1 | 0.38 | 0.58 | 0.015 | 0.023 |
| c2 | 1.14 | 1.65 | 0.045 | 0.065 |
| D | 8.38 | 9.65 | 0.330 | 0.380 |

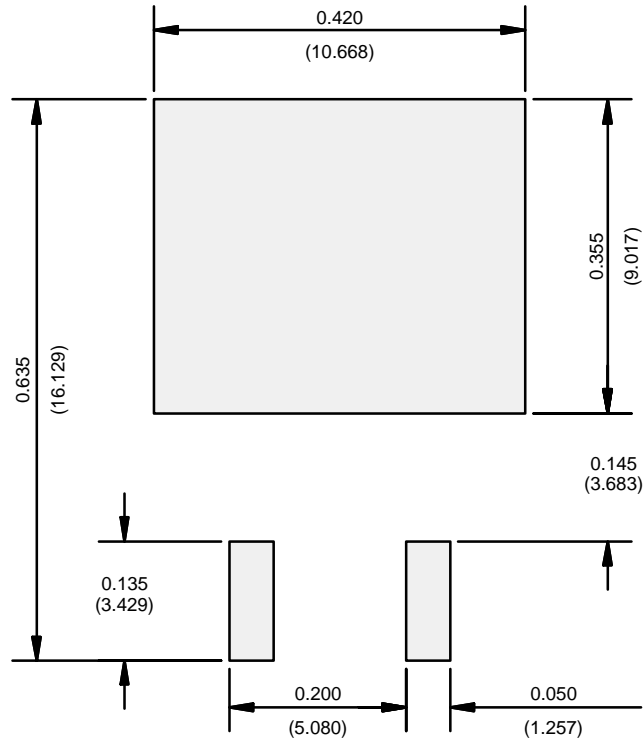
| DIM. | MILLIMETERS | | INCHES | |
|------|-------------|-------|-----------|-------|
| | MIN. | MAX. | MIN. | MAX. |
| D1 | 6.86 | - | 0.270 | - |
| E | 9.65 | 10.67 | 0.380 | 0.420 |
| E1 | 6.22 | - | 0.245 | - |
| e | 2.54 BSC | | 0.100 BSC | |
| H | 14.61 | 15.88 | 0.575 | 0.625 |
| L | 1.78 | 2.79 | 0.070 | 0.110 |
| L1 | - | 1.65 | - | 0.066 |
| L2 | - | 1.78 | - | 0.070 |
| L3 | 0.25 BSC | | 0.010 BSC | |
| L4 | 4.78 | 5.28 | 0.188 | 0.208 |

ECN: S-82110-Rev. A, 15-Sep-08
DWG: 5970

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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