

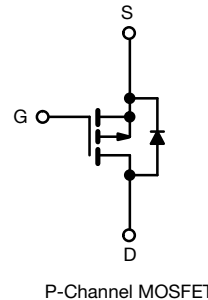
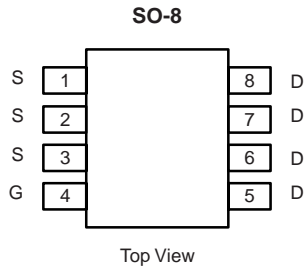
## AP15TP1R0M-VB Datasheet

### P-Channel 200V (D-S)MOSFET

PRODUCT SUMMARY	
$V_{DS}$ (V)	-200
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = -10\text{ V}$ 2.0
$Q_g$ max. (nC)	29
$Q_{gs}$ (nC)	5.4
$Q_{gd}$ (nC)	15
Configuration	Single

#### FEATURES

- Surface mount
- Available in tape and reel
- Dynamic dV/dt rating
- Repetitive avalanche rated
- P-channel
- Fast switching
- Ease of paralleling



ABSOLUTE MAXIMUM RATINGS ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	$V_{DS}$	-200	V	
Gate-Source Voltage	$V_{GS}$	$\pm 20$		
Continuous Drain Current	$V_{GS}$ at -10 V	$T_C = 25\text{ }^\circ\text{C}$	-3.6	A
		$T_C = 100\text{ }^\circ\text{C}$	-2.5	
Pulsed Drain Current <sup>a</sup>		$I_{DM}$	-12	W/ $^\circ\text{C}$
Linear Derating Factor			0.59	
Linear Derating Factor (PCB mount) <sup>e</sup>			0.025	
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	500	mJ	
Avalanche Current <sup>a</sup>	$I_{AR}$	-6.4	A	
Repetitive Avalanche Energy <sup>a</sup>	$E_{AR}$	7.4	mJ	
Maximum Power Dissipation	$P_D$	$T_C = 25\text{ }^\circ\text{C}$	74	W
Maximum Power Dissipation (PCB mount) <sup>e</sup>		$T_A = 25\text{ }^\circ\text{C}$	3.0	
Peak Diode Recovery dV/dt <sup>c</sup>	dV/dt	-5.0	V/ns	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$	
Soldering Recommendations (Peak temperature) <sup>d</sup>	for 10 s	300		

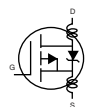

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = -50\text{ V}$ , starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 17\text{ mH}$ ,  $R_g = 25\text{ }\Omega$ ,  $I_{AS} = -6.5\text{ A}$  (see fig. 12).
- $I_{SD} \leq -6.5\text{ A}$ ,  $dI/dt \leq 120\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150\text{ }^\circ\text{C}$ .
- 1.6 mm from case.
- When mounted on 1" square PCB (FR-4 or G-10 material).

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	62	°C/W
Maximum Junction-to-Ambient (PCB mount) <sup>a</sup>	$R_{thJA}$	-	40	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	1.7	

**Note**

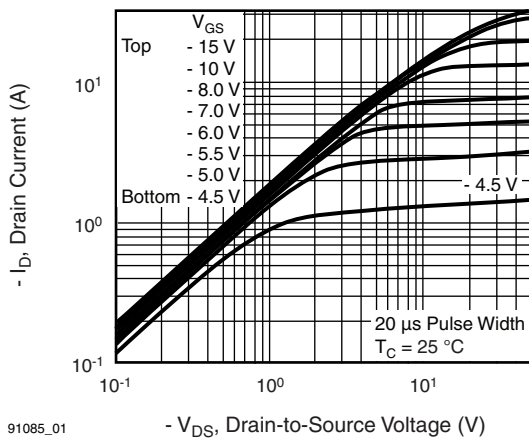
a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0, I_D = -250\text{ }\mu\text{A}$	-200	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = -1\text{ mA}$	-	-0.24	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-1.5	-	-4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$	-	-	$\pm 10$	$\mu\text{A}$
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -200\text{ V}, V_{GS} = 0\text{ V}$	-	-	-100	$\mu\text{A}$
		$V_{DS} = -160\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	-500	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -1.0\text{ A}^b$	-	2.00	-	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = -50\text{ V}, I_D = -1.0\text{ A}^b$	2.8	-	-	S
<b>Dynamic</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = -25\text{ V}, f = 1.0\text{ MHz}$ , see fig. 5	-	700	-	pF
Output Capacitance	$C_{oss}$		-	200	-	
Reverse Transfer Capacitance	$C_{rss}$		-	40	-	
Total Gate Charge	$Q_g$	$V_{GS} = -10\text{ V}, I_D = -3.5\text{ A}, V_{DS} = -160\text{ V}$ , see fig. 6 and 13 <sup>b</sup>	-	-	29	nC
Gate-Source Charge	$Q_{gs}$		-	-	5.4	
Gate-Drain Charge	$Q_{gd}$		-	-	15	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -100\text{ V}, I_D = -3.5\text{ A}, R_g = 12\text{ }\Omega, R_D = 15\text{ }\Omega$ , see fig. 10 <sup>b</sup>	-	12	-	ns
Rise Time	$t_r$		-	27	-	
Turn-Off Delay Time	$t_{d(off)}$		-	28	-	
Fall Time	$t_f$		-	24	-	
Internal Drain Inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact 	-	4.5	-	nH
Internal Source Inductance	$L_S$		-	7.5	-	
Gate Input Resistance	$R_g$	$f = 1\text{ MHz}$ , open drain	0.6	-	3.7	$\Omega$
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	-3.5	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$		-	-	-6	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = -3.5\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	-6.5	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = -3.5\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b$	-	200	300	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$		-	1.9	2.9	$\mu\text{C}$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )				

**Notes**

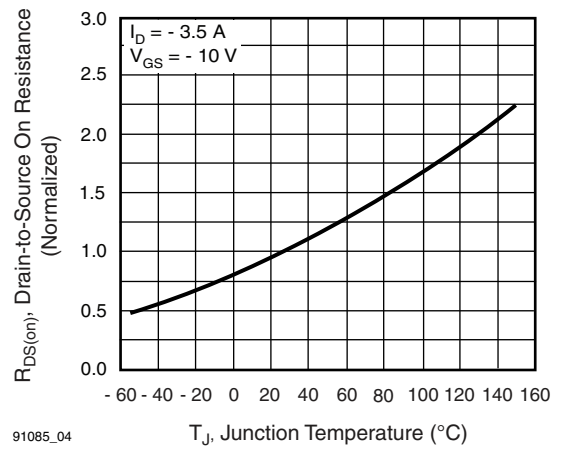
- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



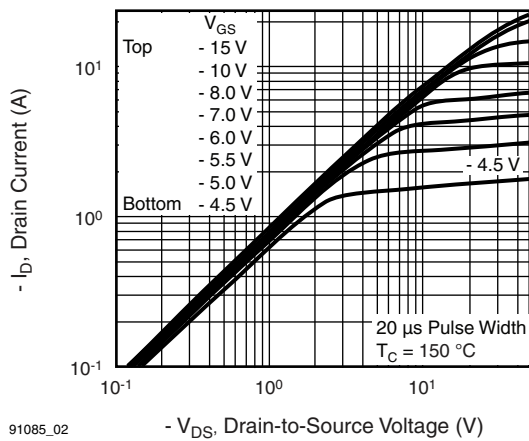
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**Fig. 1 - Typical Output Characteristics, T<sub>C</sub> = 25 °C**



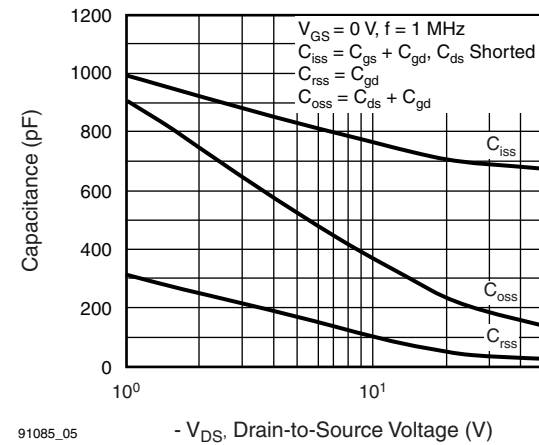
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**Fig. 4 - Normalized On-Resistance vs. Temperature**



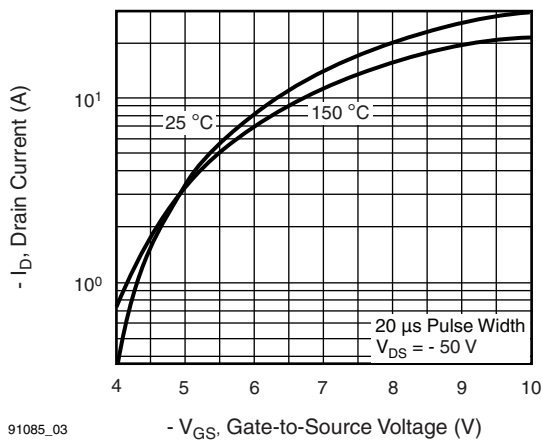
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**Fig. 2 - Typical Output Characteristics, T<sub>C</sub> = 150 °C**



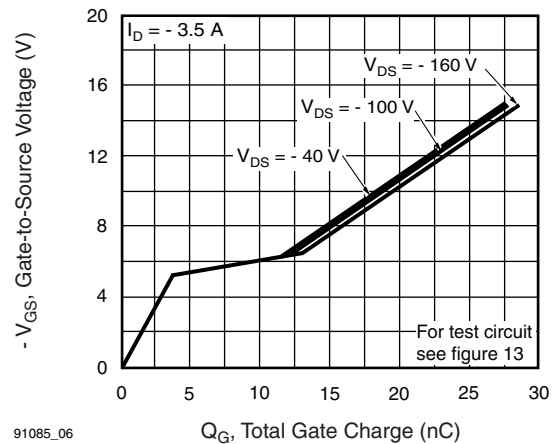
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**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**



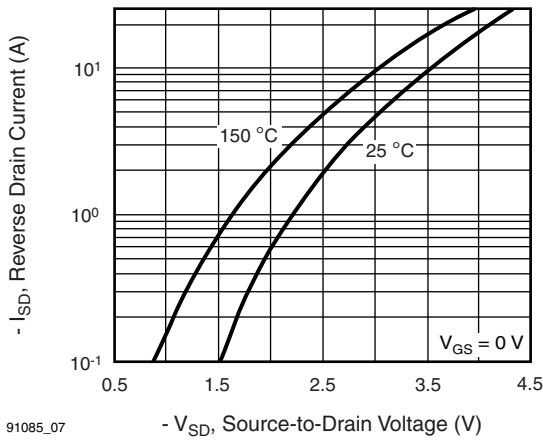
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**Fig. 3 - Typical Transfer Characteristics**



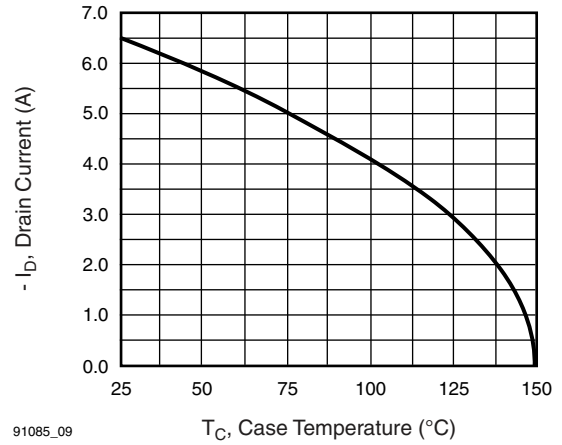
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**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**



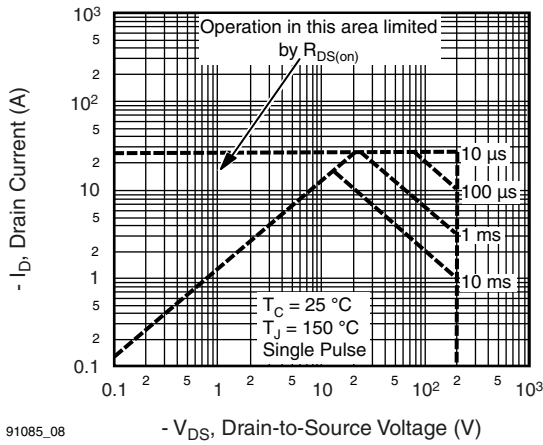
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Fig. 7 - Typical Source-Drain Diode Forward Voltage



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Fig. 9 - Maximum Drain Current vs. Case Temperature



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Fig. 8 - Maximum Safe Operating Area

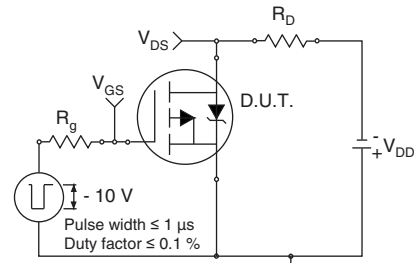


Fig. 10a - Switching Time Test Circuit

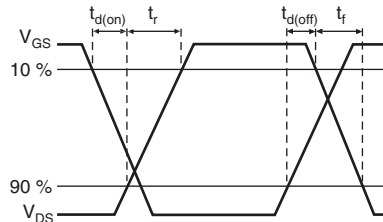
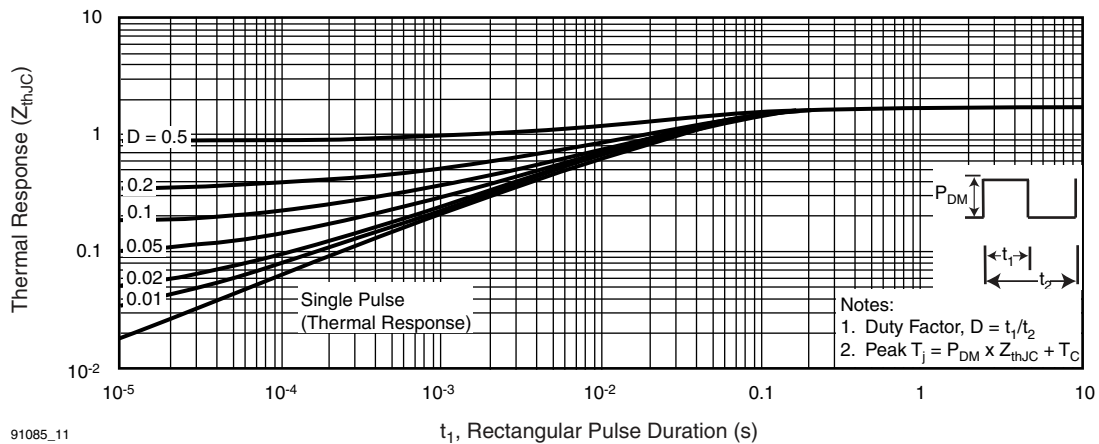


Fig. 10b - Switching Time Waveforms



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Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

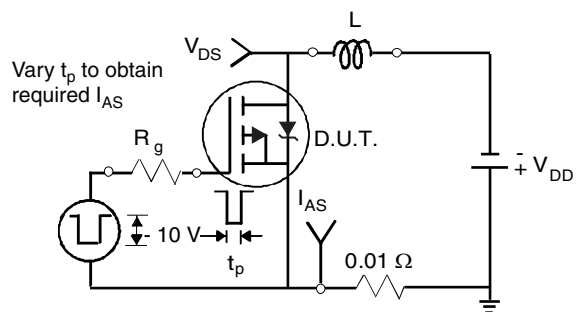


Fig. 12a - Unclamped Inductive Test Circuit

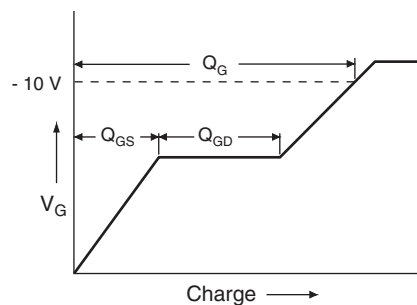


Fig. 13a - Basic Gate Charge Waveform

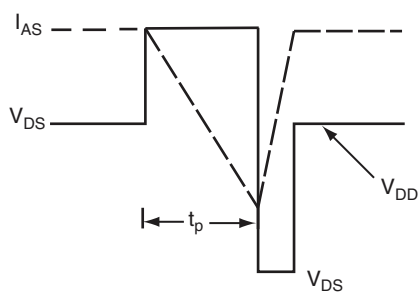


Fig. 12b - Unclamped Inductive Waveforms

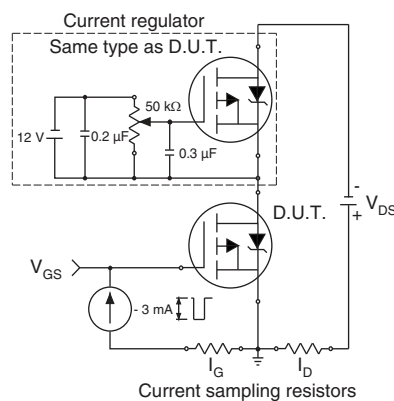


Fig. 13b - Gate Charge Test Circuit

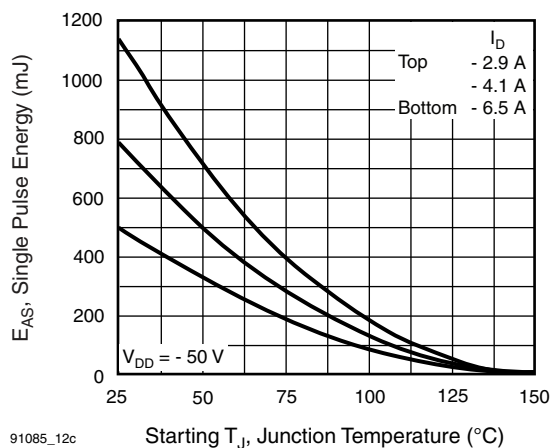
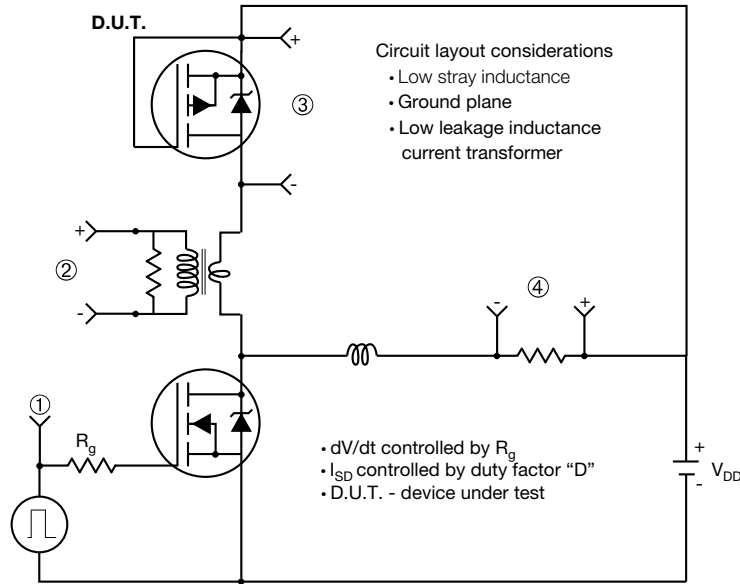
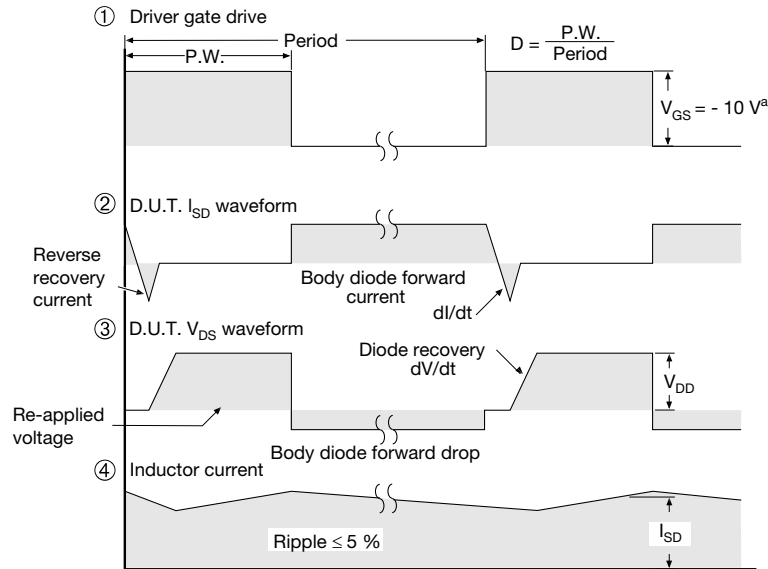


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

**Peak Diode Recovery dV/dt Test Circuit**

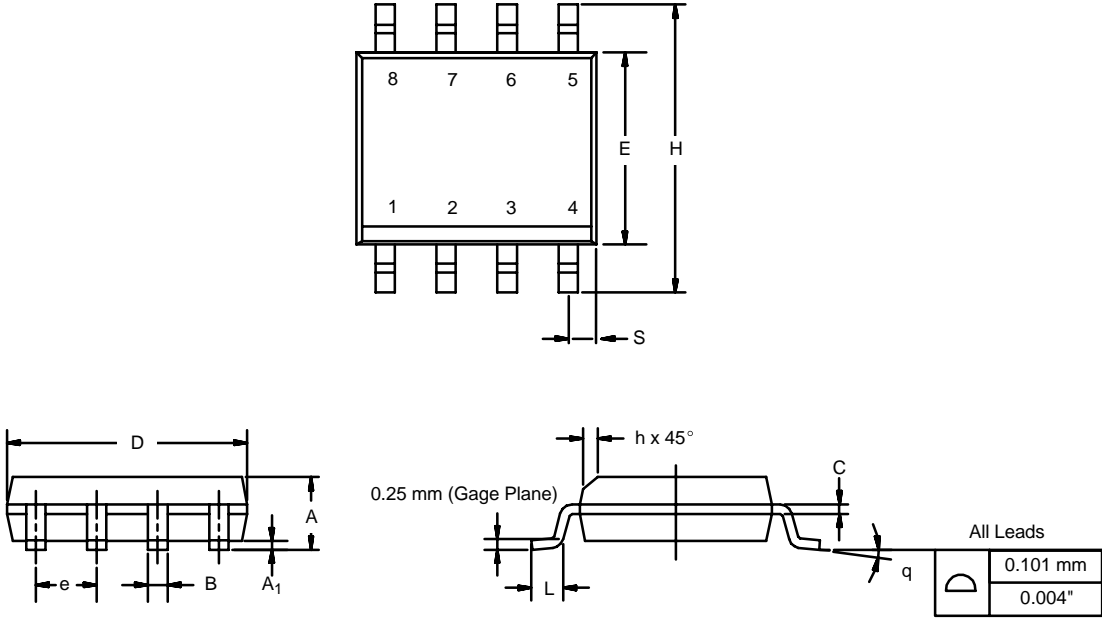


**Note**  
• Compliment N-Channel of D.U.T. for driver



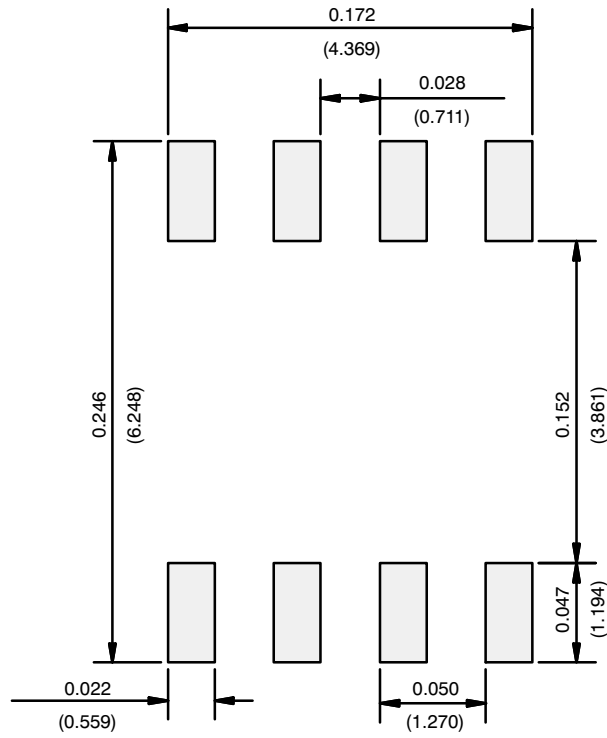
**Fig. 14 - For P-Channel**

**SOIC (NARROW): 8-LEAD**  
JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A <sub>1</sub>	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads  
Dimensions in Inches/(mm)



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