

AON7242-VB Datasheet

N-Channel 40 V (D-S) MOSFET

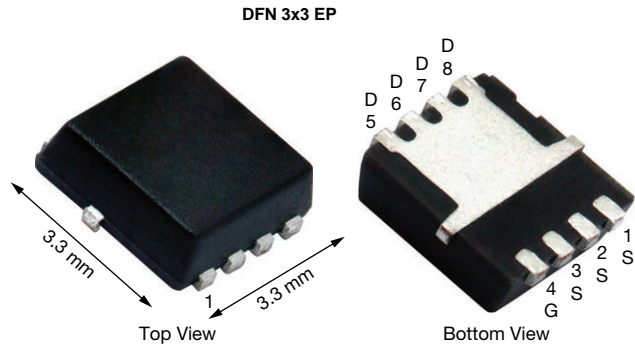
PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) f, g	Q _g (TYP.)
40	0.002 at V _{GS} = 10 V	60	19.5 nC
	0.0024 at V _{GS} = 4.5 V	60	

FEATURES

- TrenchFET® Gen IV power MOSFET
- 100 % R_g and UIS tested
- Tuned for the lowest R_{DS}-Q_{oss} FOM

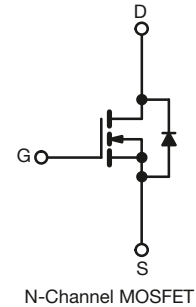


RoHS
COMPLIANT
HALOGEN
FREE



APPLICATIONS

- DC/DC power supplies
- Synchronous rectification
- Motor drive control
- Telecom POL and bricks
- Battery protection



ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)				
PARAMETER	SYMBOL		LIMIT	UNIT
Drain-Source Voltage	V _{DS}		40	V
Gate-Source Voltage	V _{GS}		+20, -16	
Continuous Drain Current (T _J = 150 °C)	T _C = 25 °C	I _D	60 ^g	A
	T _C = 70 °C		60 ^g	
	T _A = 25 °C		24.2 ^{a, b}	
	T _A = 70 °C		19.5 ^{a, b}	
Pulsed Drain Current (t = 100 μs)	I _{DM}		150	
Continuous Source-Drain Diode Current	T _C = 25 °C	I _S	47.2	
	T _A = 25 °C		3.3 ^{a, b}	
Single Pulse Avalanche Current	L = 0.1 mH	I _{AS}	20	
Single Pulse Avalanche Energy		E _{AS}	20	
Maximum Power Dissipation	T _C = 25 °C	P _D	52	W
	T _C = 70 °C		33.3	
	T _A = 25 °C		3.7 ^{a, b}	
	T _A = 70 °C		2.4 ^{a, b}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}		-55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{c, d}			260	

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum Junction-to-Ambient ^{a, e}	t ≤ 10 s	R _{thJA}	24	33	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	1.9	2.4	

Notes

- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- The DFN3x3 package is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 81 °C/W.
- Based on T_C = 25 °C.
- Package limited.

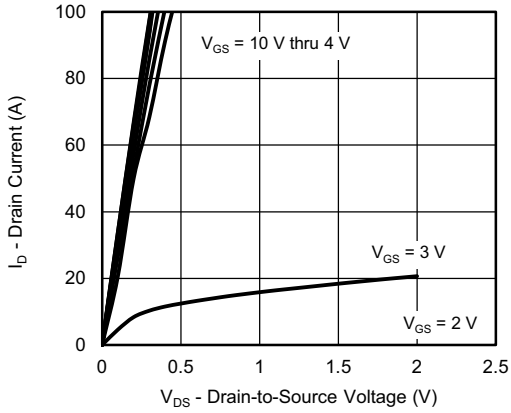
SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	40	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$	-	25	-	mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$		-	-5.3	-	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.1	-	2.4	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = +20\text{ V}, -16\text{ V}$	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	μA
On-State Drain Current ^a		$I_{D(on)}$	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	-	-	
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 10\text{ A}$	-	0.0020	-	Ω
Forward Transconductance ^a		g_{fs}	$V_{DS} = 15\text{ V}, I_D = 10\text{ A}$	-	70	
Dynamic ^b						
Input Capacitance	C_{iss}	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	3240	-	pF
Output Capacitance	C_{oss}		-	455	-	
Reverse Transfer Capacitance	C_{rss}		-	60	-	
C_{rss}/C_{iss} Ratio			-	0.026	0.052	
Total Gate Charge	Q_g	$V_{DS} = 20\text{ V}, V_{GS} = 10\text{ V}, I_D = 10\text{ A}$	-	41.5	63	nC
Gate-Source Charge		Q_{gs}	$V_{DS} = 20\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$	-	8.7	
Gate-Drain Charge	Q_{gd}		-	4.2	-	
Output Charge	Q_{oss}	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$	-	18.5	-	
Gate Resistance	R_g	$f = 1\text{ MHz}$	0.5	1.4	2.5	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 20\text{ V}, R_L = 2\text{ }\Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$	-	10	20	ns
Rise Time	t_r		-	20	40	
Turn-Off Delay Time	$t_{d(off)}$		-	24	48	
Fall Time	t_f		-	7	14	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 20\text{ V}, R_L = 2\text{ }\Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$	-	29	58	
Rise Time	t_r		-	85	170	
Turn-Off Delay Time	$t_{d(off)}$		-	30	60	
Fall Time	t_f		-	35	70	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$	-	-	47.5	A
Pulse Diode Forward Current ($t = 100\text{ }\mu\text{s}$)	I_{SM}		-	-	150	
Body Diode Voltage	V_{SD}	$I_S = 5\text{ A}, V_{GS} = 0\text{ V}$	-	0.74	1.1	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$	-	31	62	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	23	46	nC
Reverse Recovery Fall Time	t_a		-	15	-	ns
Reverse Recovery Rise Time	t_b		-	16	-	

Notes

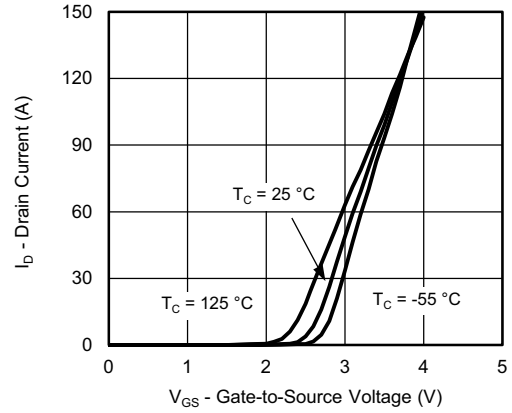
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
 b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

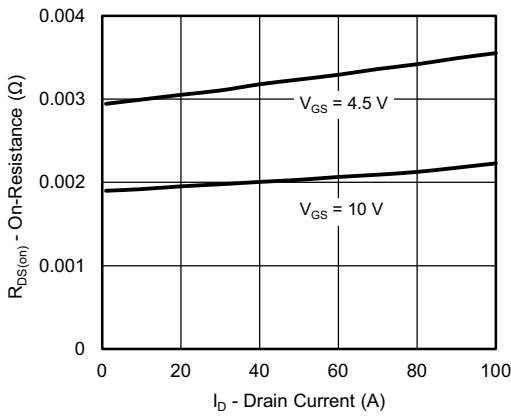
TYPICAL CHARACTERISTICS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)



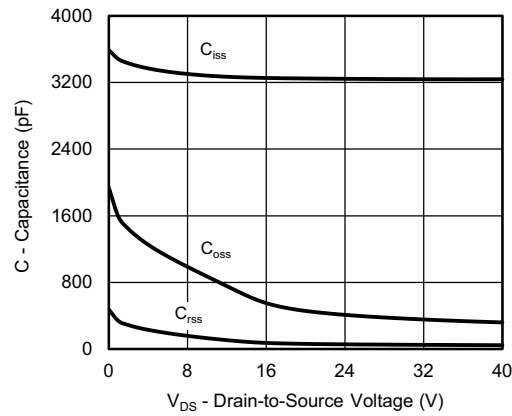
Output Characteristics



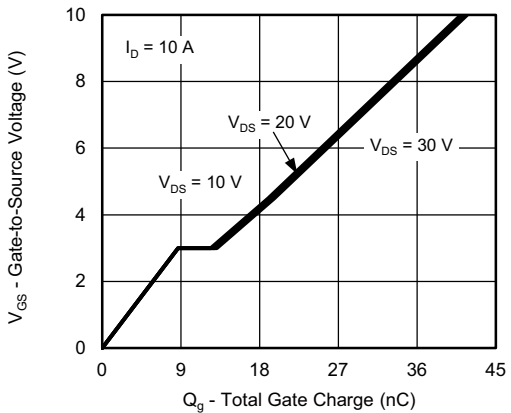
Transfer Characteristics



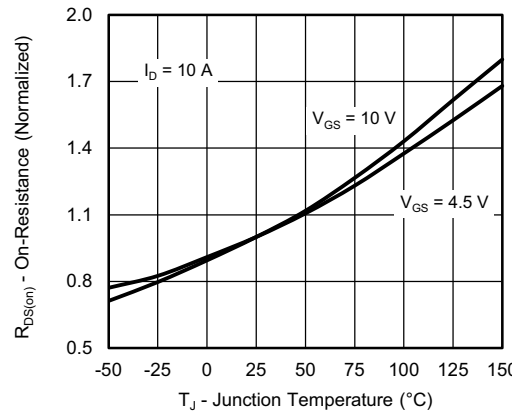
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

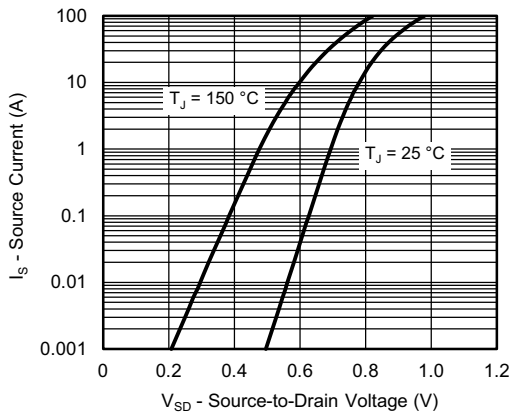


Gate Charge

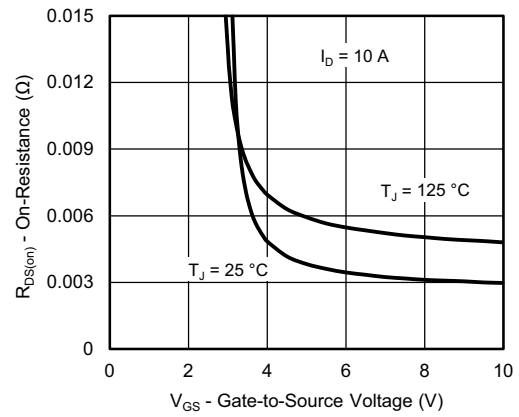


On-Resistance vs. Junction Temperature

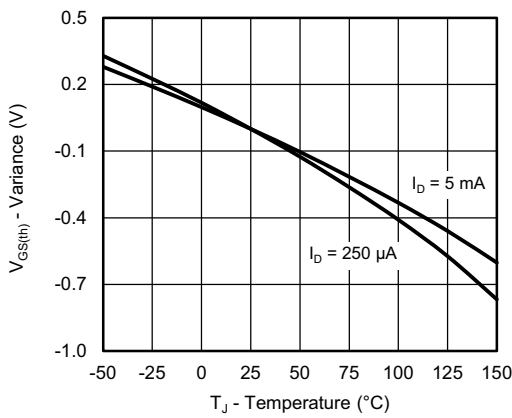
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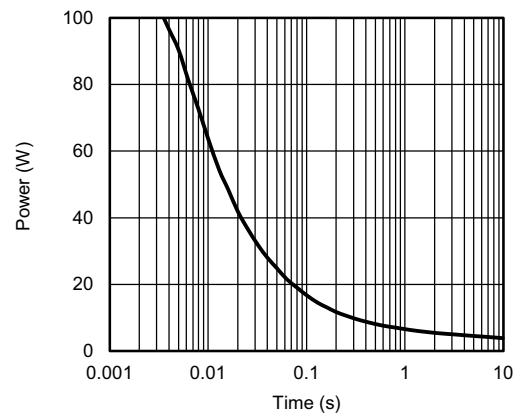
Source-Drain Diode Forward Voltage



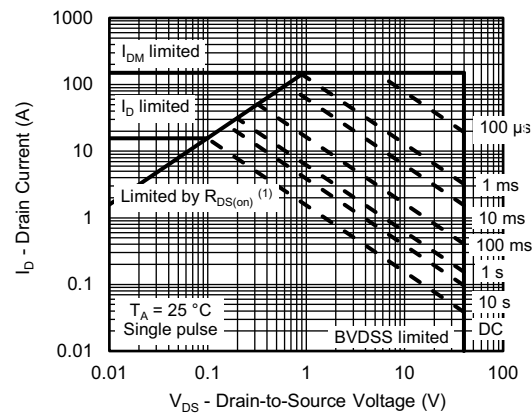
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



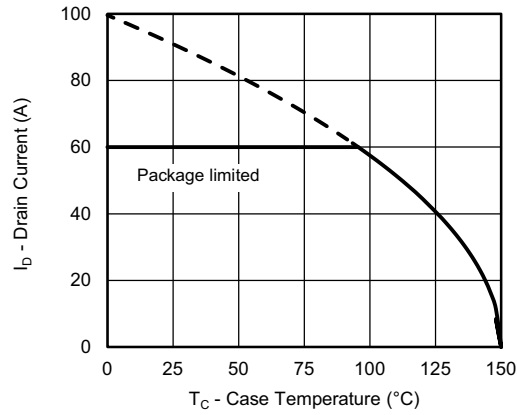
Single Pulse Power, Junction-to-Ambient



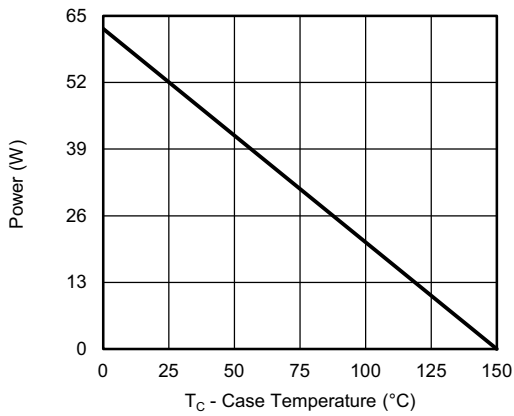
(1) $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

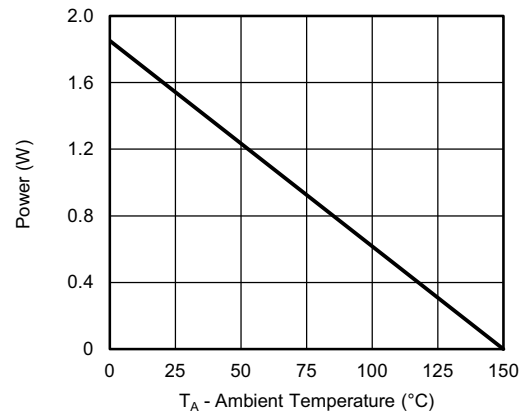
TYPICAL CHARACTERISTICS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Current Derating^a



Power, Junction-to-Case

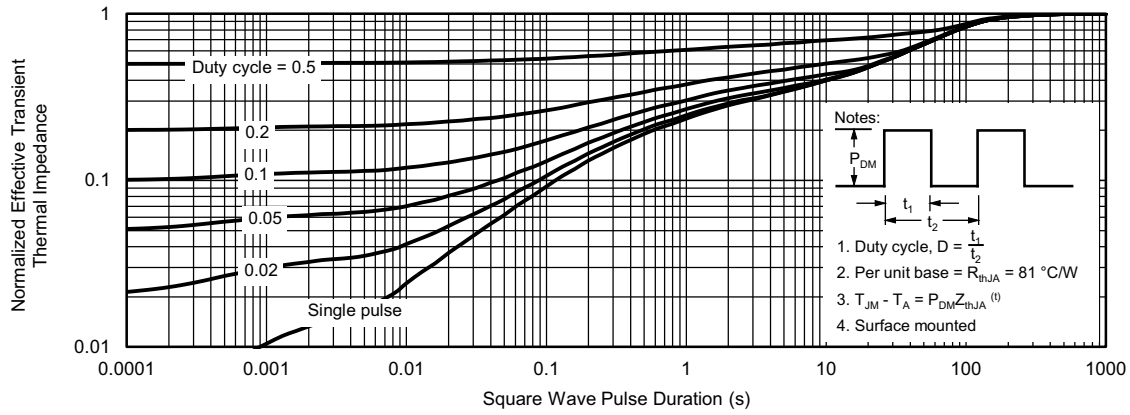


Power, Junction-to-Ambient

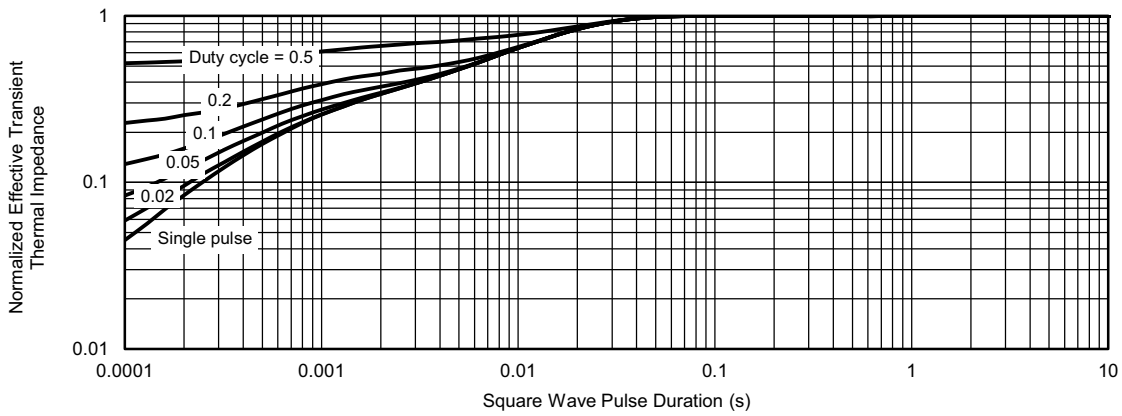
Note

- a. The power dissipation P_D is based on T_J (max.) = 150 $^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)

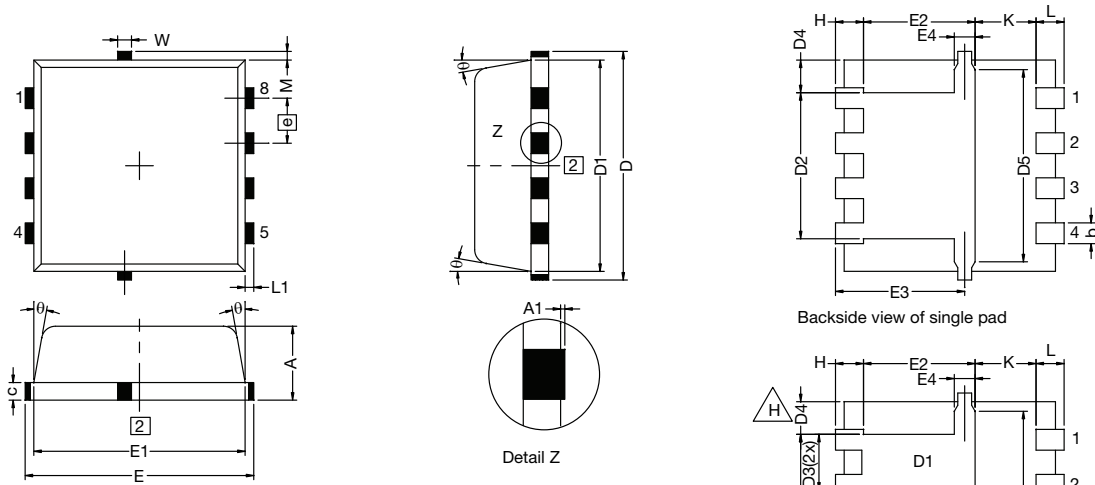


Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

DFN3x3, (Single / Dual)

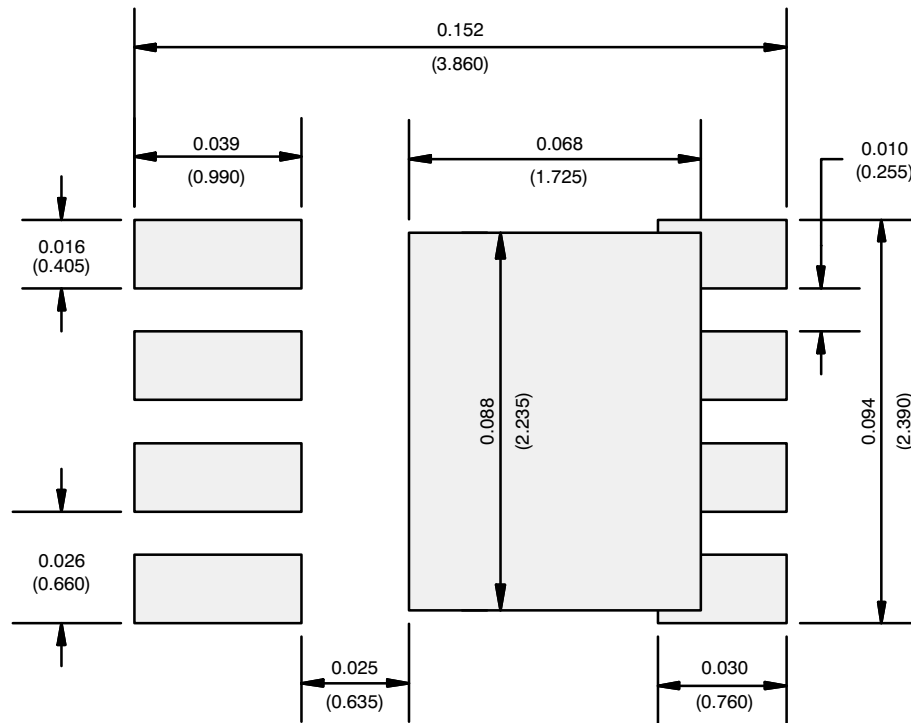


- Notes**
- 1. Inch will govern
 - [2] Dimensions exclusive of mold gate burrs
 - 3. Dimensions exclusive of mold flash and cutting burrs

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.97	1.04	1.12	0.038	0.041	0.044
A1	0.00	-	0.05	0.000	-	0.002
b	0.23	0.30	0.41	0.009	0.012	0.016
c	0.23	0.28	0.33	0.009	0.011	0.013
D	3.20	3.30	3.40	0.126	0.130	0.134
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
D3	0.48	-	0.89	0.019	-	0.035
D4	0.47 typ.			0.0185 typ		
D5	2.3 typ.			0.090 typ		
E	3.20	3.30	3.40	0.126	0.130	0.134
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
E3	1.75	1.85	1.98	0.069	0.073	0.078
E4	0.034 typ.			0.013 typ.		
e	0.65 BSC			0.026 BSC		
K	0.86 typ.			0.034 typ.		
K1	0.35	-	-	0.014	-	-
H	0.30	0.41	0.51	0.012	0.016	0.020
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
θ	0°	-	12°	0°	-	12°
W	0.15	0.25	0.36	0.006	0.010	0.014
M	0.125 typ.			0.005 typ.		

ECN: S16-2667-Rev. M, 09-Jan-17
DWG: 5882

RECOMMENDED MINIMUM PADS FOR DFN 3x3



Recommended Minimum Pads
Dimensions in Inches/(mm)

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