

AON6926-VB Datasheet Dual N-Channel 30V (D-S) MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	$R_{DS(on)}(\Omega)$	I _D (A)	Q _g (Typ.)		
30	0.0034 at V _{GS} = 10 V	60	17 nC		
	0.0043 at V _{GS} = 4.5 V	55	17 110		

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFET
- 100 % UIS Tested
- 100 % R_g Tested
- Compliant to RoHS Directive 2002/95/EC

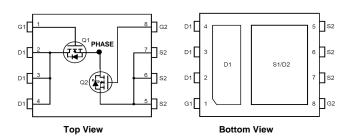


ROHS COMPLIANT HALOGEN FREE

APPLICATIONS

- Set Top Box
- Low Current DC/DC





Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V _{DS}	30	V	
Gate-Source Voltage		V_{GS}	± 20	V	
	T _C = 25 °C		60 ^a		
Continuous Drain Current (T _{.1} = 150 °C)	T _C = 70 °C	I _D	50		
Continuous Brain Gunerit (1) = 100 O)	T _A = 25 °C		25.2 ^{b, c}		
	T _A = 70 °C		22.2 ^{b, c}	Α Α	
Pulsed Drain Current		I _{DM}	200		
Continuous Source-Drain Diode Current	T _C = 25 °C	I.	2.25		
Continuous Source-Drain Diode Current	T _A = 25 °C	- I _S	1.48 ^{b, c}		
Single Pulse Avalanche Current	L = 0.1 mH	I _{AS}	5		
Single Pulse Avalanche Energy		E _{AS}	1.25	mJ	
Maximum Power Dissipation	T _C = 25 °C		56		
	T _C = 70 °C	P _D	15	w	
	T _A = 25 °C		2.18 ^{b, c}	VV	
	T _A = 70 °C	1	1.34 ^{b, c}		
Operating Junction and Storage Temperature Range		T _J , T _{stq}	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS						
Parameter		Symbol Typical		Maximum	Unit	
Maximum Junction-to-Ambient ^{a, c, d}	t ≤ 10 s	R _{thJA}	58	70	°C/W	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	38	45] 0, , ,	

Notes:

- a. Package limited, T_C = 25 °C.
- b. Surface Mounted on 1" x 1" FR4 board.
- c. t = 10 s
- d. Maximum under Steady State conditions is 110 °C/W.



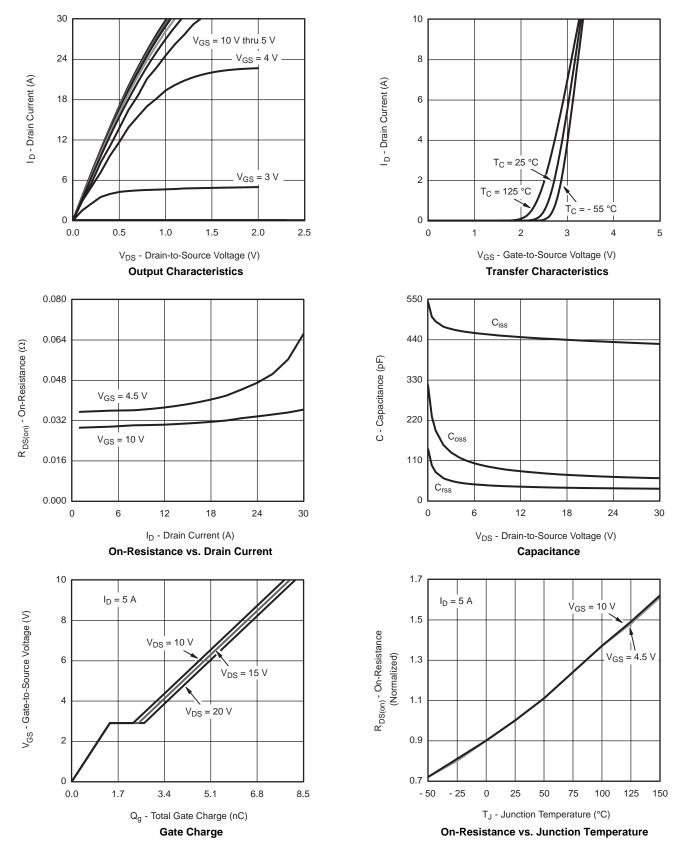
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static			•			
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	30			V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I _D = 250 μA		32		mV/°C
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I _D = 250 μA		- 5.0		
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$	1.0		2.5	V
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current		$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}$			1	μA
	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V, T _J = 55 °C			10	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	10			Α
		V _{GS} = 10 V, I _D = 5 A		0.0034		Ω
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 4 \text{ A}$		0.0043		
Forward Transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 5 A		16		S
Dynamic ^b	<u> </u>		I			l .
Input Capacitance	C _{iss}			1300		
Output Capacitance	C _{oss}	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		257		pF
Reverse Transfer Capacitance	C _{rss}			155		
Total Gate Charge	Q _g	$V_{DS} = 15 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 5 \text{ A}$		17		nC
		50 00 5		3.7	5.6	
Gate-Source Charge	Q _{gs}	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 5 \text{ A}$		1.4		
Gate-Drain Charge	Q _{gd}			1.05		
Gate Resistance	R _g	f = 1 MHz	0.8	4.3	8.6	Ω
Turn-On Delay Time	t _{d(on)}			12	24	
Rise Time	t _r	V_{DD} = 15 V, R_L = 3 Ω		55	100	ns
Turn-Off Delay Time	t _{d(off)}	$I_D\cong 5$ A, V_{GEN} = 4.5 V, R_g = 1 Ω		11	22	
Fall Time	t _f			8	16	
Turn-On Delay Time	t _{d(on)}			4	8	
Rise Time	t _r	V_{DD} = 15 V, R_L = 3 Ω		9	18	
Turn-Off Delay Time	t _{d(off)}	$I_D\cong 5$ A, V_{GEN} = 10 V, R_g = 1 Ω		10	20	
Fall Time	t _f			6	12	
Drain-Source Body Diode Characteristi	cs		•			
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			2.25	Δ
Pulse Diode Forward Current	I _{SM}				24	A
Body Diode Voltage	V_{SD}	I _S = 2 A, V _{GS} = 0 V		0.8	1.2	V
Body Diode Reverse Recovery Time	t _{rr}			11	20	ns
Body Diode Reverse Recovery Charge	Q _{rr}	I _F = 5 A, dI/dt = 100 A/μs, T _J = 25 °C		4	8	nC
Reverse Recovery Fall Time	ta	$_{1F} = 3 \text{ A}$, $_{1J} = 25 \text{ C}$		7		20
Reverse Recovery Rise Time	t _b			4		ns

Notes:

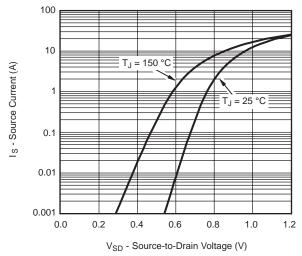
- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%$
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

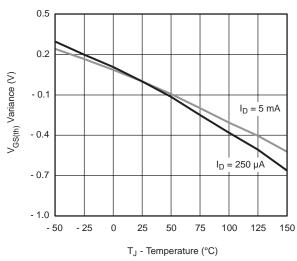




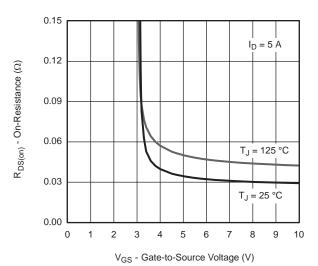




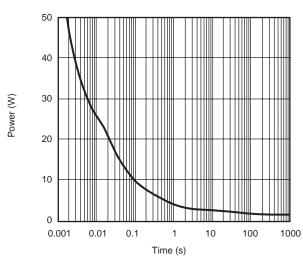
Source-Drain Diode Forward Voltage



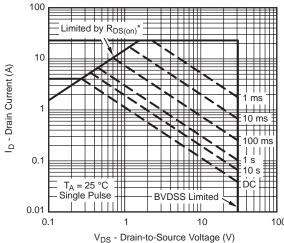
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage



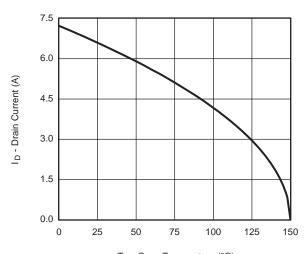
Single Pulse Power



* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

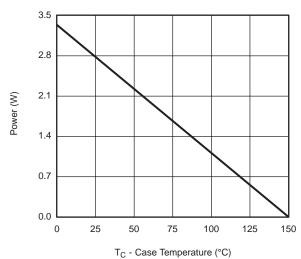
Safe Operating Area, Junction-to-Ambient

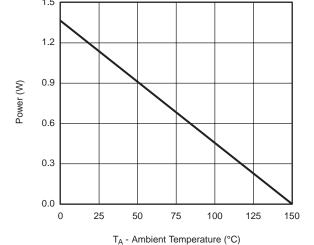




T_C - Case Temperature (°C)

Current Derating*





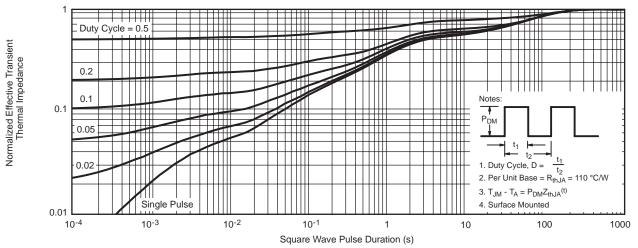
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Power, Junction-to-Foot

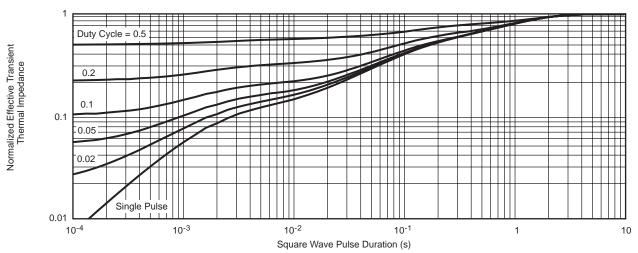
Power, Junction-to-Ambient

^{*} The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



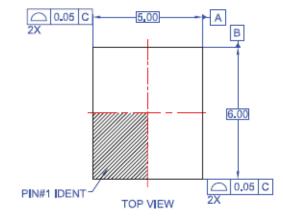


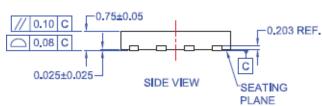
Normalized Thermal Transient Impedance, Junction-to-Ambient

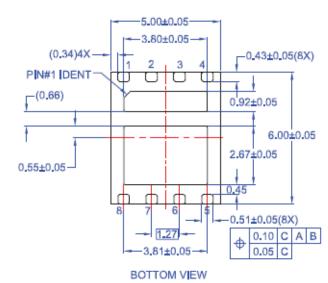


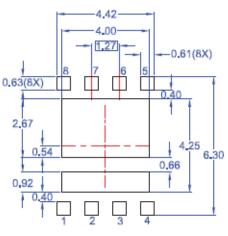
Normalized Thermal Transient Impedance, Junction-to-Foot











RECOMMENDED LAND PATTERN

NOTE:

- PACKAGE DOES NOT FULLY CONFORM TO JEDEC STANDARD.
- B. DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS AND TOLERANCES PER ASME Y14.5M,
- LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
- E. DRAWING FILENAME: MKT-MLP08Krev3.



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