Triple 2-3-2-Input OR/NOR Gate

MC10105

The MC10105 is a triple 2–3–2 input OR/NOR gate.

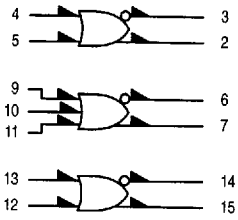
P_D = 30 mW typ/gate (No Load)
t_{pd} = 2.0 ns typ
t_r, t_f = 2.0 ns typ (20%–80%)

L SUFFIX
CERAMIC PACKAGE
CASE 620–10

P SUFFIX
PLASTIC PACKAGE
CASE 648–08

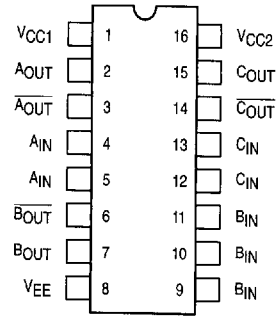
FN SUFFIX
PLCC
CASE 775–02

LOGIC DIAGRAM



V_{CC1} = PIN 1
V_{CC2} = PIN 16
V_{EE} = PIN 8

DIP
PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 6–11.

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ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			−30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		23		17	21		23	mAdc
Input Current	I_{inH}	4		425			265		265	µAdc
	I_{inL}	4	0.5		0.5			0.3		µAdc
Output Voltage Logic 1	V_{OH}	3	−1.060	−0.890	−0.960		−0.810	−0.890	−0.700	Vdc
		2	−1.060	−0.890	−0.960		−0.810	−0.890	−0.700	
Output Voltage Logic 0	V_{OL}	3	−1.890	−1.675	−1.850		−1.650	−1.825	−1.615	Vdc
		2	−1.890	−1.675	−1.850		−1.650	−1.825	−1.615	
Threshold Voltage Logic 1	V_{OHA}	3	−1.080		−0.980			−0.910		Vdc
		2	−1.080		−0.980			−0.910		
Threshold Voltage Logic 0	V_{OLA}	3		−1.655			−1.630		−1.595	Vdc
		2		−1.655			−1.630		−1.595	
Switching Times (50Ω Load)										ns
Propagation Delay	t_{4+3-}	3	1.0	3.1	1.0	2.0	2.9	1.0	3.3	
	t_{4-3+}	3	1.0	3.1	1.0	2.0	2.9	1.0	3.3	
	t_{4+2+}	2	1.0	3.1	1.0	2.0	2.9	1.0	3.3	
	t_{4-2-}	2	1.0	3.1	1.0	2.0	2.9	1.0	3.3	
Rise Time (20 to 80%)	t_{3+}	3	1.1	3.6	1.1	2.0	3.3	1.1	3.7	
	t_{2+}	2	1.1	3.6	1.1	2.0	3.3	1.1	3.7	
Fall Time (20 to 80%)	t_{3-}	3	1.1	3.6	1.1	2.0	3.3	1.1	3.7	
	t_{2-}	2	1.1	3.6	1.1	2.0	3.3	1.1	3.7	

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ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

Characteristic		Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current		I_E	8					8	1, 16
Input Current		I_{inH}	4	4				8	1, 16
		I_{inL}	4		4			8	1, 16
Output Voltage	Logic 1	V_{OH}	3					8	1, 16
			2	4				8	1, 16
Output Voltage	Logic 0	V_{OL}	3	4				8	1, 16
			2					8	1, 16
Threshold Voltage	Logic 1	V_{OHA}	3				4	8	1, 16
			2			4		8	1, 16
Threshold Voltage	Logic 0	V_{OLA}	3			4		8	1, 16
			2				4	8	1, 16
Switching Times	(50Ω Load)					**Pulse In**	**Pulse Out**	**−3.2 V**	**+2.0 V**
Propagation Delay		t_{4+3-}	3			4	3	8	1, 16
		t_{4-3+}	3			4	3	8	1, 16
		t_{4+2+}	2			4	2	8	1, 16
		t_{4-2-}	2			4	2	8	1, 16
Rise Time	(20 to 80%)	t_{3+}	3			4	3	8	1, 16
		t_{2+}	2			4	2	8	1, 16
Fall Time	(20 to 80%)	t_{3-}	3			4	3	8	1, 16
		t_{2-}	2			4	2	8	1, 16

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

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