

2.75V-42V, Low I_Q, LDO Linear Regulator

1 FEATURES

- Automotive AEC-Q100 Grade 1 Qualified
- Ultra-Low I_Q 7.5μA
- Wide Input Voltage Range: 2.75V to 42V
- ±2% FB Tolerance for Adjustable Output
- Up to 200mA Output Current
- Shutdown Current 1μA
- PG Indicator with Adjustable Delay Time for MCU Applications
- High PSRR 70dB @ 100Hz
- Stable Operation with only 1μF Low-ESR Ceramic Output Capacitor
- Low Dropout: 260mV @ 200mA
- Up to 42V High Voltage EN Pin with Logic Threshold
- Over-Current Protection
- Over Temperature Shutdown and Auto Restart
- Internal Soft Start
- -40°C to 150 °C Junction Temperature
- Product Package:
DFN-EP8 Package with Wettable Flanks
DFN-EP8 Package without Wettable Flank

2 APPLICATIONS

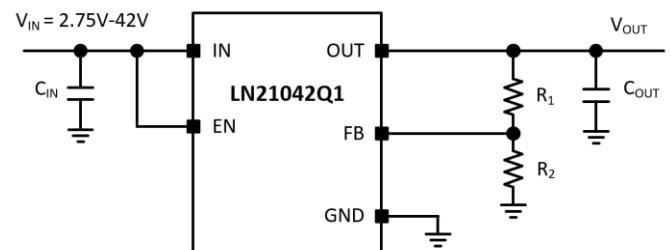
- Automotive Power Supplies
- Industrial Power Supplies
- Battery Powered Systems

3 DESCRIPTION

LN21042Q1 is an ultra-low quiescent current, low dropout linear regulator (LDO) with a wide input voltage range of 2.75V to 42V. The series provides 0.6V to 24V adjustable output and delivers up to 200mA output current. Typical shutdown current of LN21042Q1 is less than 1μA, while the quiescent current under no-load condition is 7.5μA.

LN21042Q1 provides a power good indicator with programmable delay to directly drive the reset pin of a microprocessor (MCU).

LN21042Q1 features over-current protection and over-temperature shutdown with auto restart. The product family is available in DFN-EP8 package with wettable flanks and without wettable flank.



Typical MCU Application Diagram

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4 VERSION HISTORY

Version	Change Record	Time
0.1	Initial Draft	2023/4/20
0.2	Add New Part Number, Typical Characteristic Curves, Waveforms and POD	2023/10/11
0.3	Fix error in block diagram; Fix writing/editing errors.	2023/12/20

Note: For the product datasheet with version number 0.X, the corresponding product is an unreleased product. LEN Technology Ltd. reserves the right to make any changes to the product and the documents and services related to the product and does not need to notify the recipient of this document.

5 ORDER INFORMATION

Part Number	V _{OUT}	Max Load	I _Q	IC Package	MSL-Peak-Temp ⁽¹⁾	Material	Package Qty	Top Marking ⁽²⁾
LN210421Q1CFR	Adjustable	200mA	7.5uA	DFN-EP8 with wettable flanks	Level-2-260C	RoHS	Tape & Reel 3000	0421
LN210421Q1NFR	Adjustable	200mA	7.5uA	DFN-EP8 without wettable flank	Level-2-260C	RoHS	Tape & Reel 3000	0421N

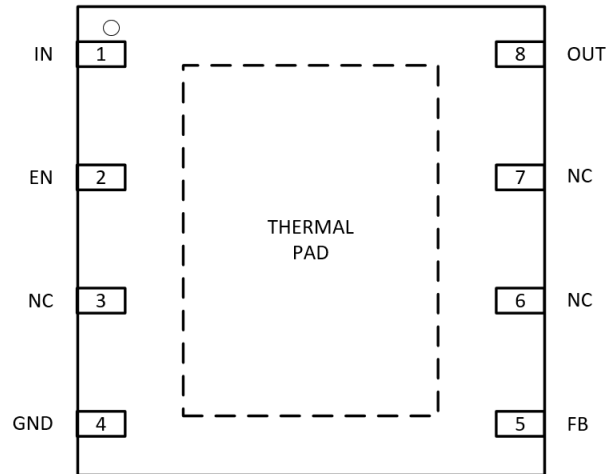
(1) MSL (Moisture Sensitivity Level) is based on JEDEC industrial classification, and the tabled temperature is the maximum solder temperature;

(2) There may be additional marking related to the internal trace code on the device.

6 PIN CONFIGURATION AND FUNCTION

6.1 Pin Configuration

DFN-EP8 (3mm X 3mm) Top View



6.2 Pin Function

Name	Number	Description
IN	1	Input pin, place a ceramic capacitor of at least 1 μ F between IN and GND.
EN	2	Enable pin, connect to a logic control signal or to IN directly.
NC	3	No internal connection. Recommend connecting to GND.
GND	4	Connect to GND.
FB	5	Feedback pin, connect through a resistor divider to the output for operation.
NC	6	No internal connection. Recommend connecting to GND.
NC	7	No internal connection. Recommend connecting to GND.
OUT	8	Output pin, place a ceramic capacitor of at 1 μ F between OUT and GND.
Thermal Pad	-	Connect the pad to GND for best thermal performance.

7 SPECIFICATIONS

7.1 Absolute Maximum Ratings

Parameters	Min	Max	Unit
V_{IN}	-0.3	45	V
V_{EN}	-0.3	V_{IN}	
V_{FB}	-0.3	5.5	
V_{OUT}	-0.3	V_{IN}	
Operating Junction Temperature	-40	150	°C
Operating Ambient Temperature	-40	125	
Storage Temperature	-55	150	

7.2 ESD Ratings

Parameters	Min	Max	Unit
HBM Human Body Model		±2000	V
CDM Charge Device Model		±750	

7.3 Recommended Operating Condition

Parameters	Min	Max	Unit
V_{IN}	2.75	42	V
V_{EN}	0	V_{IN}	
V_{FB}	0	0.7	
V_{OUT}	0.6	24	
Operating Junction Temperature	-40	150	°C

7.4 Package Thermal Parameters

Parameter ⁽¹⁾		DFN-EP8	Units
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance	53	°C/W
ψ_{JT}	Junction-to-Top Characterization Parameter	3	°C/W

(1) Measurements are based on standard 2s2p PCB defined in JESD 51-7 2s2p, under no wind, 2W loss, and 25°C ambient temperature.

7.5 Electrical Characteristics

Unless otherwise stated, the minimum and maximum limits apply over the recommended operating junction temperature range of -40°C to 150°C. Typical values are measured at 25°C and represent the most likely norm. The default conditions apply: $V_{IN} = 13.5V$.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VIN, VOUT (IN, OUT, GND PINS)						
VIN	Operating Input Voltage Range		2.75		42	V
VOUT	Operating Output Voltage Range for Adjustable Output		0.6		24	V
ISHDN	Input Shutdown Current	VEN = 0V, VIN = 13.5V		0.8	3	μA
IQ	Input Quiescent Current	VEN = 5V, VIN = 13.5V, IOUT = 0A		7.5	17	μA
REGULATION, (OUT, FB PINS)						
VFB	Regulated Feedback Voltage	VFB = VOUT, 4.3V<VIN<28V, 1mA<IOUT<IOUTMAX	0.588	0.6	0.612	V
		VFB = VOUT, 28V<VIN<42V, 1mA<IOUT<75%×IOUTMAX				
IFB	Feedback Input Leakage Current	VFB = 0.6V	-0.1	0	0.1	μA
VOUT%	Regulated Output Voltage Error for Fixed VOUT Parts	VOUT + 1V<VIN<28V, 1mA< IOUT < IOUTMAX	-2		2	%
		28V< VIN <42V, 1mA< IOUT <75%×IOUTMAX				
	Line Regulation	VOUT + 1V< VIN <42V, 1mA< IOUT <75%×IOUTMAX		±0.1		%
	Load Regulation	VOUT + 1V< VIN <42V, 1mA< IOUT <75%×IOUTMAX		±0.5		%
DROPOUT						
VDO-200mA-5V	Dropout Voltage	IOUT = 200mA, VIN = 0.9×VOUT, VOUT ≥ 5V		260		mV
VDO-200mA-3.3V	Dropout Voltage	IOUT = 200mA, VIN = 0.9×VOUT, VOUT = 3.3V		400		mV

Electrical Characteristics (Continued)

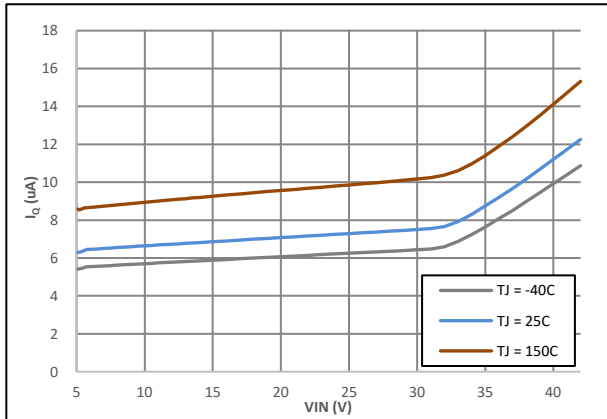
OVER CURRENT PROTECTION					
I_{LIMIT}	Current Limit Threshold	$V_{OUT} = 90\% \times V_{OUT-NOM},$ $V_{IN} = 13.5V$	200	280	500
					mA
POWER SUPPLY REJECTION RATIO (PSRR)					
$G_{PSRR-100Hz}$	PSRR@100Hz	$I_{OUT} = 50mA, V_{OUT} = 5 V$ or 3.3V		70 ⁽¹⁾	
					dB
ENABLE (EN PIN)					
V_{EN-H}	Enable high-level voltage		2		V
V_{EN-L}	Enable Low-level voltage			0.4	V
I_{EN}	EN Leakage Current	$V_{EN} = 5V$	0.5	2	μA
THERMAL SHUTDOWN					
T_{SD}	Thermal Shutdown Threshold		151	170 ⁽¹⁾	°C
T_{SD-HYS}	Thermal Shutdown Recovery Hysteresis			13 ⁽¹⁾	°C

(1) Value specified by design, not subject to production test.

7.6 Typical Characteristics

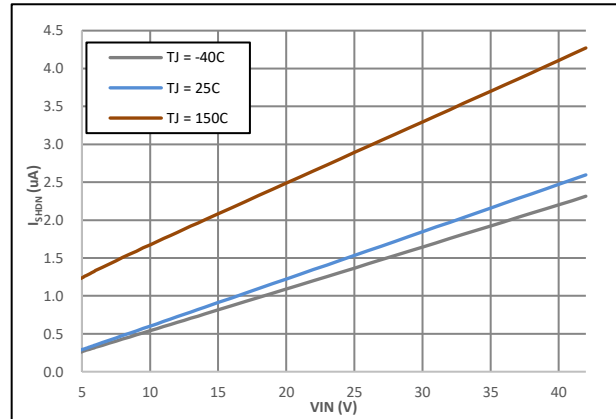
7.6.1 Characteristics Over Temperature

Unless otherwise stated, the test conditions are the same as Chapter 7.5. $T_J = -40^{\circ}\text{C}$ to 150°C .



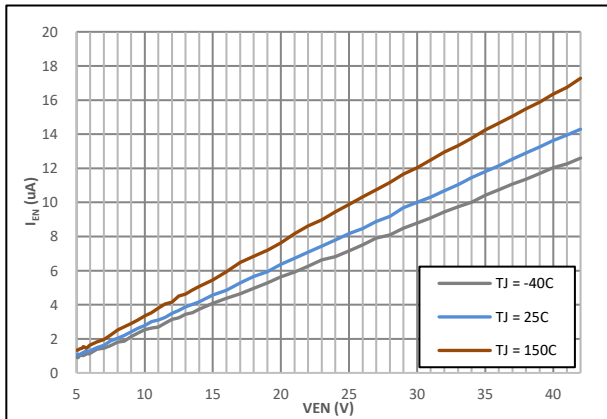
LN210421Q1, Adjustable $V_{OUT} = 5\text{V}$, No load

Figure 1. I_Q



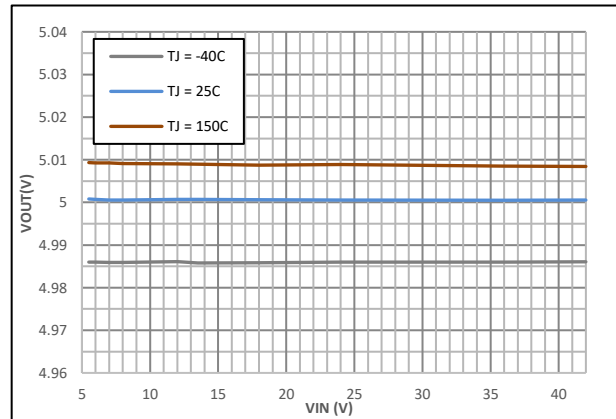
LN210421Q1, Adjustable $V_{OUT} = 5\text{V}$, No load

Figure 2. I_{SHDN}



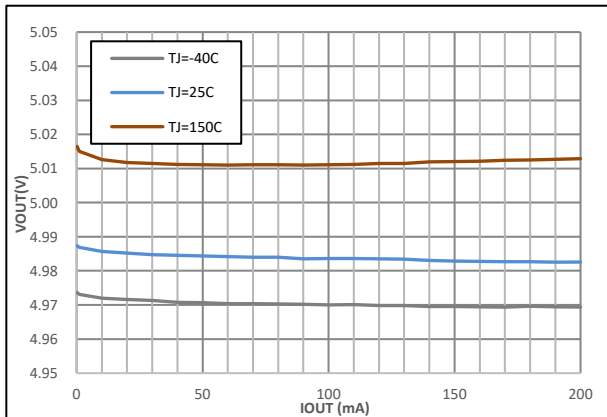
LN210421Q1, Adjustable $V_{OUT} = 5\text{V}$, No load

Figure 3. I_{EN}



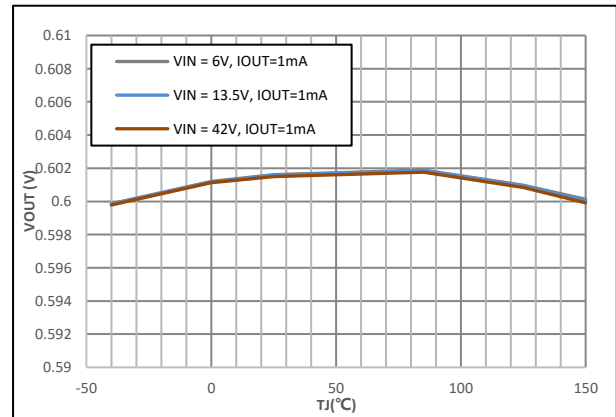
LN210421Q1, Adjustable $V_{OUT} = 5\text{V}$, $I_{OUT} = 1\text{mA}$

Figure 4. Line Regulation



LN210421Q1, Adjustable $V_{OUT} = 5\text{V}$, $V_{IN} = 6\text{V}$

Figure 5. Load Regulation

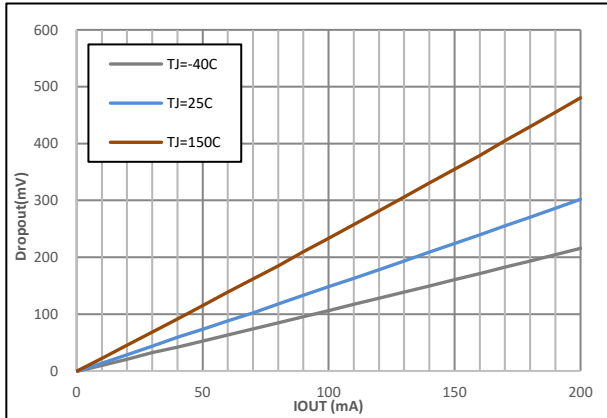


LN210421Q1, Adjustable $V_{OUT} = 0.6\text{V}$, $I_{OUT} = 1\text{mA}$

Figure 6. V_{OUT} vs. Temperature

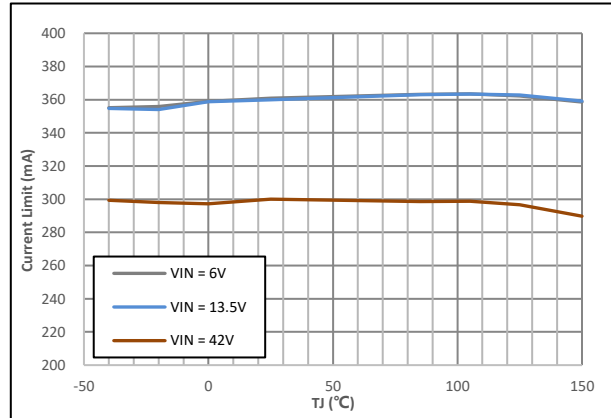
Characteristics Over Temperature (Continued)

Unless otherwise stated, the test conditions are the same as Chapter 7.5. $T_J = -40^{\circ}\text{C}$ to 150°C .



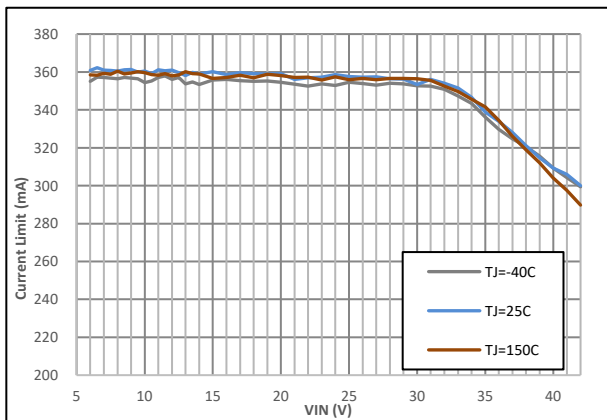
LN210421Q1, Adjustable $V_{OUT} = 5\text{V}$

Figure 7. Dropout



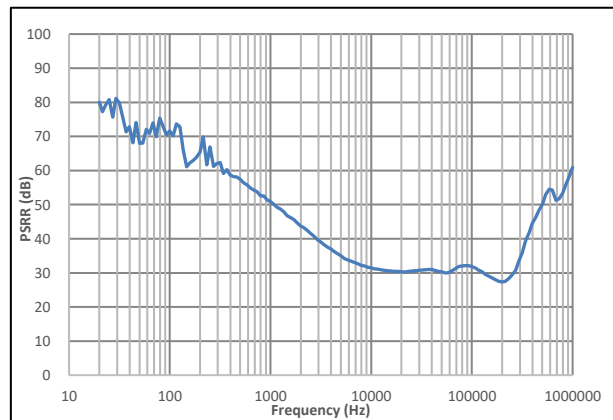
LN210421Q1, Adjustable $V_{OUT} = 5\text{V}$

Figure 8. Current Limit vs. Temperature



LN210421Q1, Adjustable $V_{OUT} = 5\text{V}$

Figure 9. Current Limit vs. VIN

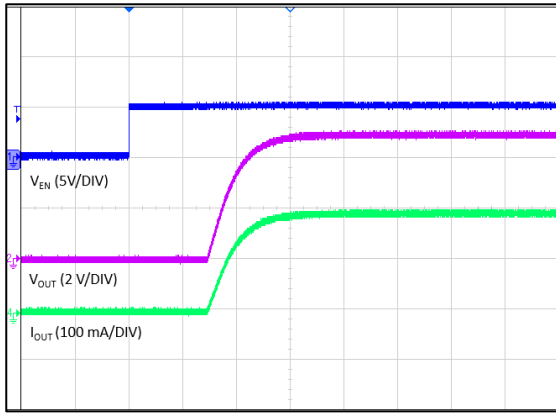


LN210421Q1, Adjustable $V_{OUT} = 5\text{V}$, $C_{IN} = 100\text{pF}$, $V_{IN} = 6\text{V}$, $I_{OUT} = 10\text{mA}$

Figure 10. PSRR

7.6.2 Typical Characteristics

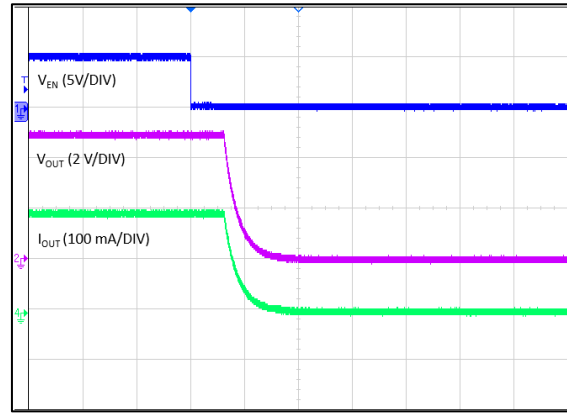
Unless otherwise stated, the test conditions are the same as Chapter 7.5. $T_J = -40^{\circ}\text{C}$ to 150°C .



Time (100 μs /DIV)

LN210421Q1, Adjustable $V_{\text{OUT}} = 5\text{V}$, $V_{\text{IN}} = 13.5\text{V}$, $R_{\text{LOAD}} = 25\Omega$

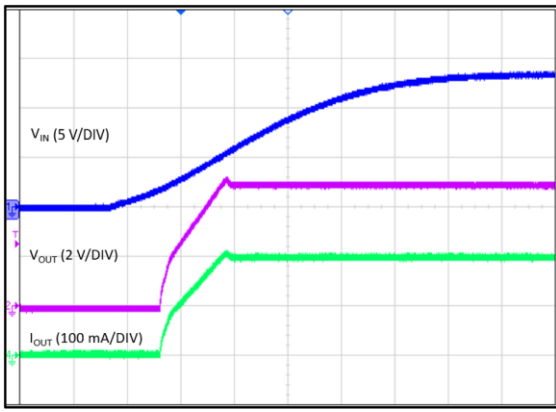
Figure 13. Startup with EN



Time (100 μs /DIV)

LN210421Q1, Adjustable $V_{\text{OUT}} = 5\text{V}$, $V_{\text{IN}} = 13.5\text{V}$, $R_{\text{LOAD}} = 25\Omega$

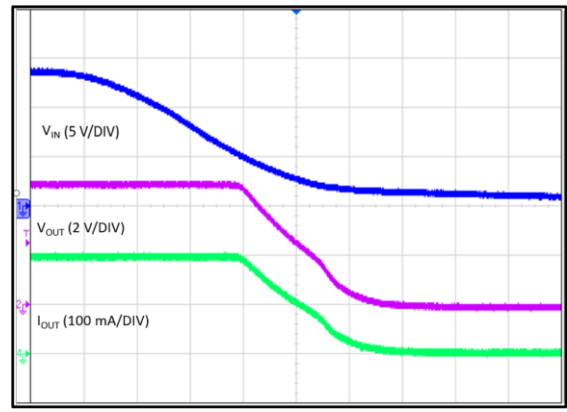
Figure 14. Shutdown with EN



Time (2ms/DIV)

LN210421Q1, Adjustable $V_{\text{OUT}} = 5\text{V}$, $V_{\text{IN}} = 13.5\text{V}$, $R_{\text{LOAD}} = 25\Omega$

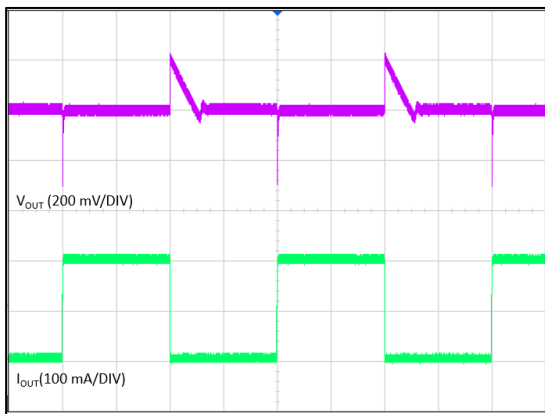
Figure 15. Startup with V_{IN}



Time (2ms/DIV)

LN210421Q1, Adjustable $V_{\text{OUT}} = 5\text{V}$, $V_{\text{IN}} = 13.5\text{V}$, $R_{\text{LOAD}} = 25\Omega$

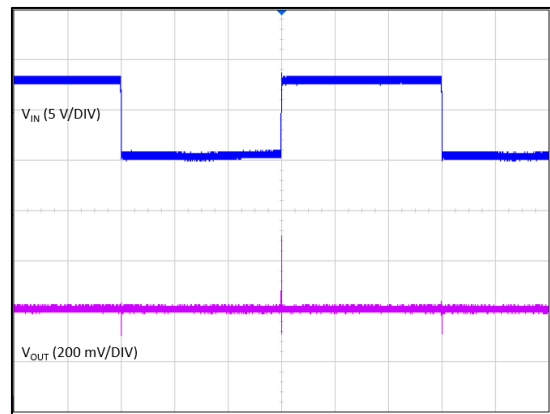
Figure 16. Shutdown with V_{IN}



Time (5ms/DIV)

LN210421Q1, Adjustable $V_{\text{OUT}} = 5\text{V}$, $V_{\text{IN}} = 13.5\text{V}$, Slew Rate $\downarrow = 0.1\text{A}/\mu\text{s}$

Figure 17. Load Transient 0 <-> 200mA



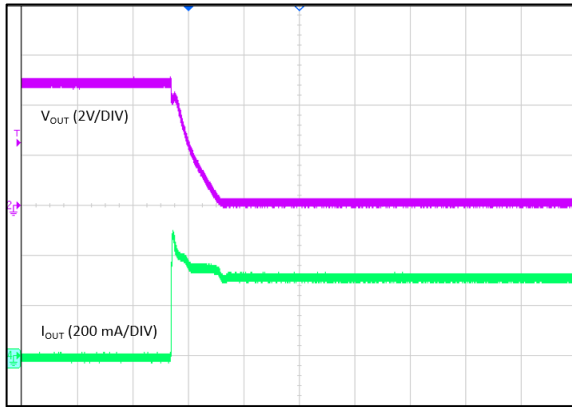
Time (1ms/DIV)

LN210421Q1, Adjustable $V_{\text{OUT}} = 5\text{V}$, $I_{\text{OUT}} = 200\text{mA}$, Slew Rate $\uparrow = 5\text{V}/\mu\text{s}$

Figure 18. Line Transient 6 <-> 13.5V

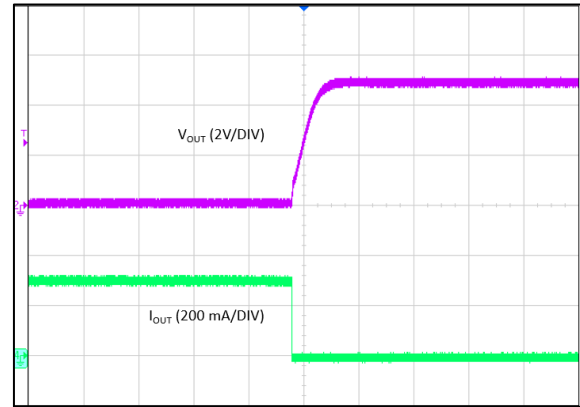
Typical Characteristics (Continued)

Unless otherwise stated, the test conditions are the same as Chapter 7.5. $T_J = -40^{\circ}\text{C}$ to 150°C .



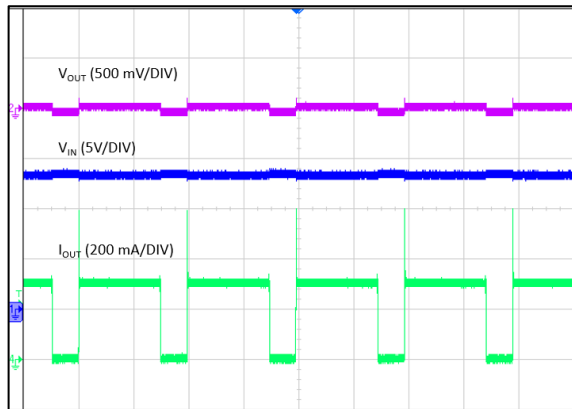
Time (200μs/DIV)
LN210421Q1, Adjustable $V_{OUT} = 5\text{V}$, $V_{IN} = 13.5\text{V}$

Figure 19. Short Circuit Entry



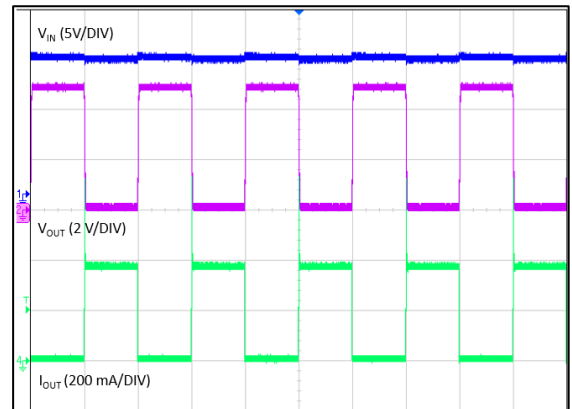
Time (200μs/DIV)
LN210421Q1, Adjustable $V_{OUT} = 5\text{V}$, $V_{IN} = 13.5\text{V}$

Figure 20. Short Circuit Recovery



Time (5ms/DIV)
LN210421Q1, Adjustable $V_{OUT} = 5\text{V}$, $V_{IN} = 13.5\text{V}$

Figure 21. Constant Short Circuit



Time (5ms/DIV)
LN210421Q1, Adjustable $V_{OUT} = 5\text{V}$, $V_{IN} = 13.5\text{V}$

Figure 22. Repetitive Short Circuit

8 FUNCTIONAL DESCRIPTION

8.1 Overview

LN21042Q1 are ultra-low quiescent current, low dropout linear regulators (LDO) with a wide input voltage range of 2.75V to 42V. The series provides 0.6V to 24V adjustable output and delivers up to 200mA output current. Typical shutdown current of LN21042Q1 is less than 1 μ A, while the quiescent current under no-load condition is 7.5 μ A.

LN21042Q1 features over-current protection and over-temperature shutdown with auto restart. The over-current threshold drops when the input voltage is above 28V.

The product family is available in DFN-EP8 package with wettable flanks and without wettable flank.

8.2 Functional Diagram

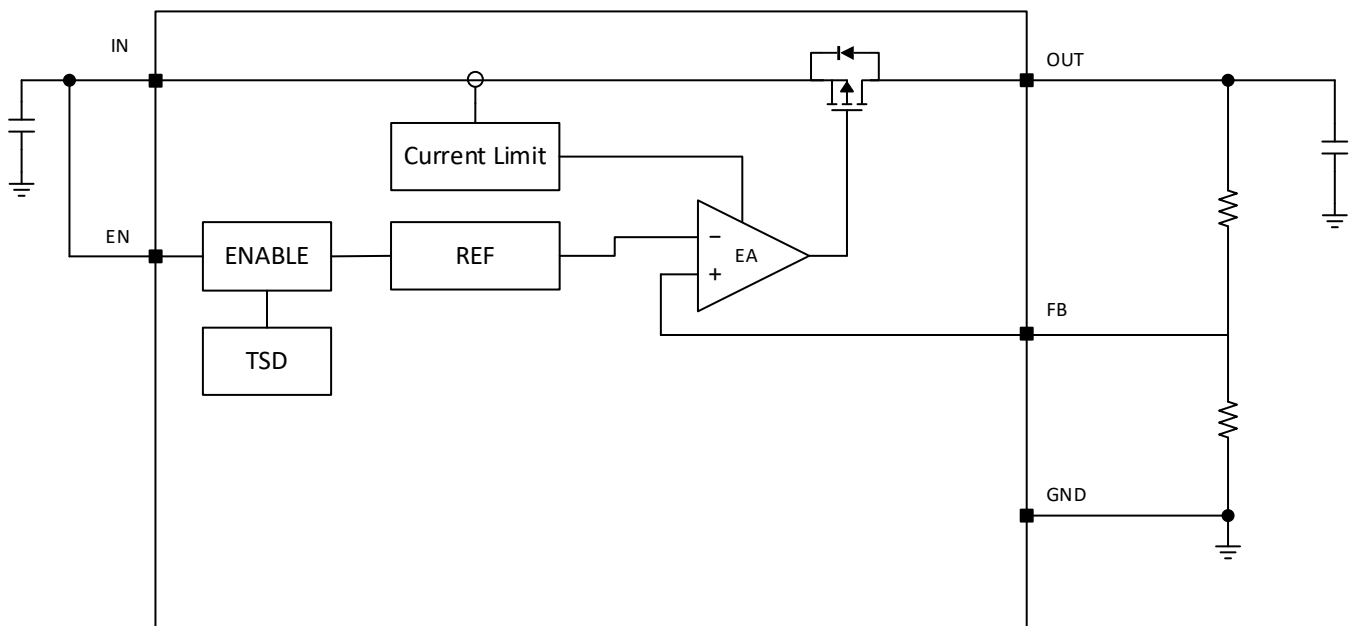


Figure 23. LN21042Q1 Functional Diagram

9 APPLICATIONS

9.1 Application Diagram

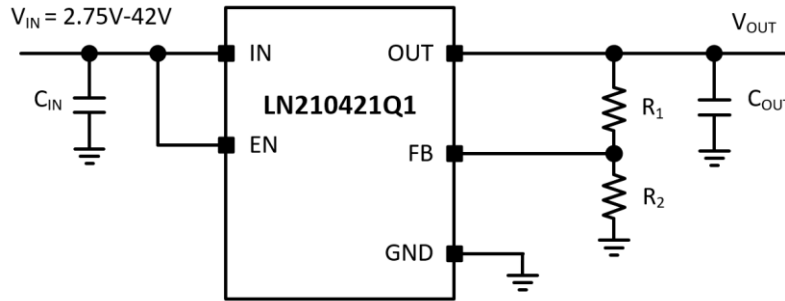


Figure 24. LN210421Q1 application diagram

9.2 Application Considerations

9.2.1 Input and Output Decouple Capacitors

For control loop stabilities, LN21042Q1 integrates internal compensation and only requires ceramic capacitors with minimum capacitance of 1μF between VIN and GND, and VOUT and GND, respectively. It is recommended that the capacitor is placed as close to the device pins as possible with minimum PCB trace length.

9.2.2 EN Pin

EN is the enable pin of the internal device supply and the output of the LDO. When the voltage on EN pin rises above the rising threshold V_{EN-H} , the LDO output is allowed; And when the voltage on EN falls below the falling threshold V_{EN-L} , the LDO output is disabled, and the device goes into shutdown mode. Another way of using EN pin is connecting EN directly to the input voltage, the pin has the same maximum operating voltage of 42V as the LDO input.

9.2.3 OUT and FB Pins

To adjust the output voltage, connect a voltage divider between OUT and GND, and connect the center of the divider to FB pin. The steady state V_{FB} is typically at 0.6V. The output voltage can be derived from:

$$V_{OUT} = \left(1 + \frac{R_1}{R_2}\right) \times V_{FB}$$

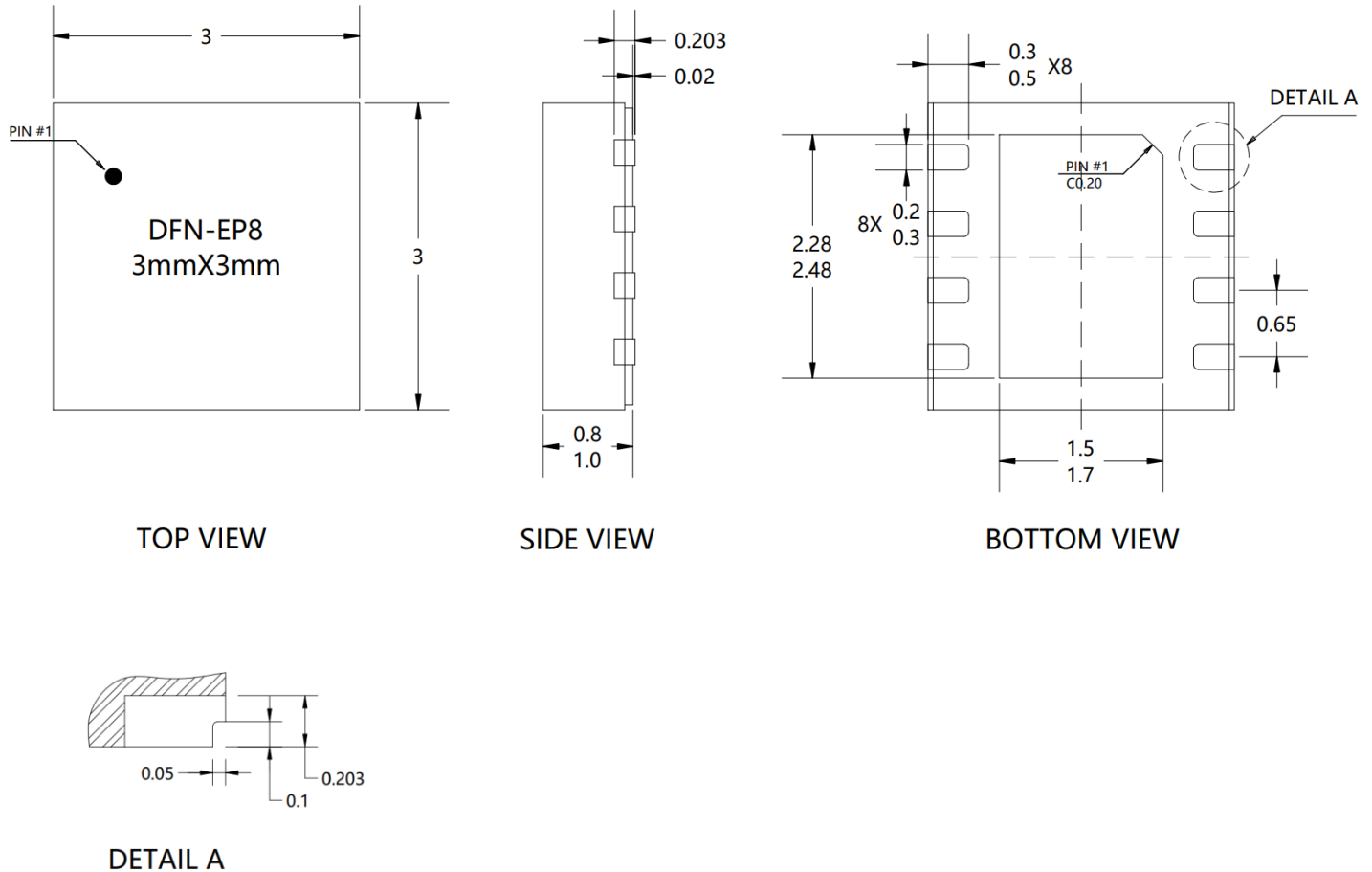
A typical selection of R_2 is 100kΩ, it is recommended to use resistor with tolerance better than 1%, and with temperature coefficient less than 100ppm. To achieve ultra-low I_Q , R_2 can be increased, but the upper limit should not exceed 1MΩ. After R_2 is selected, R_1 can then be calculated from:

$$R_1 = \frac{V_{OUT} - V_{FB}}{V_{FB}} \times R_2$$

10 PACKAGE INFORMATION

10.1 Package Outline

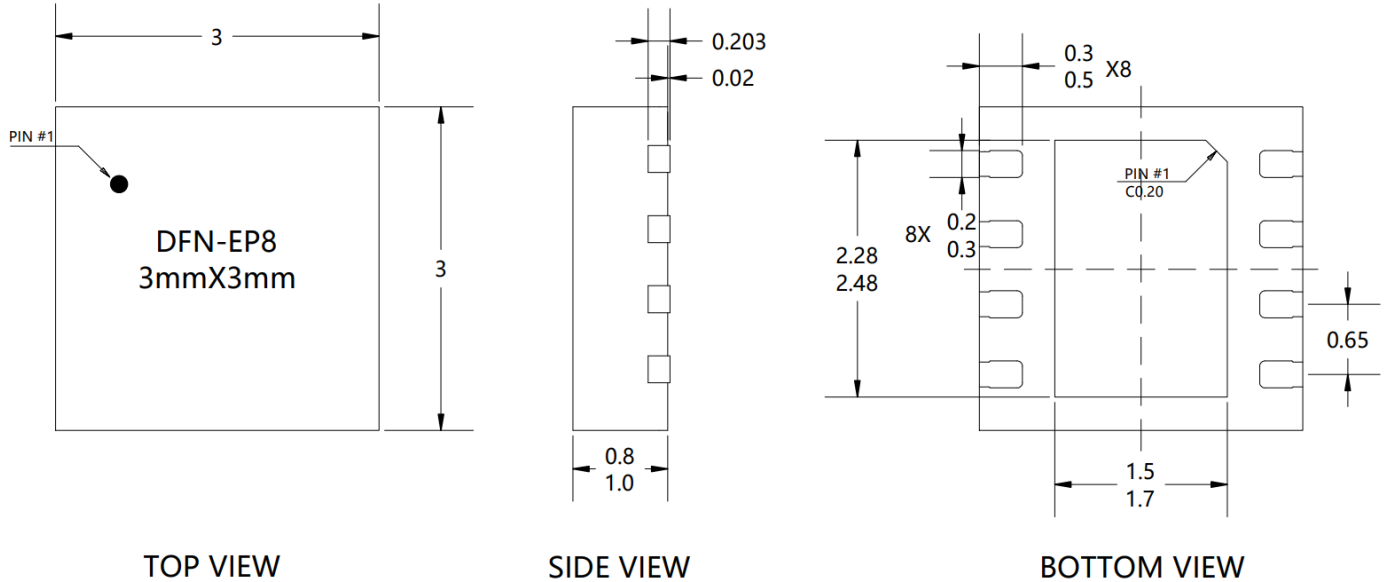
10.1.1 Package with Wettable Flanks (LN210421Q1CFR)



Notes:

1. All linear dimensions are in millimeters.
2. Dimensioning and tolerancing per ASME Y14.5-2009.
3. Both package length and width do not include mold flash.
4. Unremoved flash between leads & package end flash shall not exceed 0.15mm from bottom body per side.
5. Features may not be present.

10.1.2 Package without Wettable Flank (LN210421Q1NFR)



Notes:

1. All linear dimensions are in millimeters.
2. Dimensioning and tolerancing per ASME Y14.5-2009.
3. Both package length and width do not include mold flash.
4. Unremoved flash between leads & package end flash shall not exceed 0.15mm from bottom body per side.
5. Features may not be present.

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