SCY eMMC WITH HS400 INTERFACE

SPECIFICATION V1.31

E64GCYNT1ABE00
E128CYNT2ABE00

Contents

Introduction

SCY *eMMC*is an embedded MMC solution designed in a BGA package form. *eMMC*operation is identical to a MMC device and therefore is a simple read and write to memory using MMC protocol v5.1 which is an industry standard.

SCY *eMMC*enables manufacturers to bring the benefits of flash rapid boot-up, high reliability, robustness, consistent performance as well as many proprietary features to these new applications. It is easy to use as the MMC interface allows easy integration with any microprocessor with MMC host. Any revision or amendment of NAND is invisible to the host as the embedded MMC controller insulates NAND technology from the host. This leads to faster product development as well as faster times to market.

To fulfill the requirements of mobile application, SCY *eMMC*integrated LDPC ECC engine to enable the cost-effective leading-edge 3D NAND. SCY *eMMC*integrates optimized firmware and hardware that elevates its capabilities to include new algorithms that boost random sustained read/write performance. SCY *eMMC*provides powerful data protection architecture to deliver high endurance over the product lifecycle.

SCY *eMMC*employs an industry standard eMMC 5.1 interface featuring Command Queue, HS400 interface, FFU, as well as legacy eMMC 4.51 features such as power off notifications, packed commands, Cache, boot/RPMB partitions, HPI, and HW reset, making it an optimal device for both reliable code and data storage.

1. Product List

Capacity	Part Number	User Density (%)	Flash Type	Package Size	Pin Configuration
64GB	E64GCYNT1ABE00	91%	TLC 512Gbx1	11.5x13x1.0mm	153ball
128GB	E128CYNT2ABE00	91%	TLC 512Gbx2	11.5x13x1.0mm	153ball

Table 1-Product List

2. Key Features

■ JEDEC/e.MMC Standard version 5.1 Compatible (backward compatible to e.MMC 4.5)
- Supports a wide range of power supply voltage: 1.8 and 3.3V
- Supports HS400 Mode
- e.MMC production state awareness
- e.MMC device health report
- Supports Command Queue
- Programmable bus width: 1/4/8 bits
- Supports Boot operation in High Speed and DDR mode
- Supports Boot mode and Alternative Boot mode
- Replay Protection Memory Block (RPMB)
- Enhanced Partition Attributes
- High Priority Interrupt (HPI)
- Background operations
- Enhanced Reliable Write
- Secure removal types
- Enhance techniques: Sleep Notification in power off notification, data tagging, packed commands, discard, sanitize, RTC (real time clock)

■ LDPC ECC Engine
- Support multiple parity size with 1KB based codeword
- Support low-power decoding mode and high-correction capability decoding with soft information.

■ e.MMC Clock
- e.MMC I/F Clock Frequency : 0 ~ 200MHz
- e.MMC I/F Boot Frequency : 0 ~ 52MHz

■ Operation voltage range
- VCCQ (Power supply for e.MMC I/F) : 1.7V~1.95V or 2.7V~3.6V
- VDD (Power supply for internal flash) : 2.7V~3.6V

■ Temperature
- Operation : -25℃ ~ +85℃
- Storage : -40℃ ~ +85℃

■ RoHS compliant

3. Package Configurations

3.1 BGA 153 Ball Pin Configurations

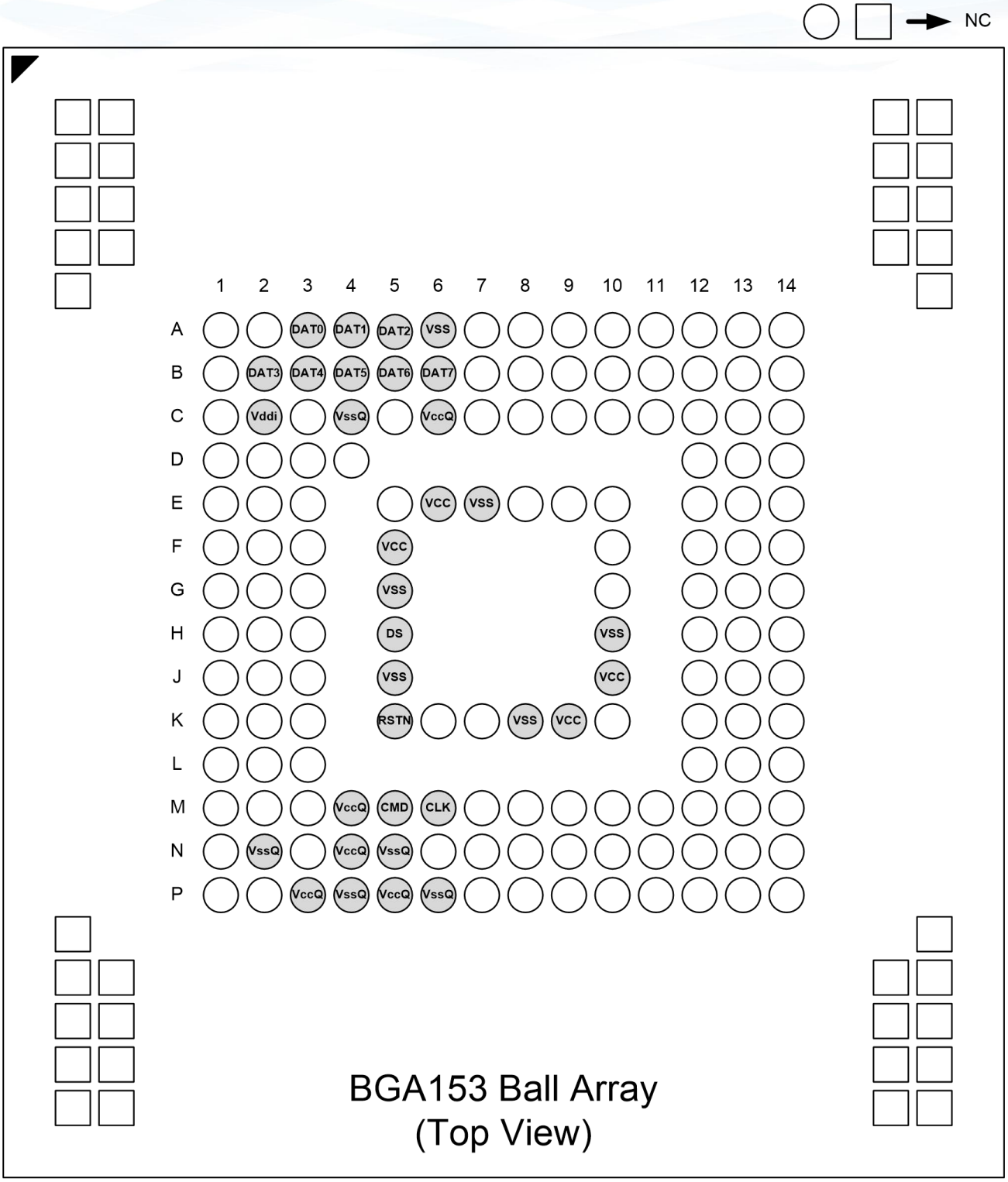


Figure 1-153 balls – Ball Array (Top View)

3.2 Pins and Signal Description

Table 2 contains the *eMMC*functional pins assignment.

Pin Number	Name	Pin Number	Name	Pin Number	Name	Pin Number	Name
A3	DAT0	C2	VDDi	J5	VSS	N4	VCCQ
A4	DAT1	C4	VSSQ	J10	VCC	N5	VSSQ
A5	DAT2	C6	VCCQ	K5	RSTN	P3	VCCQ
A6	VSS	E6	VCC	K8	VSS	P4	VSSQ
B2	DAT3	E7	VSS	K9	VCC	P5	VCCQ
B3	DAT4	F5	VCC	M4	VCCQ	P6	VSSQ
B4	DAT5	G5	VSS	M5	CMD		
B5	DAT6	H5	DS	M6	CLK		
B6	DAT7	H10	VSS	N2	VSSQ		

Table 2-eMMCFunction Pins Assignment

- CLK : Clock input
- DS : Data Strobe is generated from eMMC to host.
- In HS400 mode, read data and CRC response are synchronized with Data Strobe.
- CMD : A bidirectional signal used for device initialization and command transfers.
- Command operates in two modes, open-drain for initialization and push-pull for fast command transfer.
- DAT0-7 : Bidirectional data channels. It operates in push-pull mode.
- RSTN : H/W reset signal pin
- VCC : Supply voltage for flash memory
- VCCQ : Supply voltage for memory controller
- VDDi : Internal power node to stabilize regulator output to controller core logics
- VSS : Ground connections
- NC : No Connection and left floating.

3.3 BGA Package Dimension

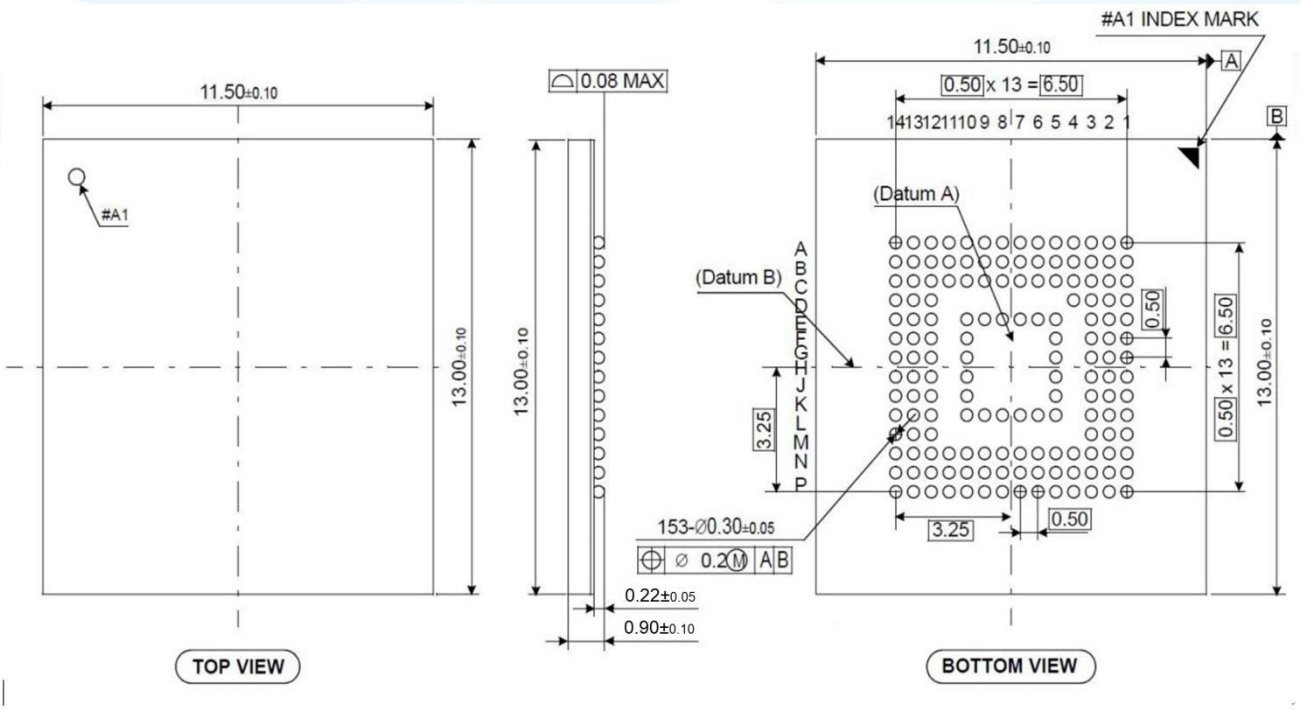


Figure 3-BGA 11.5x13x1.0mm Package Dimension

3.4 Product Block Diagram

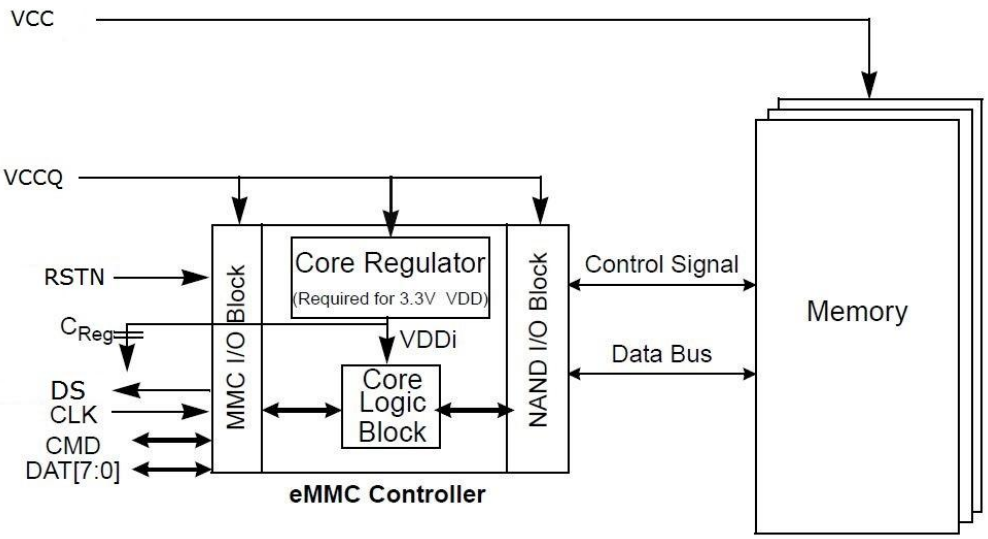


Figure 4-*eMMC*Block Diagram

4. S/W Algorithm

4.1 Partition Management

eMMCoffers the possibility for the host to configure additional split local memory partitions with independent addressable space starting from logical address 0x00000000 for different usage models. Therefore memory block area can be classified as follows Factory configuration supplies two boot partitions implemented as enhanced storage media and one RPMB partitioning of 4MB in size.

Up to four General Purpose Area Partitions can be configured to store user data or sensitive data, or for other host usage models. The size of these partitions is a multiple of the write protect group.

4.2 Enhanced Partition (Area)

SCY eMMCadopts Enhanced User Data Area as SLC Mode. Therefore when master adopts some portion as enhanced user data area in User Data Area, that area occupies triple size of original set up size. (ex> if master set 1MB for enhanced mode, total 3MB user data area is needed to generate 1MB enhanced area)

Max Enhanced User Data Area size is defined as (MAX_ENH_SIZE_MULT x HC_WP_GRP_SIZE x HC_ERASE_GRP_SIZE x 512kBytes)

4.3 User Density

Total User Density depends on device type. Different eMMCpart ID has different user density. Figure 5 shows the space allocations in a eMMCdevice.

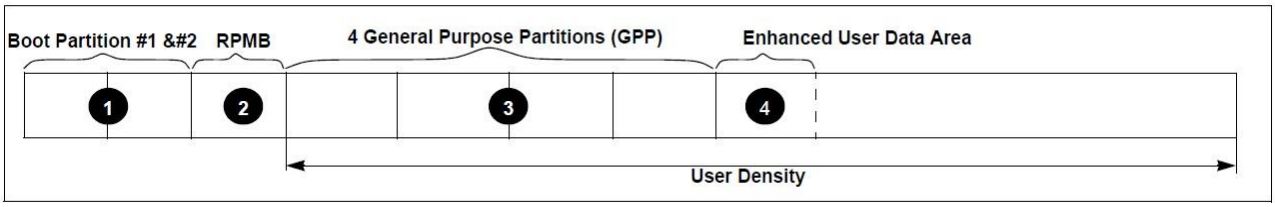


Figure 5-Space Allocation in sNAND

apacity	Boot Partition 1	Boot Partition 2	RPMB
64GB	4,096KB	4,096KB	4,096KB
128GB	4,096KB	4,096KB	4,096KB

Table 3-Capacity According to Partition

Capacity	User Density Size	Max. Enhanced Partition Size
64GB	62,528,684,032Bytes	20,837,302,272 Bytes
128GB	125,057,368,064 Bytes	20,837,302,272 Bytes

Table 4 User Density & Max. Enhanced Partition Size

4.4 Typical Performance

Capacity	Mode	Sequential Read (MB/s)	Sequential Write (MB/s)
64GB	HS400	Up to 301	Up to 157
128GB	HS400	Up to 302	Up to 245

Table 5-Typical Performance

Table 5 shows the bench test with card reader. The testing result is only for reference. Any change in testing environment may cause big difference in performance result.Test tool with card reader、uBOOT、without O/S

4.5 Power Consumption

4.5.1 Operating Current (RMS)

Capacity	eMMC Mode	Domain	Read	Write	Unit
64GB	HS400	ICC	44.3	35.6	mA
		ICCQ	101.3	69.9	
128GB		ICC	45.6	36.1	
		ICCQ	97.5	74.4	

* The measurement for current is the average RMS current consumption over a period of 100ms

* Typical value is measured at TA=25° C.

4.5.2 Standby Power Consumption in auto power saving mode and standby state

Capacity	State	ICC	ICCQ	Unit
64GB	Standby	82	69	uA
128GB		82	69	

* Power Measurement conditions: Bus configuration = x8, No CLK

* Typical value is measured at TA=25° C. Not 100% tested.

4.5.3 Sleep Power Consumption

Capacity	State	ICC	ICCQ	Unit
64GB	Sleep	0	70.8	uA
128GB		0	70.8	

* Power Measurement conditions: Bus configuration = x8, No CLK

* Enter sleep state by CMD5, VCC power is switched off. Not 100% tested.

5. *eMMC*Features Overview

e.MMC	Device Features	Function	Support
N/A	INTERFACE	Speed	HS400
N/A	BUS SPEED	Max Speed	Up to 400MB/s
4.41	SECURE ERASE/TRIM	“True Wipe”	Yes
4.41	BOOT AND MASS STORAGE	One storage device (reduced BOM)	YES
4.41	PARTITION & PROTECTION	Flexibility	YES
4.41	BACKGROUND OPERATIONS	Better user experience (low latency)	YES
4.41	POWER OFF NOTIFICATION	Faster Boot; Responsiveness	YES
4.41	HARDWARE RESET	Robust system design	YES
4.41	HPI	Control long Reads/Writes	YES
4.41	RPMB	Secure folders	YES
4.5	EXTENDED PARTITION ATTRIBUTE	Flexibility	YES
4.5	LARGE SECTOR SIZE	Potential performance	NO
4.5	PACKED COMMANDS	Reduce host overhead	YES
4.5	DISCARD	Improved performance on full media	YES
4.5	DATA TAG	Performance and/or Reliability	YES
4.5	CONTEXT MANAGEMENT	Performance and/or Reliability	YES
4.5	CACHE	Better sequential & random writes	YES
4.51	SANITIZE	“True Wipe”	YES
5.0	FIELD FIRMWARE UPGRADE (FFU)	Enables feature enhancements	YES
5.0	PRODUCTION STATE AWARENESS	Different operation during production	YES
5.0	DEVICE HEALTH	Vital NAND info	YES
5.1	ENHANCE STROBE	Sync Device and Host in HS400	YES
5.1	COMMAND QUEUE	Responsiveness	YES
5.1	RPMB THROUGHPUT	Faster RPMB write throughput	YES
5.1	CACHE FLUSH AND BARRIER	Order cache flushing	YES
5.1	BKOPS CONTROLLER	Host control on BLOPs	YES
5.1	SECURE WP	Secure write protect	YES

5.1	EUDA	Enhance User Data Area	YES

Table 7-*eMMC*Feature Overview

5.1 HS400 Interface

Industrial *eMMC*supports HS400 signaling to achieve a bus speed of 400 MB/s via a 200MHz dual data rate clock frequency. HS400 mode supports 8 bits bus width and the 1.7 – 1.95 VCCQ option. Due to the speed, the host may need to have an adjustable sampling point to reliably receive the incoming data.

5.2 Field Firmware Upgrade (FFU)

Field Firmware Updates (FFU) enables features enhancement in the field. Using this mechanism, the host downloads a new version of the firmware to the *eMMC*device and instructs the *eMMC*device to install the new downloaded firmware into the device. The entire FFU process occurs in the background without affecting the user/OS data. During the FFU process, the host can replace firmware files or single/all file systems.

5.3 Cache

The *eMMC*cache is dedicated volatile memory at the size of 512KB. Caching enables to improve *eMMC*performance for both sequential and random access.

5.4 Discard

*eMMC*supports discard command as defined in e.MMC 5.1 spec. This command allows the host to identify data which is not needed, without requiring the device to remove the data from the Media. It is highly recommended for use to guarantee optimal performance of *eMMC*and reduce amount of housekeeping operation.

5.5 Power off Notification

*eMMC*supports power off notifications as defined in e.MMC 5.1 spec. The usage of power off notifications allows the device to prepare itself to power off, and improve user experience during power-on. Note that the device may be set into sleep mode while power off notification is enabled.

Power off notification long allows the device to shutdown properly and save important data for fast boot time on the next power cycle.

5.6 Packed Commands

To enable optimal system performance, *eMMC*supports packed commands as defined in e.MMC 5.1 spec. It allows the host to pack Read or Write commands into groups (of single type of operation) and transfer these to the device in a single transfer on the bus. Thus, it allows reducing overall bus overheads.

5.7 Sleep (CMD5)

*eMMC*may be switched between a Sleep and a Standby state using the SLEEP/AWAKE (CMD5). In the Sleep state the power consumption of the memory device is minimized and the memory device reacts only to the commands RESET (CMD0) and SLEEP/AWAKE (CMD5). All the other commands are ignored by the memory device.

The VCC power supply may be switched off in Sleep state to enable even further system power consumption saving.

5.8 Enhanced Reliable Write

*eMMC*supports enhanced reliable write as defined in e.MMC 5.1 spec. Enhanced reliable write is a special write mode in which the old data pointed to by a logical address must remain unchanged until the new data written to same logical address has been successfully programmed. This is to ensure that the target address updated by the reliable write transaction never contains undefined data. When writing in reliable write, data will remain valid even if a sudden power loss occurs during programming.

5.9 Sanitize

The Sanitize operation is used to remove data from the device. The use of the Sanitize operation requires the device to physically remove data from the unmapped user address space. The device will continue the sanitize operation, with busy asserted, until one of the following events occurs:

- Sanitize operation is complete
- HPI is used to abort the operation
- Power failure
- Hardware reset

After the sanitize operation is complete no data should exist in the unmapped host address space.

5.10 Secure Erase

For backward compatibility reasons, in addition to the standard erase command the *eMMC*supports the optional Secure Erase command.

This command allows the host to erase the provided range of LBAs and ensure no older copies of this data exist in the flash.

5.11 Secure Trim

For backward compatibility reasons, *eMMC*supports Secure Trim command. The Secure Trim command is similar to the Secure Erase command but performs a secure purge operation on write blocks instead of erase groups.

5.12 High Priority Interrupt (HPI)

The operating system usually uses demand-paging to launch a process requested by the user. If the host needs to fetch pages while in a middle of a write operation the request will be delayed until the completion of the write command.

The high priority interrupt (HPI) as defined in eMMC 5.1 spec enables low read latency operation by suspending a lower priority operation before it is actually completed.

5.13 H/W Reset

Hardware reset may be used by host to reset the device, moving the device to a Pre-idle state and disabling the power-on period write protect on blocks that were power-on write protected before the reset was asserted.

5.14 Command Queue

*eMMC*Command Queue enables device visibility of next commands and allows performance improvement. The protocol allows the host to queue up to 32 data-transfer commands in the device by implementing 5 new commands.

The benefits of command queuing are:

- Random Read performance improvement (higher IOPs)
- Reducing protocol overhead
- Command issuance allowed while data transfer is on-going
- Device order the tasks according to best access to/from flash

6. Register Value

6.1 OCR Register

Parameter	DSR Slice Bit	Description	Value	Bit Width
Access Mode	[30:29]	Access mode	2h	2
	[23:15]	VDD: 2.7 - 3.6 range	1FFh	9
	[14:8]	VDD: 2.0 - 2.6 range	00h	7
	[7]	VDD: 1.7 - 1.95 range	1h	1

Table 8-OCR Register

6.2 CID Register

Parameter	DSR Slice Bit	Description	Value	Bit Width
MMC MID	[127:120]	Manufacturer ID	DFh	8
CBX	[113:112]	Card BGA	01h	2
OID	[111:104]	OEM/Application ID	18h	8
PNM	[103:56]	Product name	64G : “SCA64G” 128G : “SCA128”	48
PRV	[55:48]	Product revision	10h	8
PSN	[47:16]	Product serial number	Defined by Production	32
MDT	[15:8]	Manufacturing date	Month, year	8
CRC	[7:1]	Calculated CRC	CRC7 Generator	7

Table 9-CID Register

6.3 DSR Register

Parameter	DSR Slice Bit	Description	Value	Bit Width
RSRVD	[15:8]	Reserved	04h	8
RSRVD	[7:0]	Reserved	04h	8

Table 10-DSR Register

6.4 CSD Register

Parameter	DSR slice Bit	Description	Value	Width Bit
CSD_STRUCTURE	[127:126]	CSD structure	3h	2
SPEC_VERS	[125:122]	System specification version	4h	4
TAAC	[119:112]	Data read access-time 1 27h = 15ms	27h	8
NSAC	[111:104]	Data read access-time 2 in CLK cycles (NSAC*100)	01h	8
TRAN_SPEED	[103:96]	Max. bus clock frequency	32h	8
CCC	[95:84]	Card command classes	0F5h	12
READ_BL_LEN	[83:80]	Max. read data block length	9h	4
READ_BL_PARTIAL	[79]	Partial blocks for read allowed	0h	1
WRITE_BLK_MISALIGN	[78]	Write block misalignment	0h	1
READ_BLK_MISALIGN	[77]	Read block misalignment	0h	1
DSR_IMP	[76]	DSR implemented	0h	1
C_SIZE	[73:62]	Device size	FFFh	12
VDD_R_CURR_MIN	[61:59]	Max. read current @ VDD min	7h	3
VDD_R_CURR_MAX	[58:56]	Max. read current @ VDD max	7h	3
VDD_W_CURR_MIN	[55:53]	Max. write current @ VDD min	7h	3
VDD_W_CURR_MAX	[52:50]	Max. write current @ VDD max	7h	3
C_SIZE_MULT	[49:47]	Device size multiplier	7h	3
ERASE_GRP_SIZE	[46:42]	Erase group size	1Fh	5
ERASE_GRP_MULT	[41:37]	Erase group size multiplier	1Fh	5
WP_GRP_SIZE	[36:32]	Write protect group size	1Fh	5
WP_GRP_ENABLE	[31:31]	Write protect group enable	1h	1
DEFAULT_ECC	[30:29]	Manufacturer default	0h	2
R2W_FACTOR	[28:26]	Write speed factor	2h	3
WRITE_BL_LEN	[25:22]	Max. write data block length	9h	4
WRITE_BL_PARTIAL	[21]	Partial blocks for write allowed	0h	1
CONTENT_PROT_APP	[16]	Content protection application	0h	1
FILE_FORMAT_GRP	[15]	File format group	0h	1
COPY	[14]	Copy flag (OTP)	1h	1
PERM_WRITE_PROTECT	[13]	Permanent write protection	0h	1
TMP_WRITE_PROTECT	[12]	Temporary write protection	0h	1
FILE_FORMAT	[11:10]	File format	0h	2
ECC	[9:8]	ECC code	0h	2
CRC	[7:1]	Calculated CRC	CRC7 Generator	7

Table 11-CSD Register

6.5 EXT_CSD Register

Parameter	DSR slice Byte	Description	Value
EXT_SECURITY_ERR	[505]	Extended Security Commands Error	0h
S_CMD_SET	[504]	Supported Command Sets	1h
HPI_FEATURES	[503]	HPI Features	1h
BKOPS_SUPPORT	[502]	Background operations support	1h
MAX_PACKED_READS	[501]	Max packed read commands	20h
MAX_PACKED_WRITES	[500]	Max packed write commands	20h
DATA_TAG_SUPPORT	[499]	Data Tag Support	1h
TAG_UNIT_SIZE	[498]	Tag Unit Size	0h
TAG_RES_SIZE	[497]	Tag Resources Size	0h
CONTEXT_CAPABILITIES	[496]	Context management capabilities	78h
LARGE_UNIT_SIZE_M1	[495]	Large Unit size	1h
EXT_SUPPORT	[494]	Extended partitions attribute support	3h
SUPPORTED_MODES	[493]	FFU supported modes	1h
FFU_FEATURES	[492]	FFU features	0h
OPERATION_CODES_TIMEOUT	[491]	Operation codes timeout	17h
FFU_ARG	[490:487]	FFU Argument	FFFAFFF0h
BARRIER_SUPPORT	[486]	Cache barrier support	1h
CMDQ_SUPPORT	[308]	Command queue support	1h
CMDQ_DEPTH	[307]	Command queue depth	1Fh
NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED	[305:302]	Number of FW sectors correctly programmed	0h
VENDOR_PROPRIETARY_HEALTH_REPORT	[301:270]	Vendor proprietary health report	0h
DEVICE_LIFE_TIME_EST_TYP_B	[269]	Device life time estimation type B (TLC)	64GB=01h 128GB=00h
DEVICE_LIFE_TIME_EST_TYP_A	[268]	Device life time estimation type A (SLC)	64GB=01h 128GB=00h
PRE_EOL_INFO	[267]	Pre EOL information	64GB=01h 128GB=00h
OPTIMAL_READ_SIZE	[266]	Optimal read size	40h
OPTIMAL_WRITE_SIZE	[265]	Optimal write size	40h
OPTIMAL_TRIM_UNIT_SIZE	[264]	Optimal trim unit size	7h
DEVICE_VERSION	[263:262]	Device version	64GB = 4305h 128GB = 4405h
FIRMWARE_VERSION	[261:254]	Firmware version	00B0022031000010h
PWR_CL_DDR_200_360	[253]	Power class for 200MHz, DDR at	00h

		VCC= 3.6V	
CACHE_SIZE	[252:249]	Cache size	0400h
GENERIC_CMD6_TIME	[248]	Generic CMD6 timeout	10h
POWER_OFF_LONG_TIME	[247]	Power off notification (long) timeout	64h
BKOPS_STATUS	[246]	Background operations status	Default = 0h
CORRECTLY_PRG_SECTORS_NUM	[245:242]	Number of correctly programmed sectors	Default = 0h
INI_TIMEOUT_AP	[241]	1st Initialization time after partitioning	0Ah
CACHE_FLUSH_POLICY	[240]	Cache Flush Policy	1h
PWR_CL_DDR_52_360	[239]	Power class for 52MHz, DDR at VCC = 3.6V	0h
PWR_CL_DDR_52_195	[238]	Power class for 52MHz, DDR at VCC = 1.95V	00h
PWR_CL_200_195	[237]	Power class for 200MHz at VCCQ = 1.95V, VCC = 3.6V	00h
PWR_CL_200_130	[236]	Power class for 200MHz, at VCCQ =1.3V, VCC = 3.6V	0h
MIN_PERF_DDR_W_8_52	[235]	Minimum Write Performance for 8bit at 52MHz in DDR mode	0h
MIN_PERF_DDR_R_8_52	[234]	Minimum Read Performance for 8bit at 52MHz in DDR mode	0h
TRIM _MULT	[232]	TRIM Multiplier	2h
SEC_FEATURE_SUPPORT	[231]	Secure Feature support	55h
SEC_ERASE_MULT	[230]	Secure Erase Multiplier	64GB = 19h 128GB = 32h
SEC_TRIM_MULT	[229]	Secure TRIM Multiplier	0Ah
BOOT_INFO	[228]	Boot Information	7h
BOOT_SIZE_MULT	[226]	Boot partition size	20h
ACCESS_SIZE	[225]	Access size	6h
HC_ERASE_GROUP_SIZE	[224]	High Capacity Erase unit size	1h
ERASE_TIMEOUT_MULT	[223]	High capacity erase time out	2h
REL_WR_SEC_C	[222]	Reliable write sector count	05h
HC_WP_GRP_SIZE	[221]	High capacity write protect group size	20h
S_C_VCC	[220]	Sleep current [VCC]	7h
S_C_VCCQ	[219]	Sleep current [VCCQ]	7h
PRODUCTION_STATE_AWARENESS_TIMEOUT	[218]	Production state awareness timeout	17h
S_A_TIMEOUT	[217]	Sleep/Awake time out	12h
SLEEP_NOTIFICATION_TIME	[216]	Sleep notification timeout	0Ch
SEC_COUNT	[215:212]	Sector count	64GB = 07478000h 128GB =

			0E8F0000h
SECURE_WP_INFO	[211]	Secure Write Protect Info	1h
MIN_PERF_W_8_52	[210]	Minimum Write Performance for 8bit @52MHz	0h
MIN_PERF_R_8_52	[209]	Minimum Read Performance for 8bit @52MHz	0h
MIN_PERF_W_8_26_4_52	[208]	Minimum Write Performance for 4bit @52MHz or @26MHz	0h
MIN_PERF_R_8_26_4_52	[207]	Minimum Read Performance for 4bit @52MHz or @26MHz	0h
MIN_PERF_W_4_26	[206]	Minimum Write Performance for 4bit @26MHz	0h
MIN_PERF_R_4_26	[205]	Minimum Read Performance for 4bit @26MHz	0h
PWR_CL_26_360	[203]	Power Class for 26MHz @ 3.6V	0h
PWR_CL_52_360	[202]	Power Class for 52MHz @ 3.6V	0h
PWR_CL_26_195	[201]	Power Class for 26MHz @ 1.95V	00h
PWR_CL_52_195	[200]	Power Class for 52MHz @ 1.95V	0h
PARTITION_SWITCH_TIME	[199]	Partition switching timing	0Ah
OUT_OF_INTERRUPT_TIME	[198]	Out-of-interrupt busy timing	0Ah
DRIVER_STRENGTH	[197]	I/O Driver Strength	1Fh
CARD_TYPE	[196:195]	Card Type	57h
CSD_STRUCTURE	[194]	CSD Structure Version	2h
EXT_CSD_REV	[192]	Extended CSD Revision	8h
CMD_SET	[191]	Command Set	Default = 0h Updated in runtime
CMD_SET_REV	[189]	Command Set Revision	0h
POWER_CLASS	[187]	Power Class	0h
HS_TIMING	[185]	High Speed Interface Timing	Default = 1h Updated in runtime by host
DATA_STRB_MODE_SUPPORT	[184]	Data strobe mode support	1h
BUS_WIDTH	[183]	Bus Width Mode	Default = 2h Updated in runtime by host
ERASE_MEM_CONT	[181]	Content of explicit erased memory range	0h
PARTITION_CONFIG	[179]	Partition Configuration	Default = 0h Updated in

			runtime by host
BOOT_CONFIG_PROT	[178]	Boot config protection	Default = 0h Updated in runtime by host
BOOT_BUS_CONDITIONS	[177]	Boot bus width1	Default = 0h Updated in runtime by host
ERASE_GROUP_DEF	[175]	High-density erase group definition	Default = 0h Updated in runtime by host
BOOT_WP_STATUS	[174]	Boot write protection status registers	Default = 0h Updated in runtime by host
BOOT_WP	[173]	Boot area write protect register	0h
USER_WP	[171]	User area write protect register	0h
FW_CONFIG	[169]	FW Configuration	0h
RPMB_SIZE_MULT	[168]	RPMB Size	20h
WR_REL_SET	[167]	Write reliability setting register	1Fh
WR_REL_PARAM	[166]	Write reliability parameter register	15h
SANITIZE_START	[165]	Start Sanitize operation	Default = 0h Updated in runtime by host
BKOPS_START	[164]	Manually start background operations	Default = 0h Updated in runtime by host
BKOPS_EN	[163]	Enable background operations handshake	00h
RST_n_FUNCTION	[162]	H/W reset function	Default = 0h Updated by host
HPI_MGMT	[161]	HPI management	Default = 0h Updated by host
PARTITIONING SUPPORT	[160]	Partitioning support	07h
MAX_ENH_SIZE_MULT	[159:157]	Max Enhanced Area Size	64GB = 4DAh 128GB = 4DAh

PARTITIONS_ATTRIBUTE	[156]	Partitions Attribute	Default = 0h Updated by host
PARTITION_SETTING_COMPLETED	[155]	Partitioning Setting	Default = 0h Updated by host
GP_SIZE_MULT	[154:153]	General Purpose Partition Size (GP4)	0h
GP_SIZE_MULT	[151:149]	General Purpose Partition Size (GP3)	0h
GP_SIZE_MULT	[148:146]	General Purpose Partition Size (GP2)	0h
GP_SIZE_MULT	[145:143]	General Purpose Partition Size (GP1)	0h
ENH_SIZE_MULT	[142:140]	Enhanced User Data Area Size	0h
ENH_START_ADDR	[139:136]	Enhanced User Data Start Address	0h
SEC_BAD_BLK_MGMNT	[134]	Bad Block Management mode	0h
PRODUCTION_STATE_AWARENESS	[133]	Production state awareness	0h
TCASE_SUPPORT	[132]	Package Case Temperature is controlled	0h
PERIODIC_WAKEUP	[131]	Periodic Wake-up	0h
PROGRAM_CID_CSD_DDR_SUPPORT	[130]	Program CID/CSD in DDR mode support	1h
VENDOR_SPECIFIC_FIELD	[127:87]	Vendor Specific Fields	Reserved
PWR_CL_DDR_266	[86]	Maximum power class for HS533	0h
CARD_TYPE_2ND_INDEX	[84]	Device HS533 support	0h
SKU_FEATURES_ID	[83]	SKU identification	0h
VENDOR_SPECIFIC_FIELD	[82:64]	Vendor Specific Fields	Reserved
NATIVE_SECTOR_SIZE	[63]	Native sector size	01h
USE_NATIVE_SECTOR	[62]	Sector size emulation	0h
DATA_SECTOR_SIZE	[61]	Sector size	0h
INI_TIMEOUT_EMU	[60]	1st initialization after disabling sector size emulation	0Ah
CLASS_6_CTRL	[59]	Class 6 commands control	0h
DYNCAP_NEEDED	[58]	Number of addressed group to be Released	0h
EXCEPTION_EVENTS_CTRL	[57:56]	Exception events control	0h
EXCEPTION_EVENTS_STATUS	[55:54]	Exception events status	0h
EXT_PARTITIONS_ATTRIBUTE	[53:52]	Extended Partitions Attribute	0h
CONTEXT_CONF	[51:37]	Context configuration	Default = 0h
PACKED_COMMAND_STATUS	[36]	Packed command status	Default = 0h Updated in runtime
PACKED_FAILURE_INDEX	[35]	Packed command failure index	Default = 0h

			Updated in runtime
POWER_OFF_NOTIFICATION	[34]	Power Off Notification	Default = 0h Update in runtime by the host
CACHE_CTRL	[33]	Control to turn the Cache ON/OFF	0h
FLUSH_CACHE	[32]	Flushing of the cache	0h
BARRIER_CTRL	[31]	Cache barrier	0h
MODE_CONFIG	[30]	Mode config	0h
MODE_OPERATION_CODES	[29]	Mode operation codes	0h
FFU_STATUS	[26]	FFU status	0h
PRE_LOADING_DATA_SIZE	[25:22]	Pre loading data size	0h
MAX_PRE_LOADING_DATA_SIZE	[21:18]	Max pre loading data size	64GB = 266AAAAh 128GB = 4DAAAAAh
PRODUCT_STATE_AWARENESS_ENABLEMENT	[17]	Product state awareness enablement	01h AUTO_PRE_SOLDERING
SECURE_REMOVAL_TYPE	[16]	Secure Removal Type	3Bh
CMDQ_MODE_EN	[15]	Command queue	0h

Table 12-EXT_CSD Register

7. Electrical Characteristics

7.1 Supply Voltage

Permanent damage to eMMCmay occur if the supply voltages are exceeded. These are only stress ratings, and the functional operations should be restricted with the conditions detailed in the following table. Exposure to the absolute maximum rating conditions may also affect the reliability of the devices. The input and output negative voltage ratings may be exceeded if the input and output currents are not exceeded.

Parameter	Symbol	Min	Max	Unit
Supply Voltage	VCCQ(Low)	1.7	1.95	V
	VCCQ(High)	2.7	3.6	V
	VCC	2.7	3.6	V

	VSS, VSSQ	-0.3	0.3	V

Table 13-Supply Voltage

7.2 Bus Signal Levels

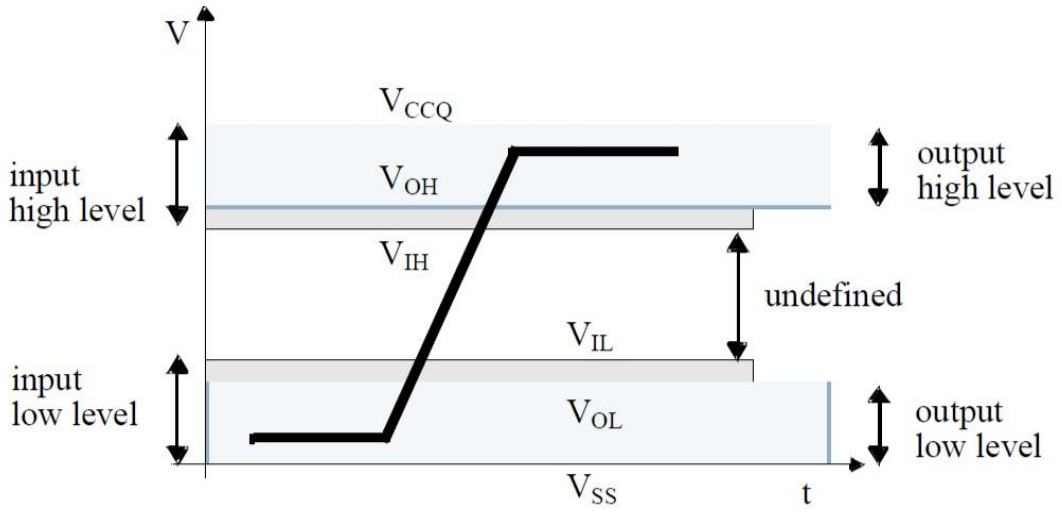


Figure 6-Bus Signal Levels

Symbol	Min	Max	Unit	Remark
Open-drain bus signal level				
VOH	VCCQ – 0.2		V	
VOL		0.3	V	IOL = 2mA
Push-pull bus signal level (2.7V~3.6V VCCQ)				
VOH	0.75*VCCQ		V	IOH = -100mA @VCC min
VOL		0.125*VCCQ	V	IOL = 100mA @VCC min
VIH	0.625*VCCQ	VCCQ + 0.3	V	
VIL	VSSQ – 0.3	0.25*VCCQ	V	
Push-pull bus signal level (1.70V~1.95V VCCQ)				
VOH	VCCQ – 0.45		V	IOH = -2mA
VOL		0.45	V	IOL = 2mA
VIH	0.65*VCCQ	VCCQ + 0.3	V	

VIL	VSSQ – 0.3	0.35*VCCQ	V	

Table 14-Bus Signal Level

7.3 Bus Timing in Single Data Rate Mode

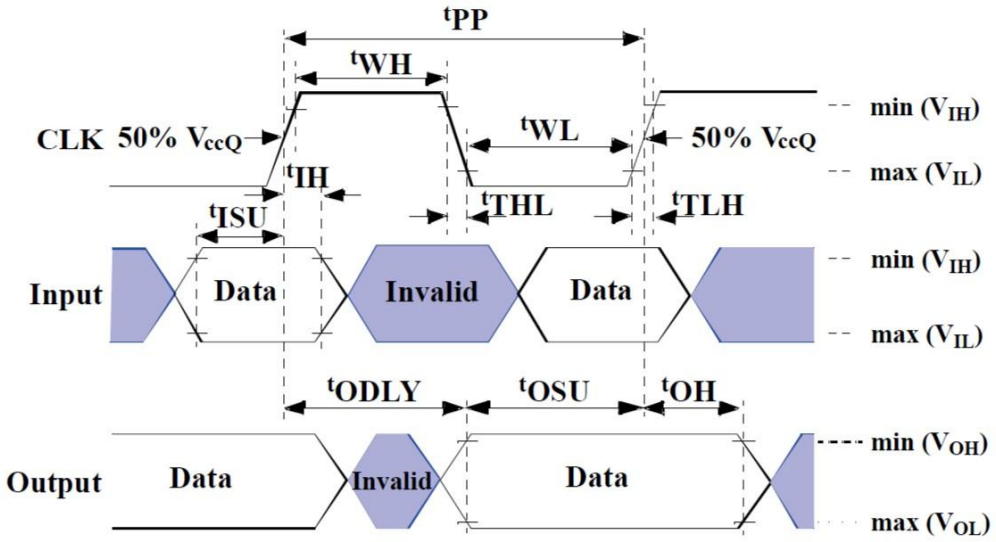


Figure 7-Bus Timing in Single Data Rate Mode

Symbol	Min	Max	Unit	Remark
fPP	0	52	Mhz	Clock frequency data transfer mode, CL <= 30pF Tolerance + 100kHz
fOD	0	400	kHz	Clock frequency identification mode Tolerance +20kHz
tWH	6.5		ns	CL <= 30pF
tWL	6.5		ns	CL <= 30pF
tTLH		3	ns	CL <= 30pF
tTHL		3	ns	CL <= 30pF
2.7V~3.6V VCCQ				
tISU	3		ns	CL <= 30pF
tIH	3		ns	CL <= 30pF
tODLY		13.7	ns	CL <= 30pF

tOH	2.5		ns	CL <= 30pF
tRISE		3	ns	CL <= 30pF
tFALL		3	ns	CL <= 30pF
1.70V~1.95V VCCQ				
tISU	3		ns	CL <= 30pF
tIH	3		ns	CL <= 30pF
tODLY		13.7	ns	CL <= 30pF
tOH	2.5		ns	CL <= 30pF
tRISE		3	ns	CL <= 30pF
tFALL		3	ns	CL <= 30pF

Table 15-High-Speed Device Interface Timing

Symbol	Min	Max	Unit	Remark
fPP	0	26	Mhz	Clock frequency data transfer mode CL <= 30pF
fOD	0	400	kHz	Clock frequency identification mode
tWH	10		ns	CL <= 30pF
tWL	10		ns	CL <= 30pF
tTLH		10	ns	CL <= 30pF
tTHL		10	ns	CL <= 30pF
2.7V~3.6V VCCQ				
tISU	3		ns	CL <= 30pF
tIH	3		ns	CL <= 30pF
tOSU	11.7		ns	CL <= 30pF
tOH	8.3		ns	CL <= 30pF
1.70V~1.95V VCCQ				
tISU	3		ns	CL <= 30pF
tIH	3		ns	CL <= 30pF
tOSU	11.7		ns	CL <= 30pF
tOH	8.3		ns	CL <= 30pF

Table 16-Backward Compatible Device Interface Timing

7.4 Bus Timing in HS200 Mode

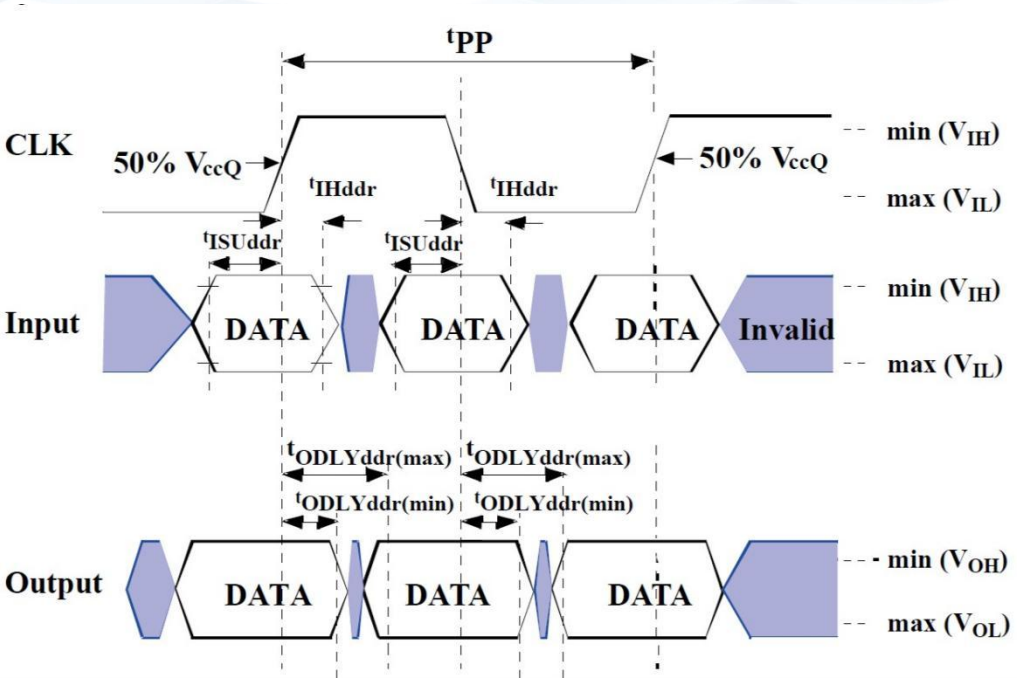


Figure 8 Bus Timing in Dual Data Rate Mode

Symbol	Min	Max	Unit	Remark
Input CLK				
DC	45	55	%	Clock Duty Cycle Include jitter, phase noise
tTLH		3	ns	CL <= 30pF
tTHL		3	ns	CL <= 30pF
Input CMD (referenced to CLK-SDR mode)				
tISUddr	3		ns	CL <= 20pF
tIHddr	3		ns	CL <= 20pF
Output CMD (referenced to CLK-SDR mode)				
tODLY		13.7	ns	CL <= 20pF
tOH	2.5		ns	CL <= 20pF
tRISE		3	ns	CL <= 20pF
tFALL		3	ns	CL <= 20pF

Input DAT (referenced t CLK-DDR mode)				
tISUddr	2.5		ns	CL <= 20pF
tIHddr	2.5		ns	CL <= 20pF
Output DAT (referenced t CLK-DDR mode)				
tODLYddr	1.5	7	ns	CL <= 20pF
tRISE		2	ns	CL <= 20pF
tFALL		2	ns	CL <= 20pF

Table 17-High-Speed Dual Data Rate Interface Timing

7.5 Bus Timing in HS200 Mode

■ HS200 Clock Timing

Host CLK Timing in HS200 mode shall conform to the timing specified in Figure 9 and Table 18. CLK input should satisfy the clock timing over all possible operation and environment conditions. CLK input parameters should be measured while CMD and DAT lines are stable high or low, as close as possible to the Device.

The maximum frequency of HS200 is 200Mhz. Hosts can use any frequency up to the maximum that HS200 allows.

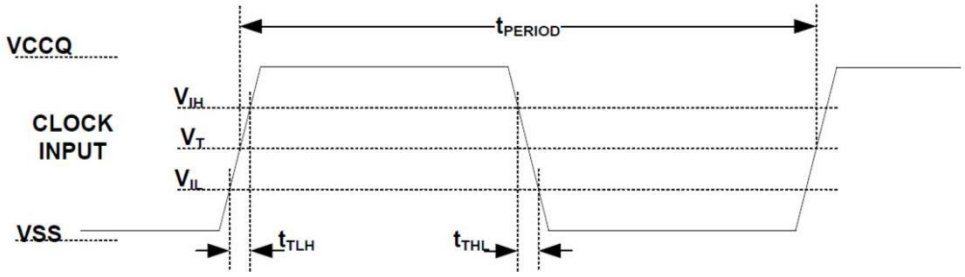


Figure 9-HS200 Clock Signal Timing

Notes:

1. V_{IH} denote V_{IH}(min.) and V_{IL} denotes V_{IL}(max.).
2. V_T=0.975V – Clock Threshold (VCCQ = 1.8V), indicates clock reference point for timing measurements.

Symbol	Min	Max	Unit	Remark
tPERIOD	5	-	ns	200MHz(max), between rising edges
tTLH, tTHL	-	0.2-tPERIOD	ns	tTLH, tTHL < 1ns(max) at 200MHz, CDEVICE = 6pF. The absolute maximum value of tTLH, tTHL is

				10ns regardless of clock frequency.
Duty Cycle	30	70	%	

Table 18-HS200 Clock Signal Timing

■ HS200 Device Input Timing

Figure 10 and Table 19 define Device input timing.

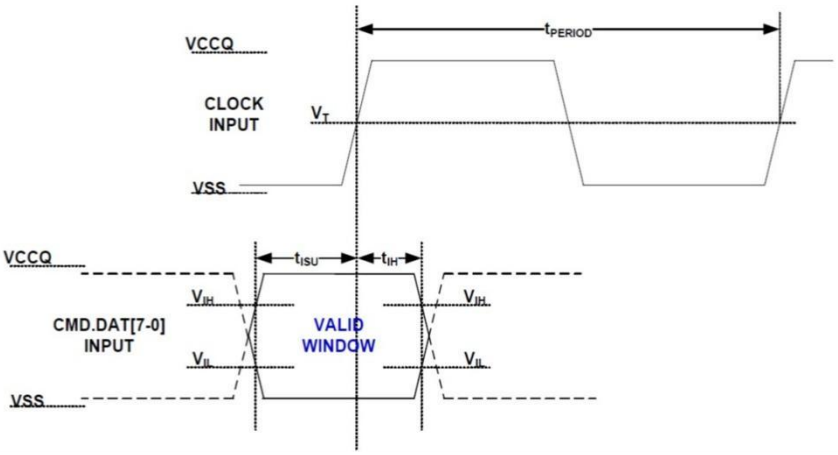


Figure 10-HS200 Device Input Timing

Notes:

1. tISU and tIH are measured at VIL(max) and VIH(min).
2. VIH denotes VIH(min) and VIL denotes VIL(max).

Symbol	Min	Max	Unit	Remark
tISU	1.40	-	ns	CDEVICE <= 6pF
tIH	0.8	-	ns	CDEVICE <= 6pF

Table 19-HS200 Device Input Timing

■ HS200 Device Output Timing

tPH parameter is defined to allow device output delay to be longer than tPERIOD. After initialization the tPH may have random phase relation to the clock. The Host is responsible to find the optimal sampling point for the Device outputs, while switching to the HS200 mode. Figure 11 and Table 20 define Device output timing.

While setting the sampling point of data, a long term drift, which mainly depends on temperature drift, should be considered. The temperature drift is expressed by ΔTPH. Output valid data window (tVW) is available regardless of the drift (ΔTPH) but position of data window varies by the drift, as describes in Figure 11.

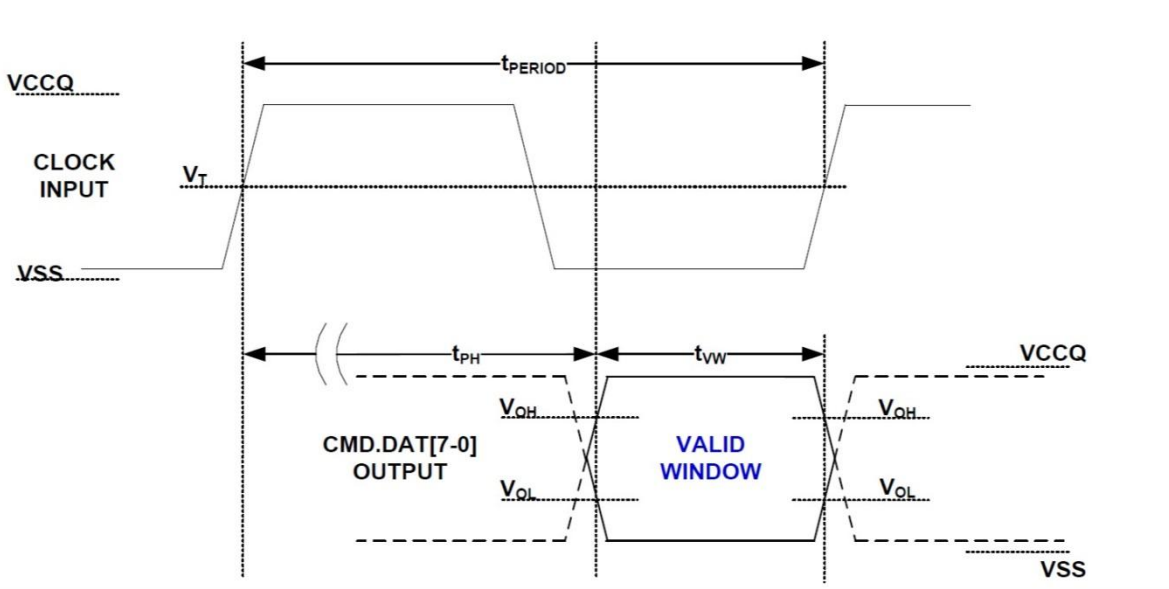


Figure 11-HS200 Device Output Timing

Notes: V_{OH} denotes V_{OH}(min) and V_{OL} denotes V_{OL}(max).

Symbol	Min	Max	Unit	Remark
tPH	0	2	UI	Device output momentary phase from CLK input to CMD or DAT lines output. Does not include a long term temperature drift.
ΔTPH	-350 (ΔT=-20℃)	+1550 (ΔT=90℃)	ps	Delay variation due to temperature change after tuning. Total allowable shift of output valid window (tVW) from last system Tuning procedure. ΔTPH is 2600ps for ΔT from -25℃to 125℃ druing operation.
tVW	0.575	-	UI	tVW = 2.88ns at 200MHz. Host path may add Signal Integrity included noise, skews, etc. Expected tVW at Host input is larger than 0.475UI.

Table 20-HS200 Device Output Timing

Notes: Unit Interval (UI) is one bit nominal time. For example, UI=5ns at 200MHz.

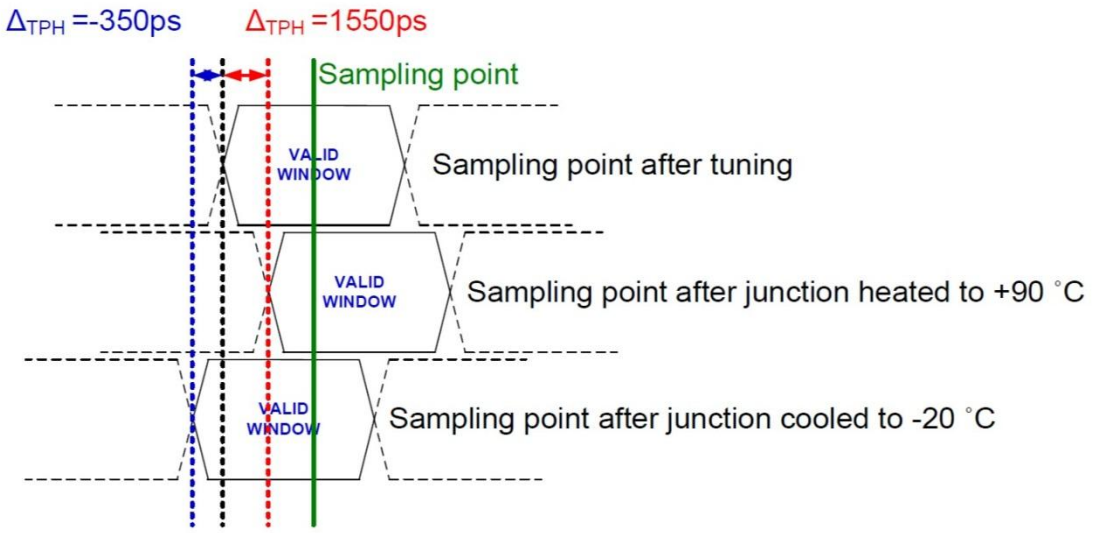


Figure 12-t_{PH} Consideration

7.6 Bus Timing in HS400 Mode

■ HS400 Device Input Timing

The CMD input timing for HS400 mode is the same as CMD input timing for HS200 mode. Figure 13 and Table 21 define Device input timing.

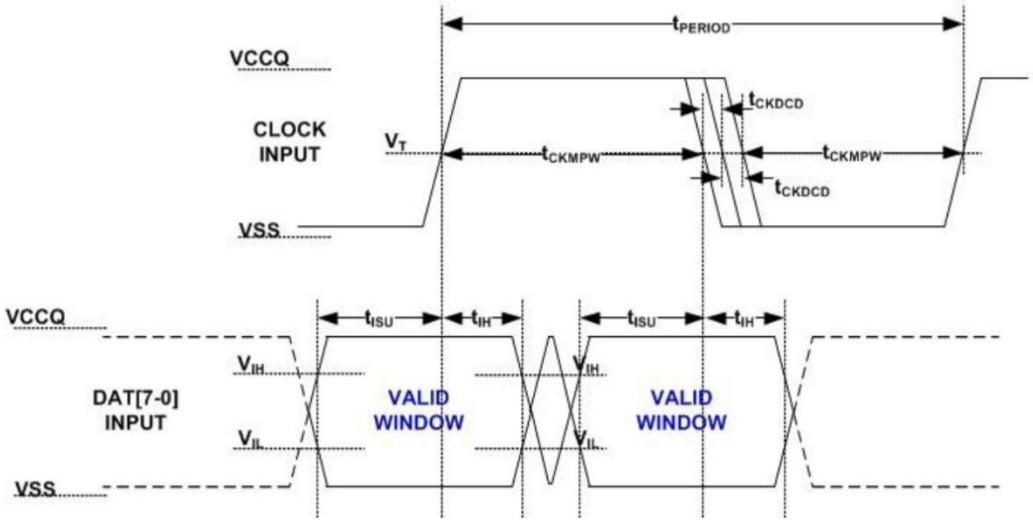


Figure 13-HS400 Device Data Input Timing

Symbol	Min	Max	Unit	Remark
tPERIOD	5	-	ns	200MHz(max), between rising edges. With respect to VT

SR	1.125		V/ns	Slew rate for input CLK/DAT. With respect to VIH/VIL
tCKDCD	0	0.3	ns	Duty cycle distortion. Allowable deviation from an ideal 50% duty cycle. With respect to VT Includes jitter, phase noise
tCKMPW	2.2		ns	Minimum pulse width With respect to VT
tISUddr	0.4		ns	CDEVICE <= 6pF With respect to VIH/VIL
tIHddr	0.4	-	ns	CDEVICE <= 6pF With respect to VIH/VIL

Table 21-HS400 Device Input Timing

■ HS400 Device Output Timing

The Data Strobe is used to read data in HS400 mode. The Data Strobe is toggled only during data read or CRC status response.

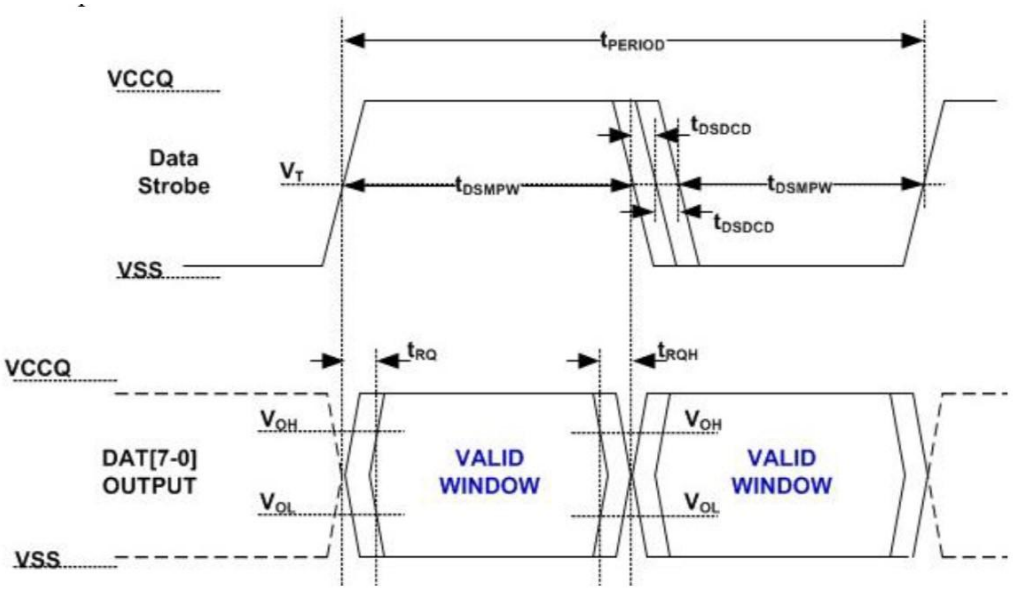


Figure 14-HS400 Device Output Timing

Symbol	Min	Max	Unit	Remark
tPERIOD	5		ns	200MHz(max), between rising edges. With respect to VT
SR	1.125		V/ns	Slew rate for Data Strobe and Output Data. With respect to VOH/VOL HS400 reference load

tDSDCD	0	0.2	ns	Data Strobe Duty cycle distortion. Allowable deviation from the input CLK duty cycle distortion (tCKDCD) With respect to VT Includes jitter, phase noise
tDSMPW	2.0		ns	Data Strobe minimum pulse width With respect to VT
tRPRE	0.4		tPERIOD	Data Strobe Read pre-amble Max value up to infinite is valid
tRPST	0.4		tPERIOD	Data Strobe Read post-amble Max value up to infinite is valid
tRQ		0.4	ns	With respect to VOH/VOL HS400 reference load
tRQH		0.4	ns	With respect to VOH/VOL HS400 reference load

Table 22-HS400 Device Output Timing

Parameter	Symbol	Min	Max	Unit
Pull-up resistance for CMD	RCMD	4.7	100	Kohm
Pull-up resistance for DAT0-7	RDAT	10	100	Kohm
Pull-down resistance for DS	RDS	10	100	Kohm
Internal pull up resistance for DAT1-DAT7	Rint	10	150	Kohm
Bus signal line capacitance	CL		13	pF
Single Device capacitance	CDevice		6	pF

Table 23-HS400 Capacitor

8. Connection Guide

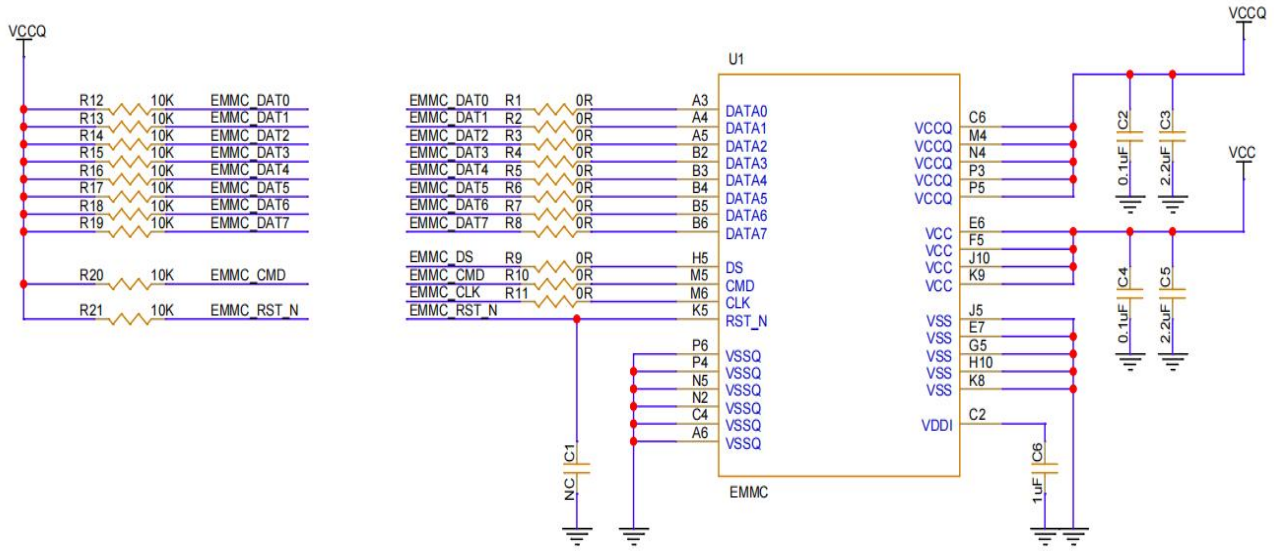
8.1 Schematic Diagram

Coupling capacitor should be connected with VCC/VCCQ and VSS as closely as possible.

The resistance on the CLK line is highly recommended (0Ω by default).0Ω~100Ω is also available.

SCY recommends to separate VCC and VCCQ power.VDDi Capacitor is min 0.1uF.

SCY recommends lay the VSS between the CLK and the Data lines.



The resistance on the CLK line is highly recommended (0Ω by default)