NSi8120/NSi8121/NSi8122

High Reliability Dual-Channel Digital Isolators

Datasheet (EN) 2.3

Product Overview

The NSi812x devices are high reliability dual-channel digital isolator. The NSi812x device is safety certified by UL1577 support several insulation withstand voltages (3.75kV$_{rms}$, 5kV$_{rms}$), while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the NSi812x is up to 150Mbps, and the common-mode transient immunity (CMTI) is up to 150kV/us. The NSi812x device provides digital channel direction configuration and the default output level configuration when the input power is lost. Wide supply voltage of the NSi812x device support to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use. AEC-Q100 (Grade 1) option is provided for all devices.

Key Features

- Up to 5000V$_{rms}$ Insulation voltage
- Date rate: DC to 150Mbps
- Power supply voltage: 2.5V to 5.5V
- All devices are AEC-Q100 qualified
- High CMTI: 150kV/us
- Chip level ESD: HBM: ±6kV
- High system level EMC performance:
  - Enhanced system level ESD, EFT, Surge immunity
- Default output high level or low level option
- Isolation barrier life: >60 years
- Low power consumption: 1.5mA/ch (1 Mbps)
- Low propagation delay: <15ns
- Operation temperature: -40℃~125℃
- RoHS-compliant packages:
  - SOP8 narrow body
  - SOW16 wide body

Safety Regulatory Approvals

- UL recognition: up to 5000V$_{rms}$ for 1 minute per UL1577
- CQC certification per GB4943.1-2011
- CSA component notice 5A
- DIN VDE V 0884-11:2017-01 F

Applications

- Industrial automation system
- Isolated SPI, RS232, RS485
- General-purpose multichannel isolation
- Motor control

Device Information

Part Number	*Package*	*Body Size*
NSI812xNx	SOP8	4.90mm ×3.90mm
NSI812xWx	SOW16	10.30mm × 7.50mm

Functional Block Diagrams

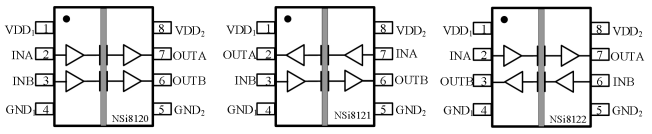


Figure 1. NSi812xN Block Diagram

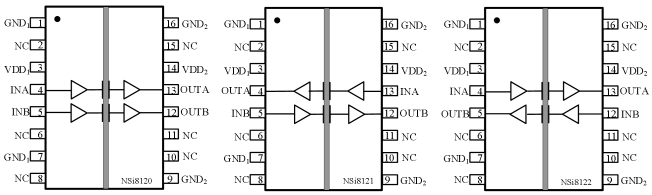


Figure 2. NSi812xW Block Diagram

INDEX

1. Pin Configuration And Functions

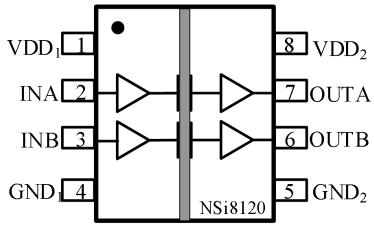


Figure 1.1 NSi8120N Package

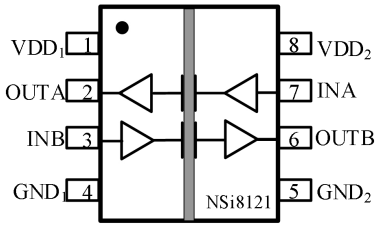


Figure 1.2 NSi8121N Package

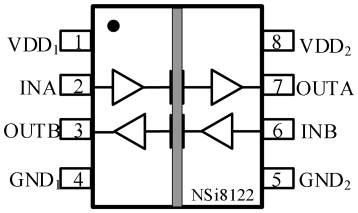


Figure 1.3 NSi8122N Package

Table1.1 NSi8120N/ NSi8121N/ NSi8122N Pin Configuration and Description

NSi8120N PIN NO.	*NSi8121N PIN NO.*	*NSi8122N PIN NO.*	*SYMBOL*	*FUNCTION*
1	1	1	VDD1	Power Supply for Isolator Side 1
2	7	2	INA	Logic Input A
3	3	6	INB	Logic Input B
4	4	4	GND1	Ground 1, the ground reference for Isolator Side 1
5	5	5	GND2	Ground 2, the ground reference for Isolator Side 2
6	6	3	OUTB	Logic Output B
7	2	7	OUTA	Logic Output A
8	8	8	VDD2	Power Supply for Isolator Side 2

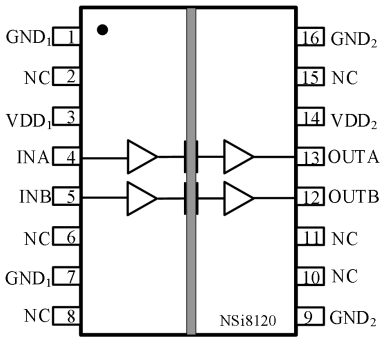


Figure 1.4 NSi8120W Package

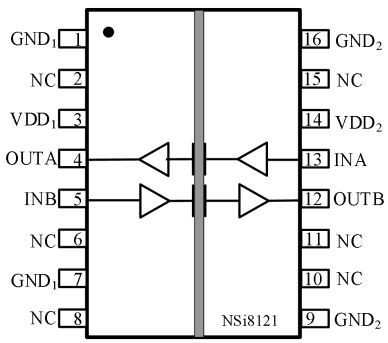


Figure 1.5 NSi8121W Package

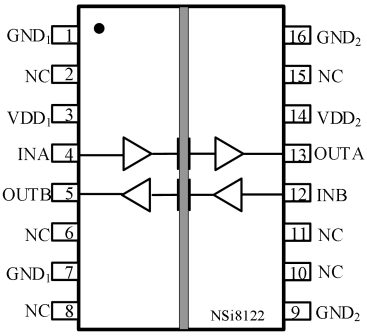


Figure 1.6 NSi8122W Package

Table 1.2 NSi8120W/ NSi8121W/ NSi8122W Pin Configuration and Description

NSi8120W PIN NO.	*NSi8121W PIN NO.*	*NSi8122W PIN NO.*	*SYMBOL*	*FUNCTION*
1	1	1	GND1	Ground 1, the ground reference for Isolator Side 1
2	2	2	NC	No Connection.
3	3	3	VDD1	Power Supply for Isolator Side 1
4	13	4	INA	Logic Input A
5	5	12	INB	Logic Input B

6	6	6	NC	No Connection.
7	7	7	GND1	Ground 1, the ground reference for Isolator Side 1
8	8	8	NC	No Connection.
9	9	9	GND2	Ground 2, the ground reference for Isolator Side 2
10	10	10	NC	No Connection.
11	11	11	NC	No Connection.
12	12	5	OUTB	Logic Output A
13	4	13	OUTA	Logic Output B
14	14	14	VDD2	Power Supply for Isolator Side 2
15	15	15	NC	No Connection.
16	16	16	GND2	Ground 2, the ground reference for Isolator Side 2

2. Absolute Maximum Ratings

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Power Supply Voltage	VDD1, VDD2	-0.5		6.5	V	
Maximum Input Voltage	VINA, VINB	-0.4		VDD+0.4[1]	V	
Maximum Output Voltage	V_{OUTA}, V_{OUTB}	-0.4		VDD+0.4[1]	V	
Maximum Input/Output Pulse Voltage	VINA, VINB, V_{OUTA}, V_{OUTB}	-0.8		VDD+0.8	V	Pulse width should be less than 100ns, and the duty cycle should be less than 10%
Output current	Io	-15		15	mA	
Maximum Surge Isolation Voltage	V_{IOSM}			5.3	kV	
Operating Temperature	Topr	-40		125	℃	
Junction temperature	Tj	-40		150	℃	
Storage Temperature	Tstg	-65		150	℃	
Electrostatic discharge	HBM			±6000	V	
	CDM			±2000	V	

[1] The maximum voltage must not exceed 6.5V.

3. Recommended Operating Conditions

Parameters	*Symbol*	*min*	*typ*	*max*	*unit*
Power Supply Voltage	VDD1, VDD2	2.5		5.5	V

Operating Temperature	Topr	-40		125	℃
High Level Input Voltage	VIH	2			V
Low Level Input Voltage	VIL			0.8	V
Data rate	DR			150	Mbps

4. Thermal Characteristics

Parameters	*Symbol*	*SOW16*	*SOP8*	*Unit*
IC Junction-to-Air Thermal Resistance	θ_{JA}	86.5	137.7	℃/W
Junction-to-case (top) thermal resistance	$\theta_{JC(top)}$	49.6	54.9	℃/W
Junction-to-board thermal resistance	θ_{JB}	49.7	71.7	℃/W

5. Specifications

5.1. Electrical Characteristics

(VDD1=2.5V~5.5V, VDD2=2.5V~5.5V, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Power on Reset	VDD_{POR}		2.2		V	POR threshold as during power-up
	VDD_{HYS}		0.1		V	POR threshold Hysteresis
Input Threshold	V_{IT}		1.6		V	Input Threshold at rising edge
	V_{IT_HYS}		0.4		V	Input Threshold Hysteresis
High Level Input Voltage	V_{IH}	2			V	
Low Level Input Voltage	V_{IL}			0.8	V	
High Level Output Voltage	V_{OH}	VDD-0.3			V	$I_{OH} \le 4mA$
Low Level Output Voltage	V_{OL}			0.3	V	$I_{OL} \le 4mA$
Output Impedance	R_{out}		50		ohm	
Input Pull high or low Current	I_{pull}		8	15	uA	
Start Up Time after POR	trbs		40		usec	
Common Mode Transient Immunity	CMTI	±100	±150		kV/us	

(VDD1=5V± 10%, VDD2=5V± 10%, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Supply current	**NSi8120**					

	I_{DD1}(Q0)		0.58	0.87	mA	All Input 0V for NSi8120x0 Or All Input at supply for NSi8120x1
	I_{DD2}(Q0)		1.18	1.77	mA	
	I_{DD1}(Q1)		2.92	4.38	mA	All Input at supply for NSi8120x0 Or All Input 0V for NSi8120x1
	I_{DD2}(Q1)		1.24	1.86	mA	
	I_{DD1}(1M)		1.71	2.56	mA	All Input with 1Mbps, C_L=15pF
	I_{DD2}(1M)		1.38	2.07	mA	
	I_{DD1}(10M)		1.78	2.67	mA	All Input with 10Mbps, C_L=15pF
	I_{DD2}(10M)		3.2	4.8	mA	
	I_{DD1}(100M)		2.10	3.15	mA	All Input with 100Mbps, C_L=15pF
	I_{DD2}(100M)		21.0	31.5	mA	
	NSi8121/ NSi8122					
	I_{DD1}(Q0)		1.03	1.55	mA	All Input 0V for NSi812xx0 Or All Input at supply for NSi812xx1
	I_{DD2}(Q0)		1.00	1.5	mA	
	I_{DD1}(Q1)		2.20	3.3	mA	All Input at supply for NSi812xx0 Or All Input 0V for NSi812xx1
	I_{DD2}(Q1)		2.13	3.2	mA	
	I_{DD1}(1M)		1.72	2.58	mA	All Input with 1Mbps, C_L=15pF
	I_{DD2}(1M)		1.68	2.52	mA	
	I_{DD1}(10M)		2.62	3.93	mA	All Input with 10Mbps, C_L=15pF
	I_{DD2}(10M)		2.71	4.06	mA	
	I_{DD1}(100M)		11.01	16.5	mA	All Input with 100Mbps, C_L = 15pF
	I_{DD2}(100M)		12.8	19.2	mA	
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	t_{PLH}	5	8.20	15	ns	See Figure 2.7 , C_L = 15pF
	t_{PHL}	5	10.56	15	ns	See Figure 2.7, C_L = 15pF
Pulse Width Distortion $\lvert t_{PHL} - t_{PLH} \rvert$	PWD			5.0	ns	See Figure 2.7 , C_L = 15pF
Rising Time	t_r			5.0	ns	See Figure 2.7 , C_L = 15pF
Falling Time	t_f			5.0	ns	See Figure 2.7 , C_L = 15pF
Peak Eye Diagram Jitter	t_{JIT}(PK)		350		ps	
Channel-to-Channel Delay Skew	t_{SK}(c2c)			2.5	ns	
Part-to-Part Delay Skew	t_{SK}(p2p)			5.0	ns	

(VDD1=3.3V± 10%, VDD2=3.3V± 10%, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at VDD1 = 3.3V, VDD2 = 3.3V, Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Supply current	**NSi8120**					
	I_{DD1}(Q0)		0.55	0.83	mA	All Input 0V for NSi8120x0 Or All Input at supply for NSi8120x1
	I_{DD2}(Q0)		1.12	1.68	mA	
	I_{DD1}(Q1)		2.87	4.3	mA	All Input at supply for NSi8120x0 Or All Input 0V for NSi8120x1
	I_{DD2}(Q1)		1.18	1.77	mA	
	I_{DD1}(1M)		1.7	2.55	mA	All Input with 1Mbps, C_L = 15pF
	I_{DD2}(1M)		1.27	1.91	mA	
	I_{DD1}(10M)		1.73	2.6	mA	All Input with 10Mbps, C_L = 15pF
	I_{DD2}(10M)		2.41	3.6	mA	
	I_{DD1}(100M)		2.05	3.08	mA	All Input with 100Mbps, C_L = 15pF
	I_{DD2}(100M)		14.05	21.08	mA	
	NSi8121/ NSi8122					
	I_{DD1}(Q0)		0.98	1.47	mA	All Input 0V for NSi812xx0 Or All Input at supply for NSi812xx1
	I_{DD2}(Q0)		0.95	1.43	mA	
	I_{DD1}(Q1)		2.14	3.21	mA	All Input at supply for NSi812xx0 Or All Input 0V for NSi812xx1
	I_{DD2}(Q1)		2.08	3.12	mA	
	I_{DD1}(1M)		1.63	2.45	mA	All Input with 1Mbps, C_L = 15pF
	I_{DD2}(1M)		1.59	2.39	mA	
	I_{DD1}(10M)		2.22	3.33	mA	All Input with 10Mbps, C_L = 15pF
	I_{DD2}(10M)		2.25	3.38	mA	
	I_{DD1}(100M)		7.57	11.36	mA	All Input with 100Mbps, C_L = 15pF
	I_{DD2}(100M)		8.5	12.75	mA	
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	t_{PLH}	5	9.20	15	ns	See Figure 2.7 , C_L = 15pF
	t_{PHL}	5	10.40	15	ns	See Figure 2.7, C_L = 15pF
Pulse Width Distortion $\lvert t_{PHL} - t_{PLH} \rvert$	PWD			5.0	ns	See Figure 2.7 , C_L = 15pF
Rising Time	t_r			5.0	ns	See Figure 2.7 , C_L = 15pF

Falling Time	t_f			5.0	ns	See Figure 2.7 , C_L = 15pF
Peak Eye Diagram Jitter	t_{JIT}(PK)		350		ps	
Channel-to-Channel Delay Skew	t_{SK}(c2c)			2.5	ns	
Part-to-Part Delay Skew	t_{SK}(p2p)			5.0	ns	

(VDD1=2.5V± 10%, VDD2=2.5V± 10%, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at VDD1 = 2.5V, VDD2 = 2.5V, Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Supply current	**NSi8120**					
	I_{DD1}(Q0)		0.53	0.8	mA	All Input 0V for NSi8120x0 Or All Input at supply for NSi8120x1
	I_{DD2}(Q0)		1.1	1.65	mA	
	I_{DD1}(Q1)		2.85	4.28	mA	All Input at supply for NSi8120x0 Or All Input 0V for NSi8120x1
	I_{DD2}(Q1)		1.15	1.73	mA	
	I_{DD1}(1M)		1.63	2.45	mA	All Input with 1Mbps, C_L = 15pF
	I_{DD2}(1M)		1.21	1.82	mA	
	I_{DD1}(10M)		1.68	2.52	mA	All Input with 10Mbps, C_L = 15pF
	I_{DD2}(10M)		2.05	3.08	mA	
	I_{DD1}(100M)		1.95	2.93	mA	All Input with 100Mbps, C_L = 15pF
	I_{DD2}(100M)		10.4	15.6	mA	
	NSi8121/ NSi8122					
	I_{DD1}(Q0)		0.96	1.44	mA	All Input 0V for NSi812xx0 Or All Input at supply for NSi812xx1
	I_{DD2}(Q0)		0.93	1.395	mA	
	I_{DD1}(Q1)		2.11	3.165	mA	All Input at supply for NSi812xx0 Or All Input 0V for NSi812xx1
	I_{DD2}(Q1)		2.05	3.075	mA	
	I_{DD1}(1M)		1.58	2.37	mA	All Input with 1Mbps, C_L = 15pF
	I_{DD2}(1M)		1.54	2.31	mA	
	I_{DD1}(10M)		2.02	3.03	mA	All Input with 10Mbps, C_L = 15pF
	I_{DD2}(10M)		2.04	3.06	mA	
	I_{DD1}(100M)		6.03	9.045	mA	All Input with 100Mbps, C_L = 15pF
	I_{DD2}(100M)		6	9	mA	
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	

Propagation Delay	t_{PLH}	5	10	15	ns	See Figure 2.7 , C_L = 15pF
	t_{PHL}	5	10	15	ns	See Figure 2.7, C_L = 15pF
Pulse Width Distortion $\lvert t_{PHL} - t_{PLH} \rvert$	PWD			5.0	ns	See Figure 2.7 , C_L = 15pF
Rising Time	t_r			5.0	ns	See Figure 2.7 , C_L = 15pF
Falling Time	t_f			5.0	ns	See Figure 2.7 , C_L = 15pF
Peak Eye Diagram Jitter	t_{JIT}(PK)		350		ps	
Channel-to-Channel Delay Skew	t_{SK}(c2c)			2.5	ns	
Part-to-Part Delay Skew	t_{SK}(p2p)			5.0	ns	

5.2. Typical Performance Characteristics

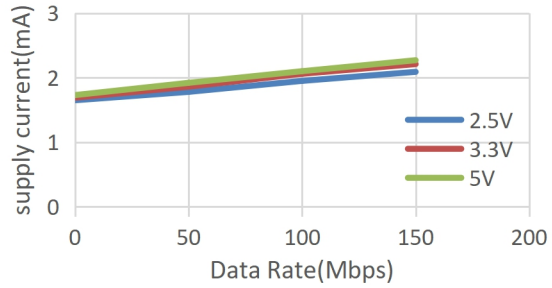


Figure 5.1 NSi8120 VDD1 Supply Current vs Data Rate

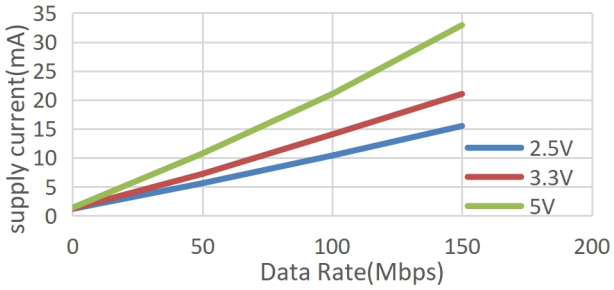


Figure 5.2 NSi8120 VDD2 Supply Current vs Data Rate

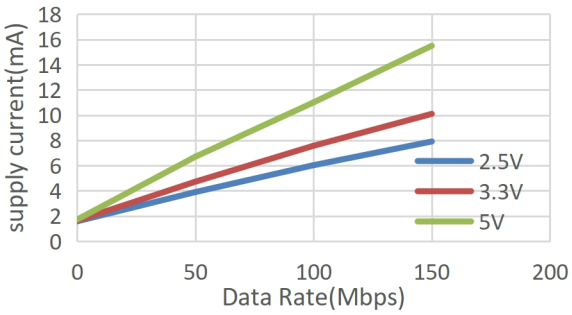


Figure 5.3 NSi8121/ NSi8122 VDD1 Supply Current vs Data Rate

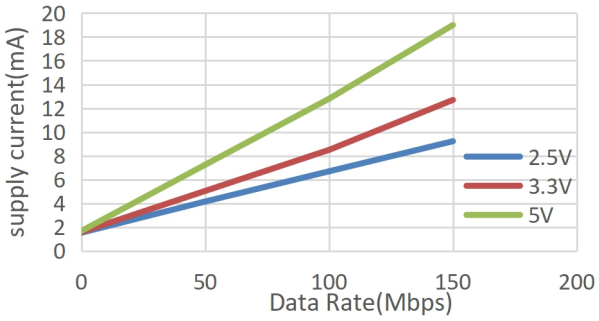
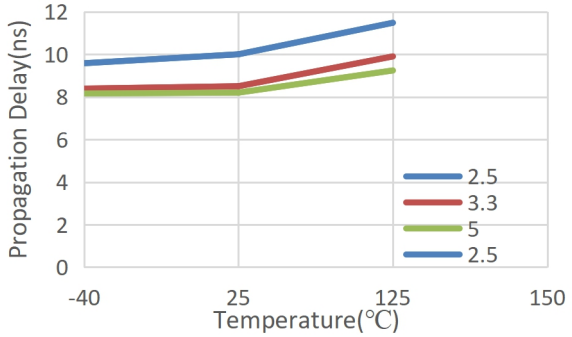


Figure 5.4 NSi8121/ NSi8122 VDD2 Supply Current vs Data Rate



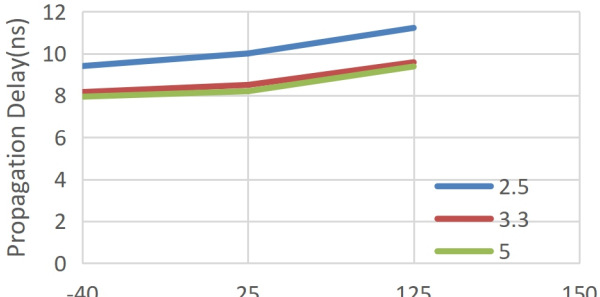


Figure 5.5 Rising Edge Propagation Delay Vs Temp

Figure 5.6 Falling Edge Propagation Delay Vs Temp

5.3. Parameter Measurement Information

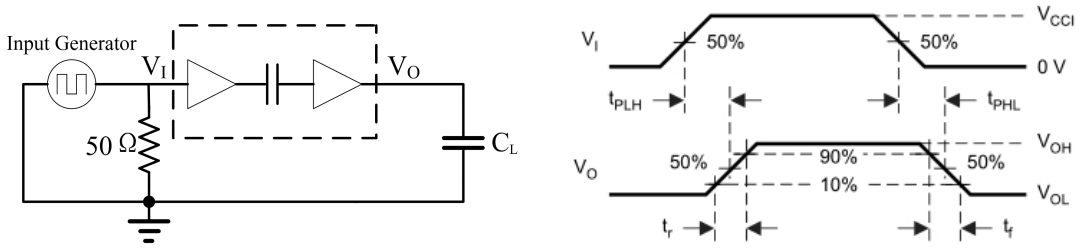


Figure 2.7 Switching Characteristics Test Circuit and Waveform

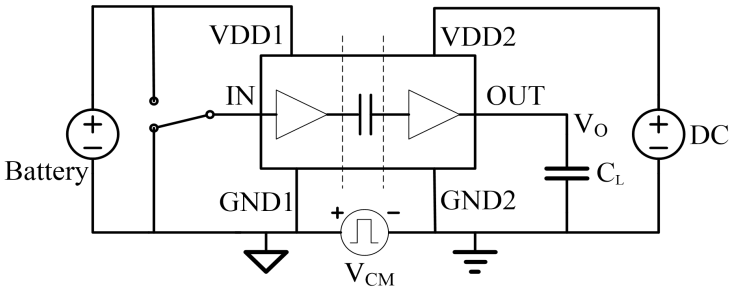


Figure 2.8 Common-Mode Transient Immunity Test Circuit

6. High Voltage Feature Description

6.1. Insulation And Safety Related Specifications

Parameters	*Symbol*	*Value*		*Unit*	*Comments*
		SOP8	*SOW16*		
Minimum External Air Gap (Clearance)	L(I01)	4.0	8.0	mm	Shortest terminal-to-terminal distance through air
Minimum External Tracking (Creepage)	L(I02)	4.0	8.0	mm	Shortest terminal-to-terminal distance across the package surface
Minimum internal gap	DTI	20		um	Distance through insulation
Tracking Resistance(Comparative Tracking Index)	CTI	>400		**V**	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		Ⅱ			

6.2. Din Vde V 0884-11（Vde V 0884-11）:2017-01 Insulation Charateristics

Description	*Test Condition*	*Symbol*	*Value*		*Unit*
			SOP8	SOW16	
Installation Classification per DIN VDE 0110					
For Rated Mains Voltage ≤ 150V_{rms}			Ⅰ to Ⅳ	Ⅰ to Ⅳ	
For Rated Mains Voltage ≤ 300V_{rms}			Ⅰ to Ⅲ	Ⅰ to Ⅳ	
For Rated Mains Voltage ≤ 400V_{rms}			Ⅰ to Ⅲ	Ⅰ to Ⅳ	
Climatic Classification			10/105/21	10/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	2	
Maximum repetitive isolation voltage		VIORM	565	1166	Vpeak
Input to Output Test Voltage, Method B1	V_{IORM} × 1.5 = $V_{pd(m)}$, 100% production test, t_{ini} = t_m = 1 sec, partial discharge < 5 pC	$V_{pd(m)}$	847	1749	Vpeak
Input to Output Test Voltage, Method A					
After Environmental Tests Subgroup 1	V_{IORM} × 1.2= $V_{pd(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd(m)}$	678	1399	Vpeak
After Input and /or Safety Test Subgroup 2 and Subgroup 3	V_{IORM} × 1.2= $V_{pd(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd(m)}$	678	1399	Vpeak
Maximum transient isolation voltage	t = 60 sec	VIOTM	5300	7000	Vpeak
Maximum Surge Isolation Voltage	Test method per IEC60065,1.2/50us waveform, VTEST=VIOSM×1.3	VIOSM	5384	5384	Vpeak
Isolation resistance	VIO =500V	RIO	>10^9	>10^9	Ω
Isolation capacitance	f = 1MHz	CIO	0.6	0.6	pF
Input capacitance		CI	2	2	pF
Total Power Dissipation at 25℃		Ps	1100	692	mW
Safety input, output, or supply current	θJA = 137.7 ℃/W, V I = 5.5 V, T J = 150 ℃, T A = 25 ℃	Is	200		mA
	θJA = 86.5 ℃/W, V I = 5.5 V, T J = 150 ℃, T A = 25 ℃			125.8	mA

Case Temperature		Ts	150	150	℃

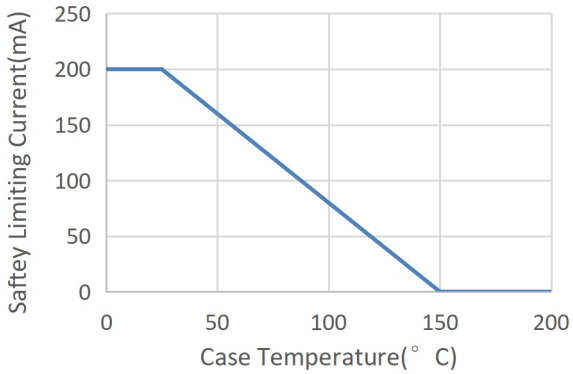


Figure 3.1 NSi8120N/NSi8121N/NSi8122N Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

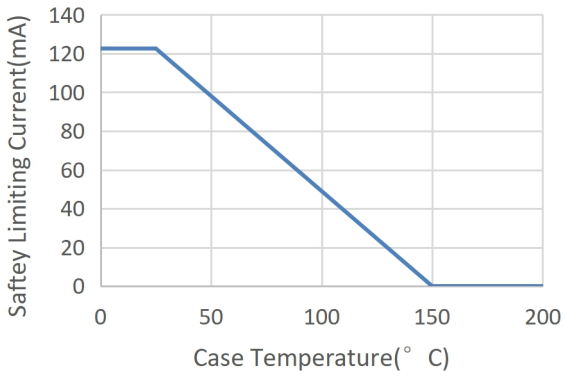


Figure 3.2 NSi8120W/NSi8121W/NSi8122W Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

6.3. Regulatory Information

The NSi8120N/NSi8121N/NSi8122N are approved by the organizations listed in table.

CUL		*VDE*	*CQC*
UL 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11:2017-01[2]	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 3750V_{rms} Isolation voltage	Single Protection, 3750V_{rms} Isolation voltage	Basic Insulation 565Vpeak, V_{IOSM}=5384Vpeak	Basic insulation at 400V_{rms} (565Vpeak)
File (E500602)	File (E500602)	File (5024579-4880-0001)	File (pending)

[1] In accordance with UL 1577, each NSi8120N/NSi8121N/NSi8122N is proof tested by applying an insulation test voltage ≥ 4500 V_{rms} for 1 sec.

[2] In accordance with DIN VDE V 0884-11, each NSi8120N/NSi8121N/NSi8122N is proof tested by applying an insulation test voltage ≥ 847 V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN VDE V 0884-11 approval.

The NSi8120W/NSi8121W/NSi8122W are approved by the organizations listed in table.

CUL	*VDE*	*CQC*

UL 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11(VDE V 0884-11):2017-01[2]	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 5000V_{rms} Isolation voltage	Single Protection, 5000V_{rms} Isolation voltage	Basic Insulation 1166Vpeak, V_{IOSM}=5384Vpeak	Basic insulation at 800V_{rms} (1131Vpeak) Reinforced insulation at 400V_{rms} (565Vpeak)
File (E500602)	File (E500602)	File (5024579-4880-0001)	File (pending)

[1] In accordance with UL 1577, each NSi8120W/NSi8121W/NSi8122W is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 sec.

[2] In accordance with DIN VDE V 0884-11, each NSi8120W/NSi8121W/NSi8122W is proof tested by applying an insulation test voltage ≥ 1749V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN VDE V 0884-11 approval.

7. Function Description

The NSi812x is a Dual-channel digital isolator based on a capacitive isolation barrier technique. The digital signal is modulated with RF carrier generated by the internal oscillator at the Transmitter side. Then it is transferred through the capacitive isolation barrier and demodulated at the Receiver side.

The NSi812x devices are high reliability dual-channel digital isolator with AEC-Q100 qualified. The NSi812x device is safety certified by UL1577 support several insulation withstand voltages (3.75kV_{rms}, 5kV_{rms}), while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the NSi812x is up to 150Mbps, and the common-mode transient immunity (CMTI) is up to 150kV/us. The NSi812x device provides digital channel direction configuration and the default output level configuration when the input power is lost. Wide supply voltage of the NSi812x device support to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use.

The NSi812x has a default output status when VDDIN is unready and VDDOUT is ready as shown in Table 4.1, which helps for diagnosis when power is missing at the transmitter side. The output B follows the same status with the input A within 60us after powering up.

Table 4.1 Output status vs. power status

Input	*VDD1 status*	*VDD2 status*	*Output*	*Comment*
H[1]	Ready	Ready	H	Normal operation.
L[2]	Ready	Ready	L	
X[3]	Unready	Ready	L H	The output follows the same status with the input within 60us after input side VDD1 is powered on.
X	Ready	Unready	X	The output follows the same status with the input within 60us after output side VDD2 is powered on.

[1] H=Logic high

[2] L=Logic low

[3] X=Logic low or logic high

8. Application Note

8.1. PCB Layout

The NSi812x requires a 0.1 µF bypass capacitor between VDD1 and GND1, VDD2 and GND2. The capacitor should be

placed as close as possible to the package. Figure 5.1 to Figure 5.4 show the recommended PCB layout, make sure the space under the chip should keep free from planes, traces, pads and via. To enhance the robustness of a design, the user may also include resistors (50–300 Ω) in series with the inputs and outputs if the system is excessively noisy. The series resistors also improve the system reliability such as latch-up immunity.

The typical output impedance of an isolator driver channel is approximately 50 Ω, ±40%. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

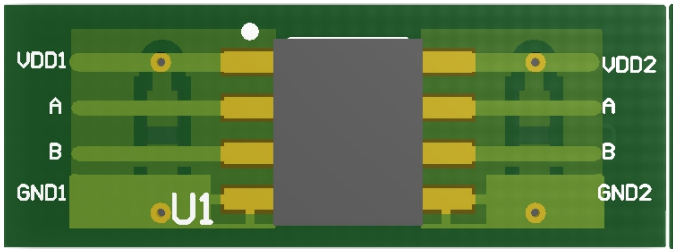


Figure5.1 Recommended PCB Layout — Top Layer

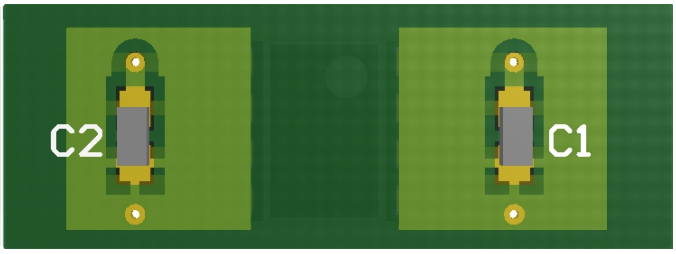


Figure5.2 Recommended PCB Layout — Bottom Layer

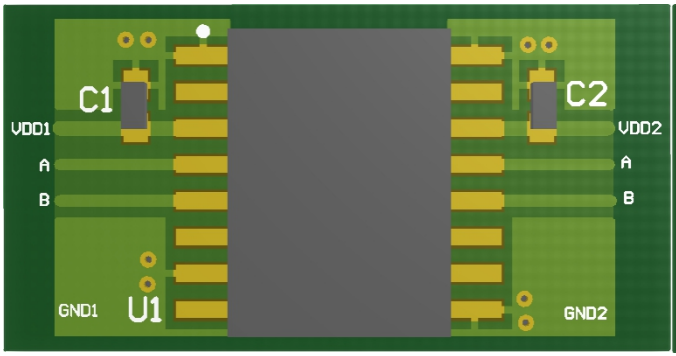


Figure5.3 Recommended PCB Layout — Top Layer

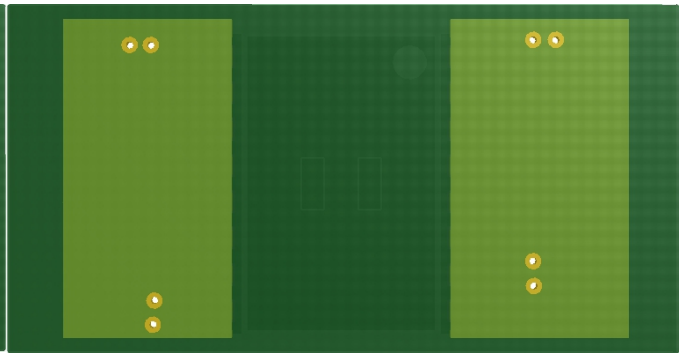


Figure5.4 Recommended PCB Layout — Bottom Layer

8.2. High Speed Performance

Figure 5.5 shows the eye diagram of NSi812x at 200Mbps data rate output. The result shows a typical measurement on the NSi812x with 350ps p-p jitter.

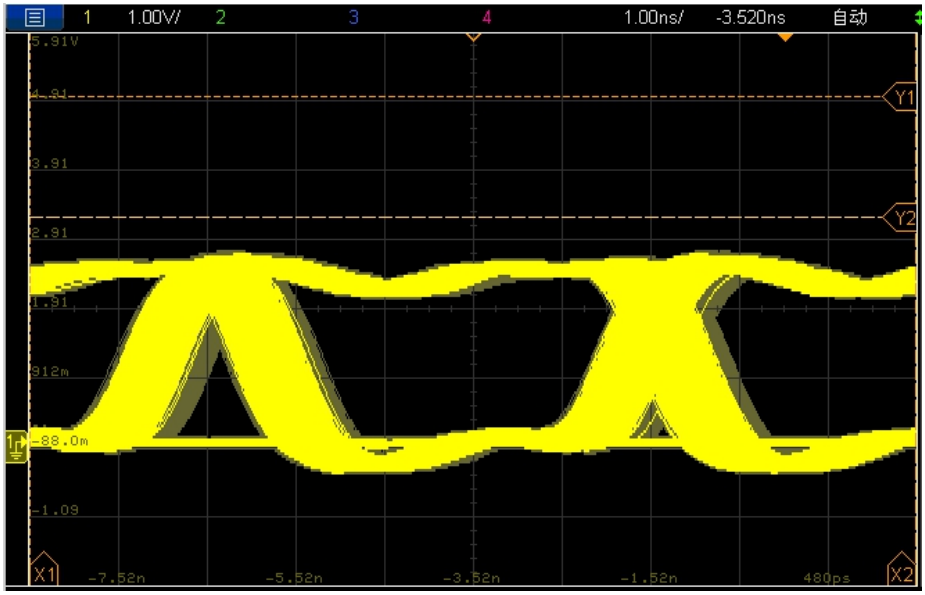


Figure5.5 NSi812x Eye Diagram

8.3. Typical Supply Current Equations

The typical supply current of NSi812x can be calculated using below equations. I_{DD1} and I_{DD2} are typical supply currents measured in mA, f is data rate measured in Mbps, C_L is the capacitive load measured in pF

NSi8120:

I_{DD1} = 0.19 *a1+1.45*b1+0.82*c1.

I_{DD2} = 1.36+ VDD1*f* C_L *c1*10^{-9}

When a1 is the channel number of low input at side 1, b1 is the channel number of high input at side 1, c1 is the channel number of switch signal input at side 1.

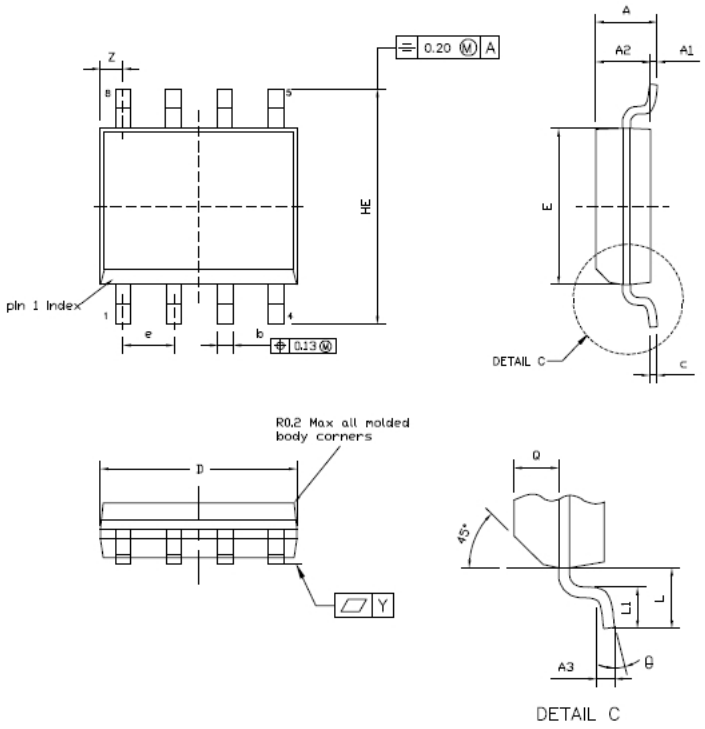
NSi8121/ NSi8122:

I_{DD1} = 0.87 +1.26*b1+0.63*c1+ VDD1*f* C_L *c2*10^{-9}

I_{DD2} = 0.87 +1.26*b2+0.63*c2+ VDD1*f* C_L *c1*10^{-9}

When b1 is the channel number of high input at side 1, c1 is the channel number of switch signal input at side 1, b2 is the channel number of high input at side 2, c2 is the channel number of switch signal input at side 2.

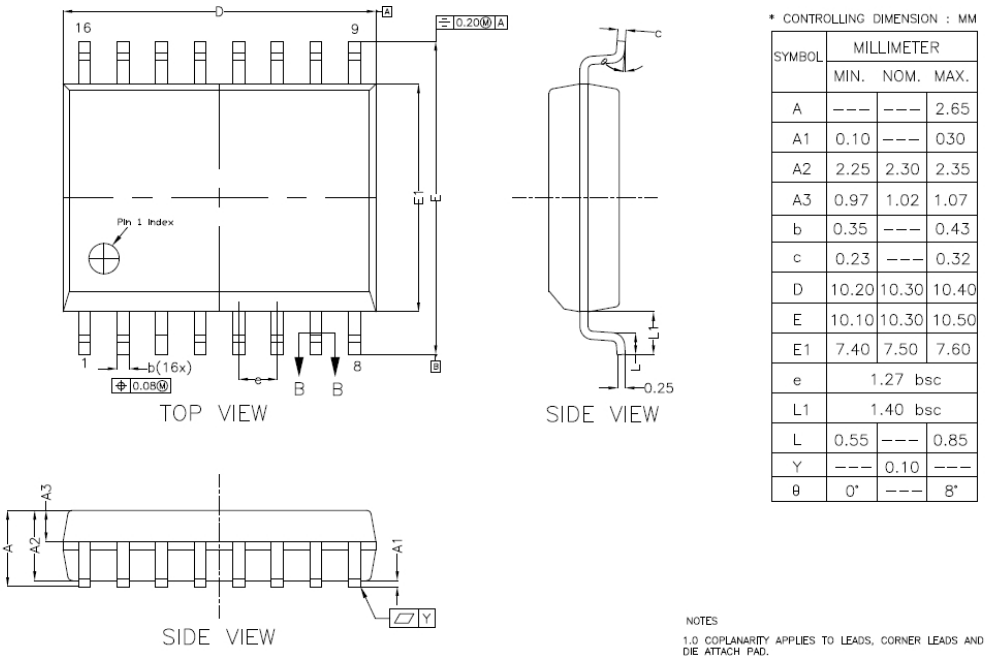
9. Package Information



* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	---	---	1.75
A1	0.10	---	0.25
A2	1.25	1.35	1.45
b	0.33	0.38	0.49
c	0.19	0.20	0.25
D	4.80	4.90	5.00
E	3.80	3.90	4.00
Q	0.60	0.65	0.70
HE	5.80	6.00	6.20
e	1.27 BSC		
L	1.05 BSC		
L1	0.40	0.64	1.00
Y	---	0.10	---
Z	0.3	0.5	0.7
A3	0.25 BSC		
θ	0°	5°	8°

Figure 9.1 SOP8 Package Shape and Dimension in millimeters (inches)

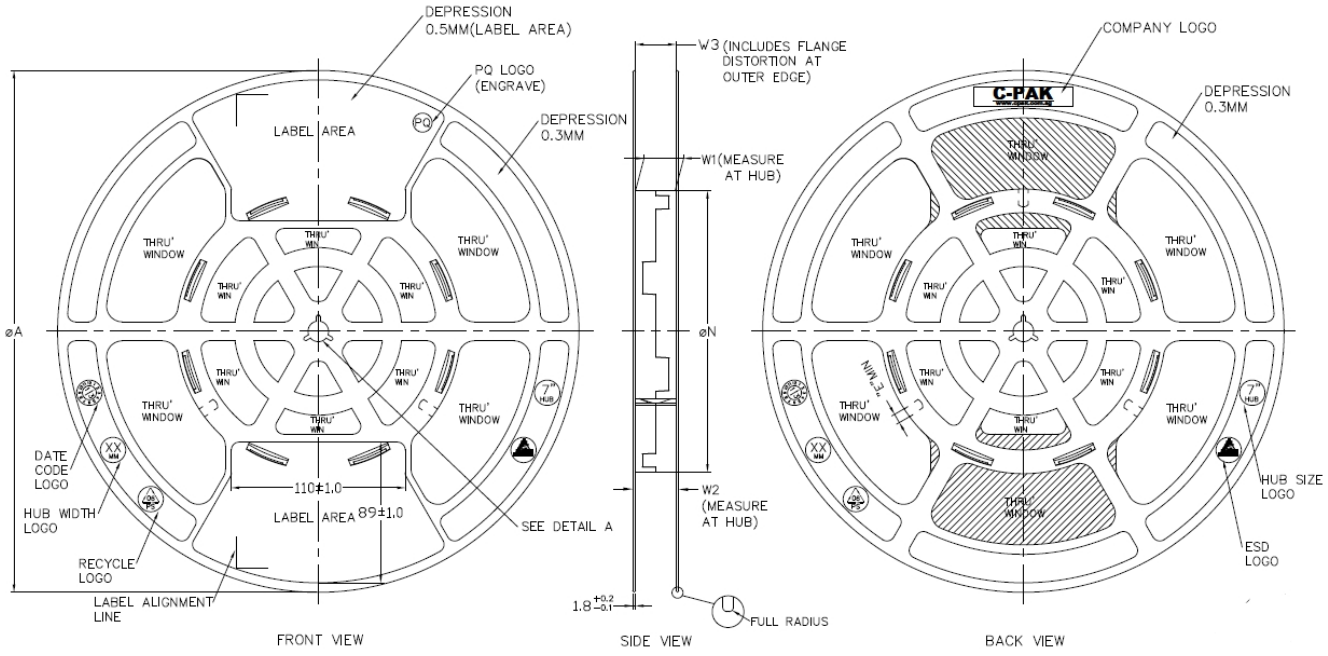


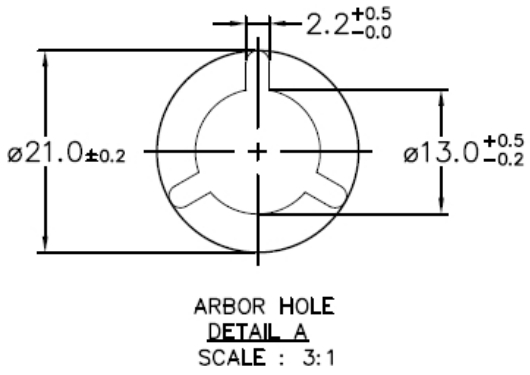
* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	---	---	2.65
A1	0.10	---	030
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.35	---	0.43
c	0.23	---	0.32
D	10.20	10.30	10.40
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27 bsc		
L1	1.40 bsc		
L	0.55	---	0.85
Y	---	0.10	---
θ	0°	---	8°

Figure 9.2 SOW16 Package Shape and Dimension in millimeters and (inches)

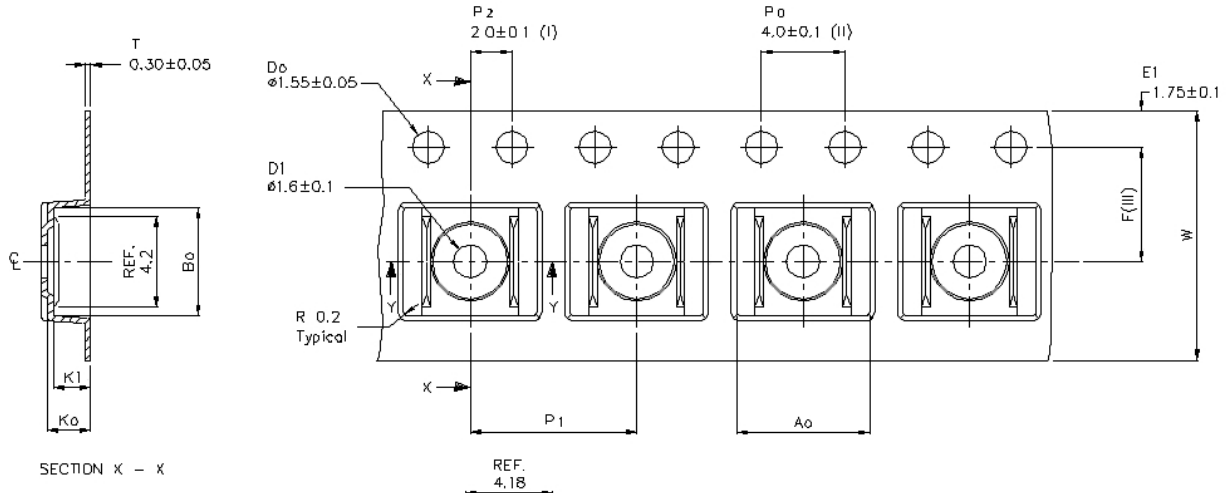
10. Tape and Reel Information

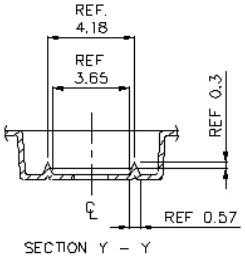




PRODUCT SPECIFICATION						
TAPE WIDTH	øA ±2.0	øN ±2.0	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	8.4 +1.5 −0.0	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4 +2.0 −0.0	18.4		5.5
16MM	330	178	16.4 +2.0 −0.0	22.4		5.5
24MM	330	178	24.4 +2.0 −0.0	30.4		5.5
32MM	330	178	32.4 +2.0 −0.0	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{6} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{5} & BELOW 10^{5}	CONDUCTIVE (GENERIC)	BLACK ONLY
E	10^{9} TO 10^{11}	ANTISTATIC (COATED)	ALL TYPES

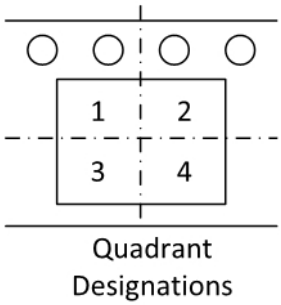




Ao	6.50 +/− 0.1
Bo	5.30 +/− 0.1
Ko	2.20 +/− 0.1
K1	1.90 +/− 0.1
F	5.50 +/− 0.1
P1	8.00 +/− 0.1
W	12.00 +/− 0.3

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED



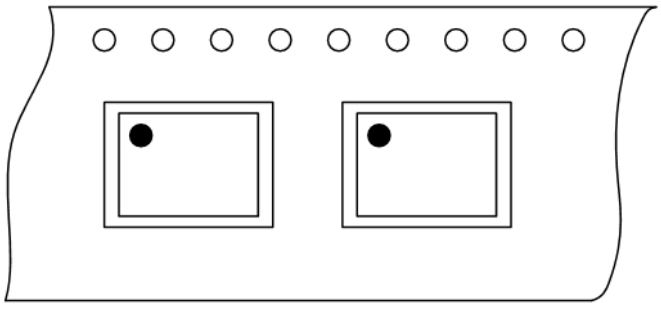
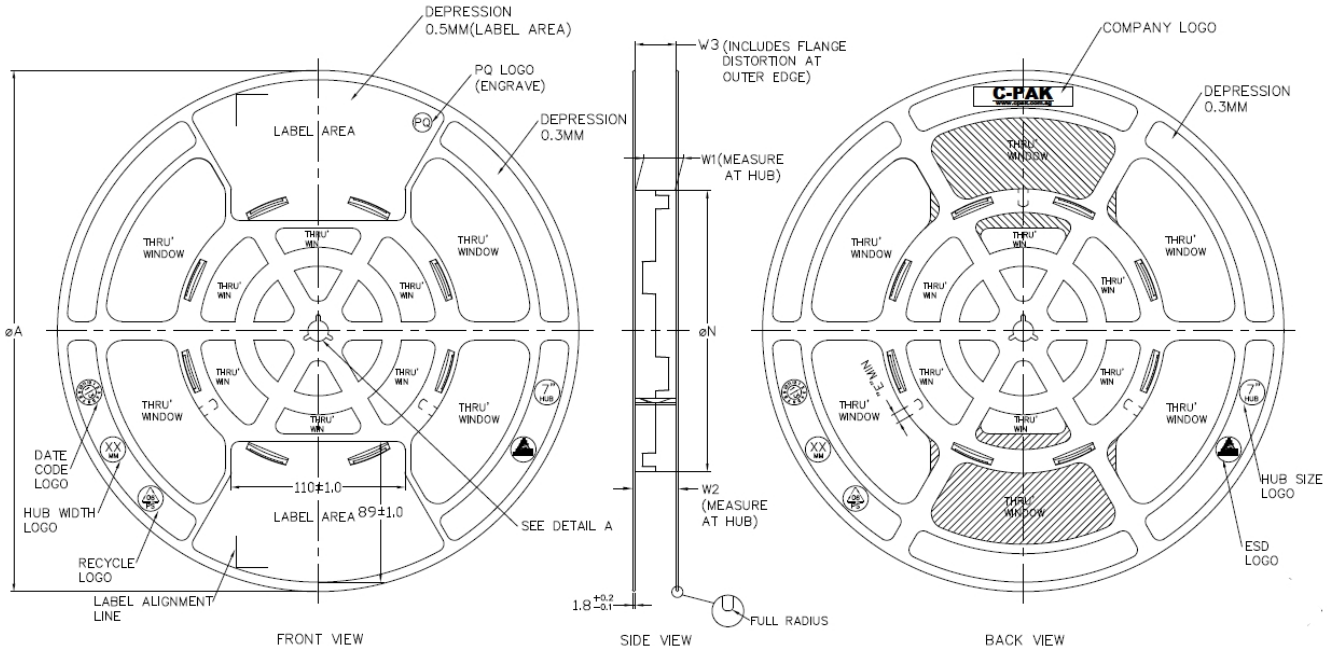
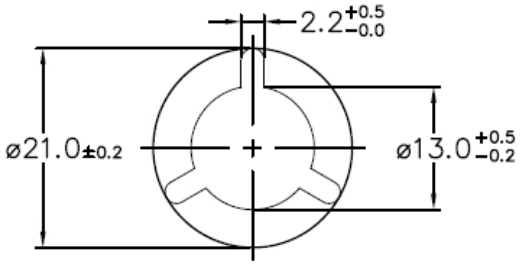


Figure 7.1 Tape and Reel Information of SOP8

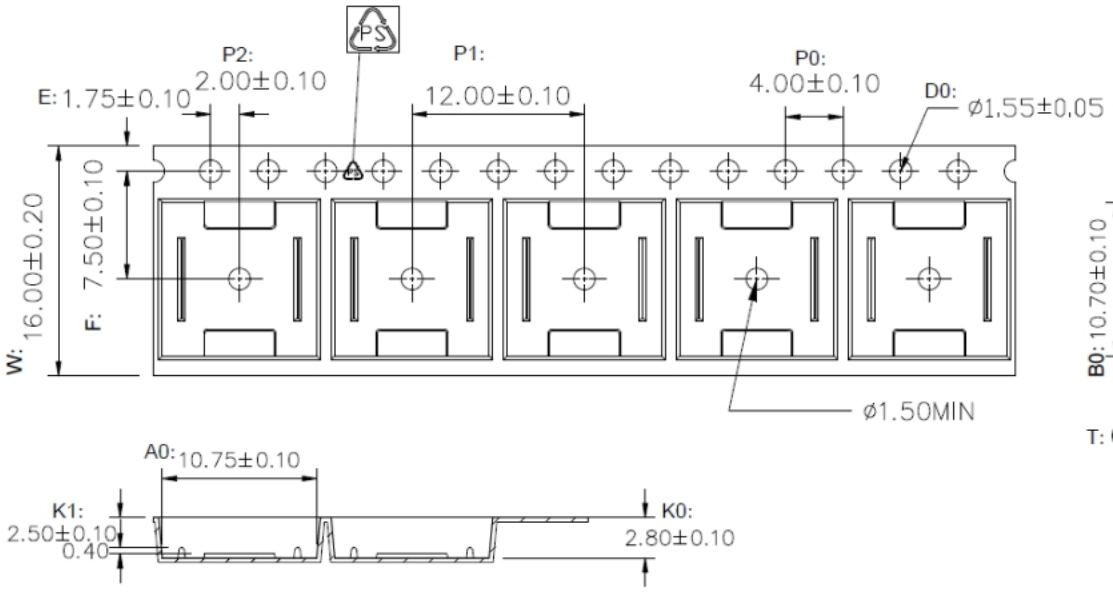




ARBOR HOLE
DETAIL A
SCALE : 3:1

PRODUCT SPECIFICATION						
TAPE WIDTH	ØA ±2.0	ØN ±2.0	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	8.4 +1.5 -0.0	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4 +2.0 -0.0	18.4		5.5
16MM	330	178	16.4 +2.0 -0.0	22.4		5.5
24MM	330	178	24.4 +2.0 -0.0	30.4		5.5
32MM	330	178	32.4 +2.0 -0.0	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{6} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{5} & BELOW 10^{5}	CONDUCTIVE (GENERIC)	BLACK ONLY
E	10^{9} TO 10^{11}	ANTISTATIC (COATED)	ALL TYPES



1. 10 sprocket hole pitch cumulative tolerance ±0.20 .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy .
4. All dimensions meet EIA-481 requirements.
5. Thickness : 0.30±0.05mm.
6. Packing length per 22" reel : 378 Meters.(復卷 N=122）
7. Component load per 13" reel : 1000 pcs.
8. Surface resistivity :10^{5} ~ 10^{10}Ω/□

RoHS

W	16.00±0.20
A0	10.75±0.10
B0	10.70±0.10
K0	2.80±0.10
K1	2.50±0.10

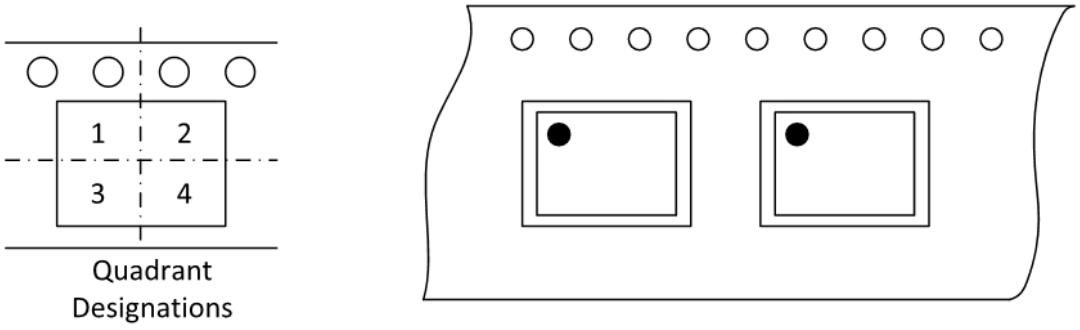


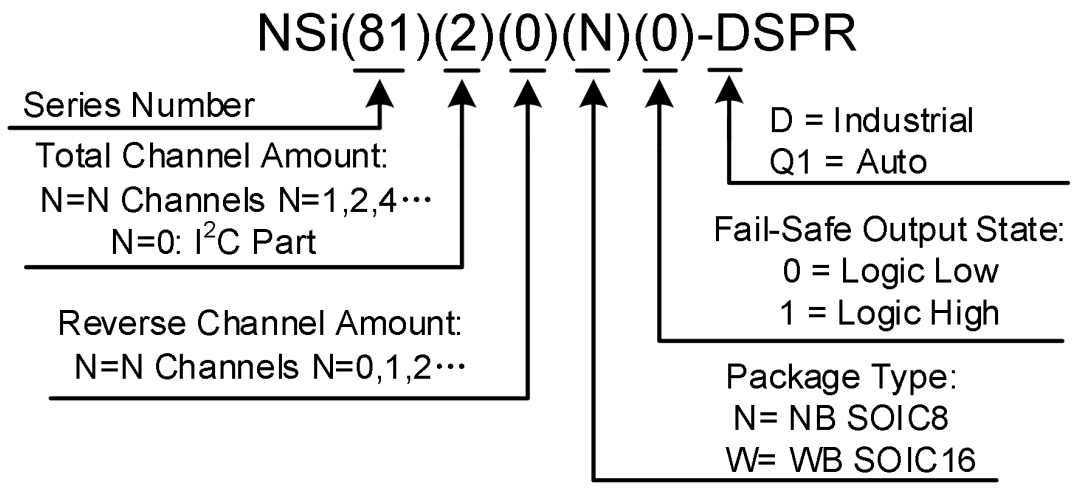
Figure 7.2 Tape and Reel Information of SOW16

11. Order Information

Part No.	Isolation Rating(kV)	Number of side 1 inputs	Number of side 2 inputs	Max Data Rate (Mbps)	Default Output State	Temperature	MSL	Package Type	Package Drawing	SPQ
NSi8120N0	3.75	2	0	150	Low	-40 to 125℃	1	SOP8 (150mil)	SOP8	2500
NSi8120N	3.75	2	0	150	High	-40 to 125℃	1	SOP8 (150mil)	SOP8	2500
NSi8121N0	3.75	1	1	150	Low	-40 to 125℃	1	SOP8 (150mil)	SOP8	2500
NSi8121N1	3.75	1	1	150	High	-40 to 125℃	1	SOP8 (150mil)	SOP8	2500
NSi8122N0	3.75	1	1	150	Low	-40 to 125℃	1	SOP8 (150mil)	SOP8	2500
NSi8122N1	3.75	1	1	150	High	-40 to 125℃	1	SOP8 (150mil)	SOP8	2500
NSi8120W0	5	2	0	150	Low	-40 to 125℃	2	SOP16 (300mil)	SOW16	1000
NSi8120W1	5	2	0	150	High	-40 to 125℃	2	SOP16 (300mil)	SOW16	1000
NSi8121W0	5	1	1	150	Low	-40 to 125℃	2	SOP16 (300mil)	SOW16	1000
NSi8121W1	5	1	1	150	High	-40 to 125℃	2	SOP16 (300mil)	SOW16	1000
NSi8122W0	5	1	1	150	Low	-40 to 125℃	2	SOP16 (300mil)	SOW16	1000
NSi8122W1	5	1	1	150	High	-40 to 125℃	2	SOP16 (300mil)	SOW16	1000

NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 ℃ according to the JEDEC industry standard classifications and peak solder temperatures.
All devices are AEC-Q100 qualified.

Part Number Rule:



12. Revision History

Revision	Description	Date
1.0	Original	2017/11/15
1.1	Change to Ordering information	2018/3/26
1.2	Add maximum operation current specification.	2018/6/20
1.3	Change block diagram	2018/7/28
1.4	Correct Table 6.2 Pin No.	2018/8/20
1.5	Add specification “Input Pull high or low Current”	2018/9/10
1.6	Add “Maximum Input/Output Pulse Voltage”	2018/10/9
1.7	Change to Ordering information	2018/12/20
1.8	Change Certification Information	2019/06/17
1.9	Add Recommended operating conditions	2020/2/27
2.0	Update format	2021/2/25
2.1	Added MSL information	2021/3/28
2.2	changed tape and reel information of SOW16	2021/5/16
2.3	Correct part number,Change Storage Temperature	2021/11/17