REVISION HISTORY

Revision	Description	Issue Date
Rev. 1.0	Initial Issue	Dec.1.2006
Rev. 1.1	Revised V_{IH} to TTL compatible	Jan.9.2008
Rev. 1.2	Revised V_{IH} to 0.7*Vcc	May.6.2008
Rev. 1.3	Revised V_{DR}	Mar.3.2009
Rev. 1.4	Revised V_{TERM} to V_{T1} and V_{T2} Revised Test Condition of I_{SB1}/I_{DR} Revised **FEATURES** & **ORDERING INFORMATION** **Lead free and green package available** to **Green package available** Added packing type in **ORDERING INFORMATION** Deleted T_{SOLDER} in **ABSOLUTE MAXIMUN RATINGS** Adding PKG type : 32 TSOP-II	Aug.5.2009
Rev. 1.5	Revised **PACKAGE OUTLINE DIMENSION** in page 9/10/11	May.7.2010
Rev. 1.6	Revised typo in **PIN CONFIGURATION**	Jul.21.2010
Rev. 1.7	Revised **ORDERING INFORMATION** in page 12 Revised **PACKAGE OUTLINE DIMENSION** in page 8/12	Aug.25.2010
Rev. 1.8	Revised typo in **REVISION HISTORY** **ORDERING INFORMATION** in page 12 to 13	Oct.29.2010
Rev. 1.9	Added SL Grade Deleted E Grade Revised I_{SB1}/I_{DR}	Aug.9.2011
Rev. 1.10	Added PKG type : 32 P-DIP	Nov.24.2011
Rev. 1.11	Revised “Standby Power Supply Current” in page 4 Revised “Data Retention Current” in page 8	Apr.30.2012

LY62W5128

Rev. 1.11

512K X 8 BIT LOW POWER CMOS SRAM

FEATURES

- Fast access time : 55/70ns
- Low power consumption:
  Operating current : 30/20mA (TYP.)
  Standby current : 4μA (TYP.) LL-version
  3μA (TYP.) SL-version
- Single 2.7V ~ 5.5V power supply
- All outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage : 1.5V (MIN.)
- **Green package available**
- Package : 32-pin 450 mil SOP
  32-pin 8mm x 20mm TSOP-I
  32-pin 8mm x 13.4mm STSOP
  36-ball 6mm x 8mm TFBGA
  32-pin 400 mil TSOP-II
  32-pin 600 mil P-DIP

GENERAL DESCRIPTION

The LY62W5128 is a 4,194,304-bit low power CMOS static random access memory organized as 524,288 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

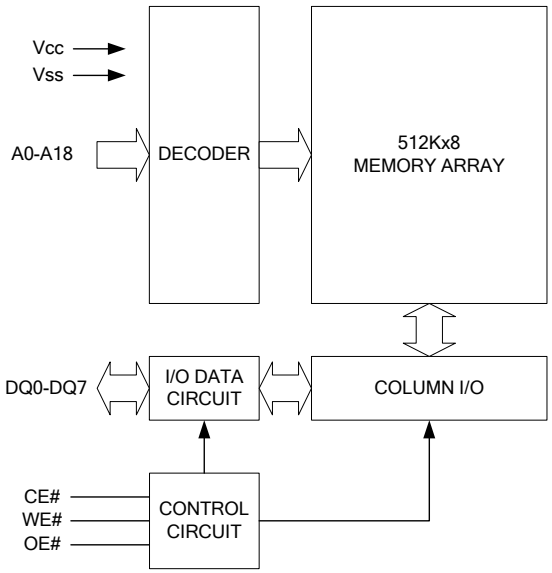
The LY62W5128 is well designed for very low power system applications, and particularly well suited for battery back-up nonvolatile memory application.

The LY62W5128 operates from a single power supply of 2.7V ~ 5.5V and all inputs and outputs are fully TTL compatible

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation	
				Standby(I_{SB1}TYP.)	Operating(Icc,TYP.)
LY62W5128	0 ~ 70℃	2.7 ~ 5.5V	55/70ns	4μA(LL)/3μA(SL)	30/20mA
LY62W5128(I)	-40 ~ 85℃	2.7 ~ 5.5V	55/70ns	4μA(LL)/3μA(SL)	30/20mA

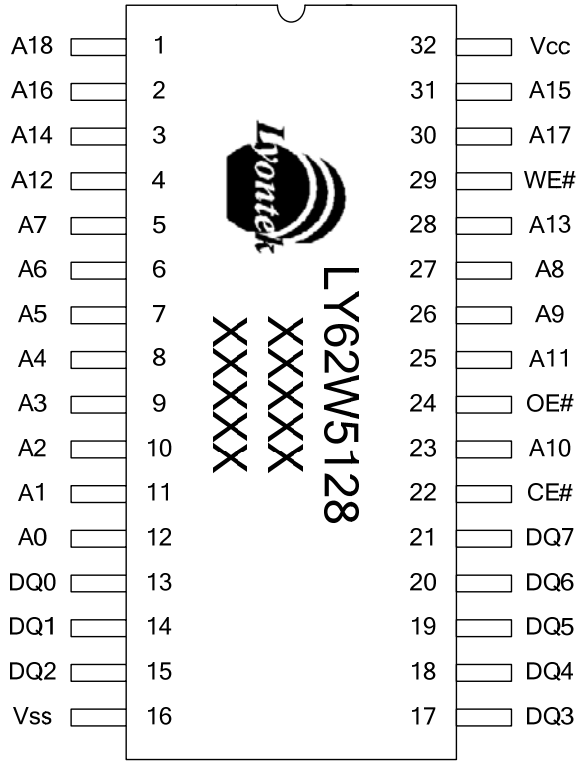
FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

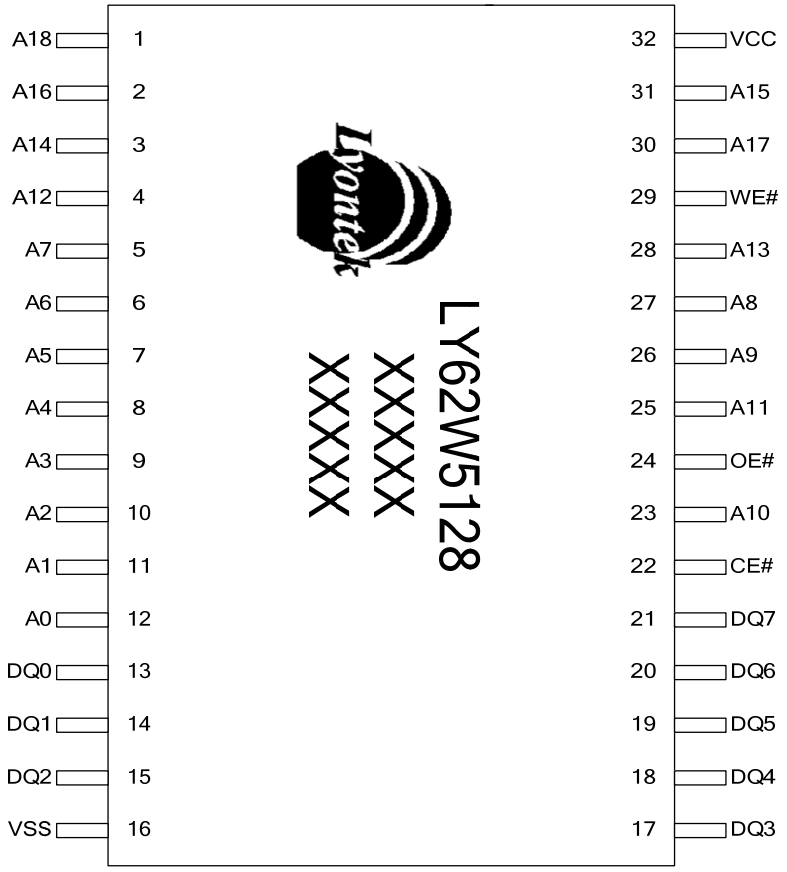
SYMBOL	DESCRIPTION
A0 - A18	Address Inputs
DQ0 – DQ7	Data Inputs/Outputs
CE#	Chip Enable Inputs
WE#	Write Enable Input
OE#	Output Enable Input
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

PIN CONFIGURATION

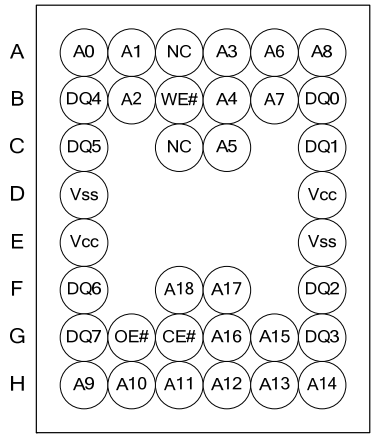


SOP/P-DIP

TSOP-I/STSOP



TSOP-II



TFBGA(See through with Top View)

TFBGA(Top View)

ABSOLUTE MAXIMUN RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V_{CC} relative to V_{SS}	V_{T1}	-0.5 to 6.5	V
Voltage on any other pin relative to V_{SS}	V_{T2}	-0.5 to V_{CC}+0.5	V
Operating Temperature	T_A	0 to 70(C grade) -40 to 85(I grade)	℃
Storage Temperature	T_{STG}	-65 to 150	℃
Power Dissipation	P_D	1	W
DC Output Current	I_{OUT}	50	mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	High-Z	I_{SB1}
Output Disable	L	H	H	High-Z	I_{CC},I_{CC1}
Read	L	L	H	D_{OUT}	I_{CC},I_{CC1}
Write	L	X	L	D_{IN}	I_{CC},I_{CC1}

Note: H = V_{IH}, L = V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP. *4	MAX.	UNIT
Supply Voltage	V_{CC}			2.7	3.0	5.5	V
Input High Voltage	V_{IH} *1			0.7*V_{CC}	-	V_{CC}+0.3	V
Input Low Voltage	V_{IL} *2			- 0.2	-	0.6	V
Input Leakage Current	I_{LI}	$V_{CC} \geqq V_{IN} \geqq V_{SS}$		- 1	-	1	µA
Output Leakage Current	I_{LO}	$V_{CC} \geqq V_{OUT} \geqq V_{SS}$, Output Disabled		- 1	-	1	µA
Output High Voltage	V_{OH}	I_{OH} = -1mA		2.4	2.7	-	V
Output Low Voltage	V_{OL}	I_{OL} = 2mA		-	-	0.4	V
Average Operating Power supply Current	I_{CC}	Cycle time = Min. CE# = V_{IL} and CE2 = V_{IH}, $I_{I/O}$ = 0mA Other pins at V_{IL} or V_{IH}	- 55	-	30	60	mA
			- 70	-	20	50	mA
	I_{CC1}	Cycle time = 1µs CE#≦0.2V and CE2≧V_{CC}-0.2V,, $I_{I/O}$ = 0mA Other pins at 0.2V or V_{CC}-0.2V		-	4	10	mA
Standby Power Supply Current	I_{SB1}	CE# ≧V_{CC}-0.2V or CE2≦0.2V Others at 0.2V or V_{CC} - 0.2V	LL/LLI	-	4	50	µA
			SL *5 25℃	-	3	10	µA
			SLI *5 40℃	-	3	10	µA
			SL/SLI	-	3	25	µA

Notes:
1. V_{IH}(max) = V_{CC} + 3.0V for pulse width less than 10ns.
2. V_{IL}(min) = V_{SS} - 3.0V for pulse width less than 10ns.
3. Over/Undershoot specifications are characterized, not 100% tested.
4. Typical values are included for reference only and are not guaranteed or tested.
   Typical values are measured at V_{CC} = V_{CC}(TYP.) and T_A = 25℃
5. This parameter is measured at V_{CC} = 3.0V

CAPACITANCE (T_A = 25℃, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C_{IN}	-	6	pF
Input/Output Capacitance	$C_{I/O}$	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to V_{CC} - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C_L = 30pF + 1TTL, I_{OH}/I_{OL} = -2mA/4mA

AC ELECTRICAL CHARACTERISTICS

(1) READ CYCLE

PARAMETER	SYM.	LY62W5128-55		LY62W5128-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	55	-	70	-	ns
Address Access Time	t_{AA}	-	55	-	70	ns
Chip Enable Access Time	t_{ACE}	-	55	-	70	ns
Output Enable Access Time	t_{OE}	-	30	-	35	ns
Chip Enable to Output in Low-Z	t_{CLZ}*	10	-	10	-	ns
Output Enable to Output in Low-Z	t_{OLZ}*	5	-	5	-	ns
Chip Disable to Output in High-Z	t_{CHZ}*	-	20	-	25	ns
Output Disable to Output in High-Z	t_{OHZ}*	-	20	-	25	ns
Output Hold from Address Change	t_{OH}	10	-	10	-	ns

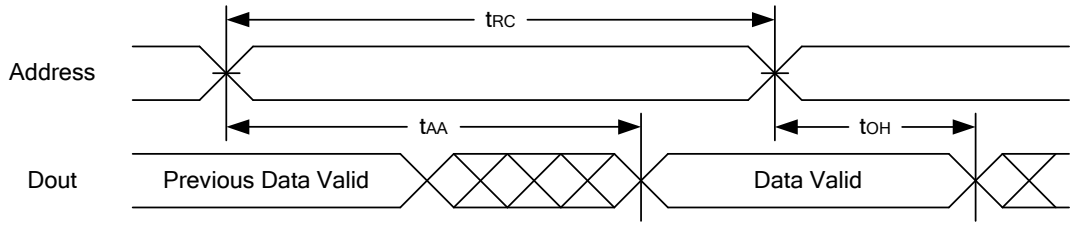
(2) WRITE CYCLE

PARAMETER	SYM.	LY62W5128-55		LY62W5128-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	55	-	70	-	ns
Address Valid to End of Write	t_{AW}	50	-	60	-	ns
Chip Enable to End of Write	t_{CW}	50	-	60	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	ns
Write Pulse Width	t_{WP}	45	-	55	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	ns
Data to Write Time Overlap	t_{DW}	25	-	30	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	0	-	ns
Output Active from End of Write	t_{OW}*	5	-	5	-	ns
Write to Output in High-Z	t_{WHZ}*	-	20	-	25	ns

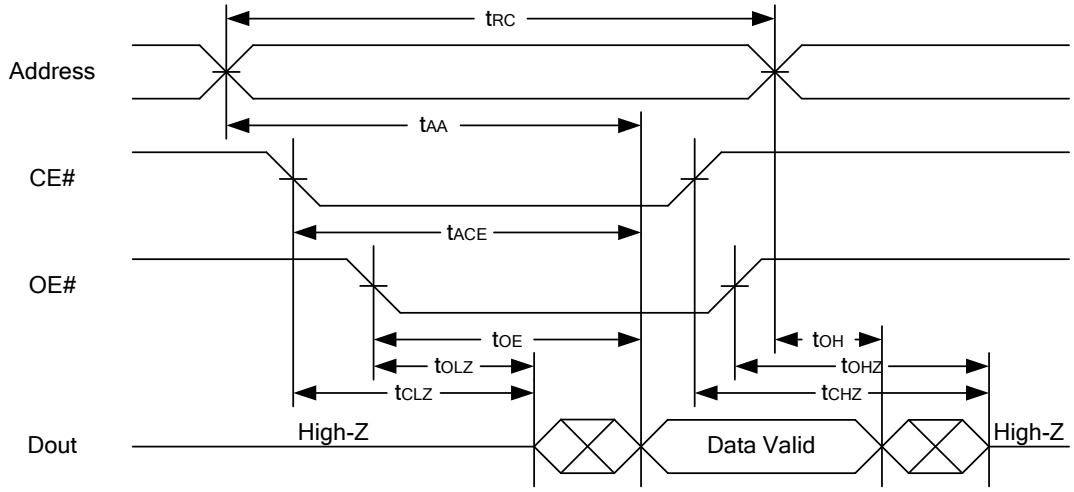
*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)

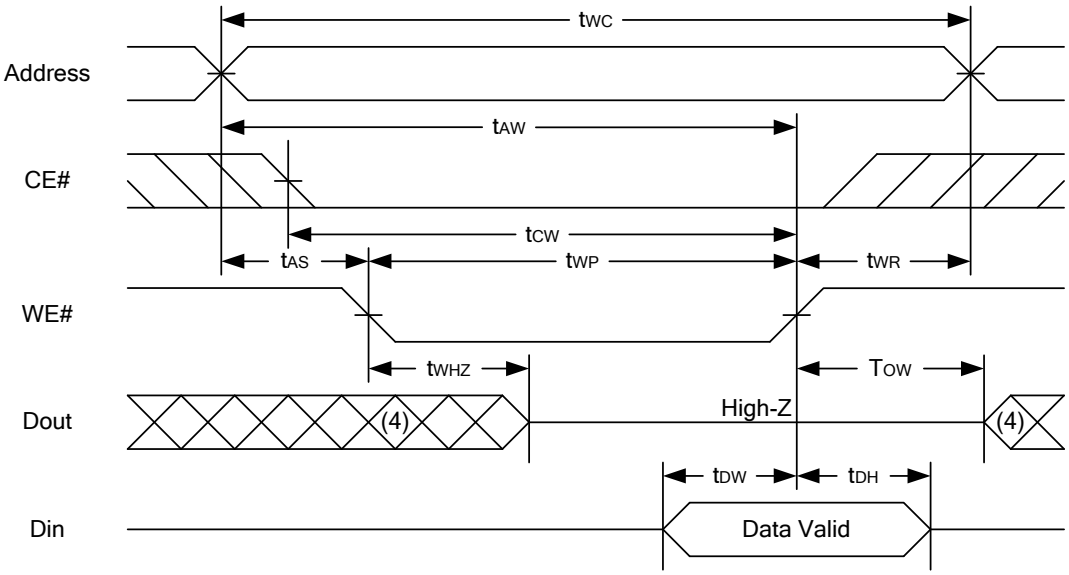


READ CYCLE 2 (CE# and OE# Controlled) (1,3,4,5)

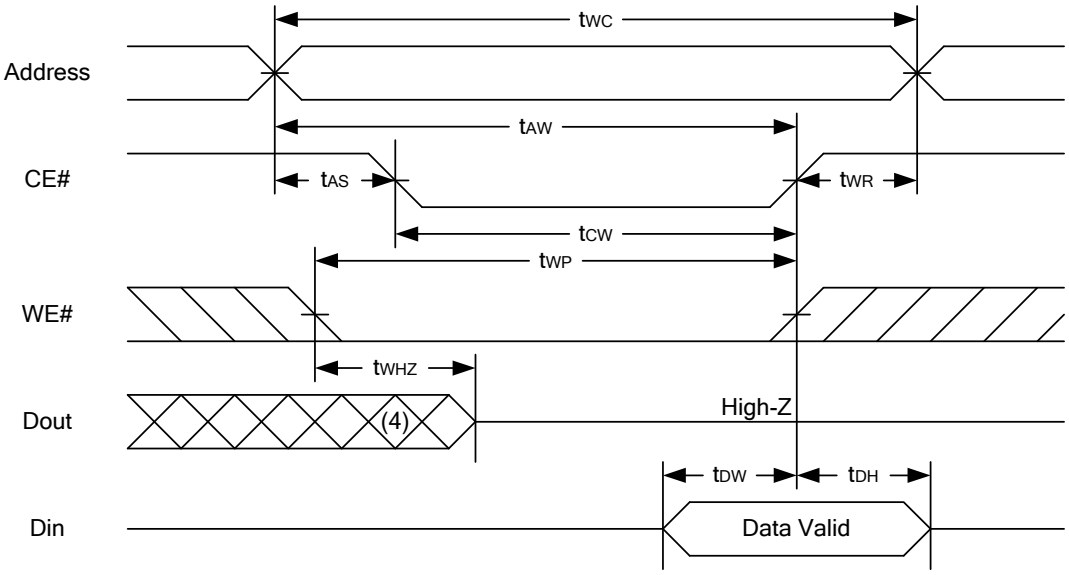


Notes :
1.WE# is high for read cycle.
2.Device is continuously selected OE# = low, CE# = low.
3.Address must be valid prior to or coincident with CE# = low,; otherwise t_{AA} is the limiting parameter.
4.t_{CLZ}, t_{OLZ}, t_{CHZ} and t_{OHZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.
5.At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{OHZ} is less than t_{OLZ}.

WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)



WRITE CYCLE 2 (CE# Controlled) (1,2,5,6)



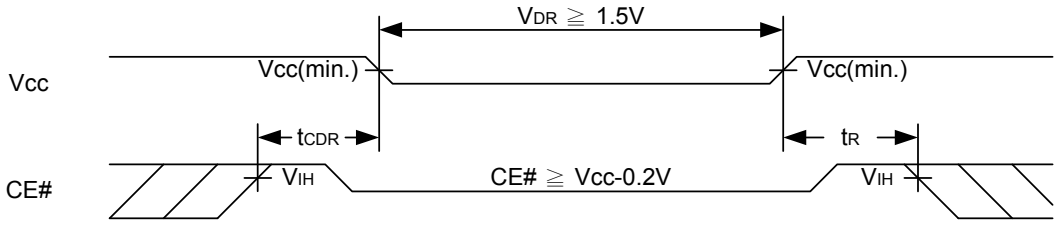
Notes :
1.WE#, CE# must be high during all address transitions.
2.A write occurs during the overlap of a low CE#, low WE#.
3.During a WE# controlled write cycle with OE# low, t_{WP} must be greater than $t_{WHZ} + t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
4.During this period, I/O pins are in the output state, and input signals must not be applied.
5.If the CE# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6.t_{OW} and t_{WHZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.

DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
V_{CC} for Data Retention	V_{DR}	CE# ≧ V_{CC} - 0.2V or CE2 ≦ 0.2V			1.5	-	5.5	V
Data Retention Current	I_{DR}	V_{CC} = 1.5V CE# ≧ V_{CC} - 0.2V or CE2 ≦ 0.2V Other pins at 0.2V or V_{CC}-0.2V	LL/LLI		-	2	30	µA
			SL	25℃	-	2	8	µA
			SLI	40℃	-	2	8	µA
			SL/SLI		-	2	23	µA
Chip Disable to Data Retention Time	t_{CDR}	See Data Retention Waveforms (below)			0	-	-	ns
Recovery Time	t_R				t_{RC*}	-	-	ns

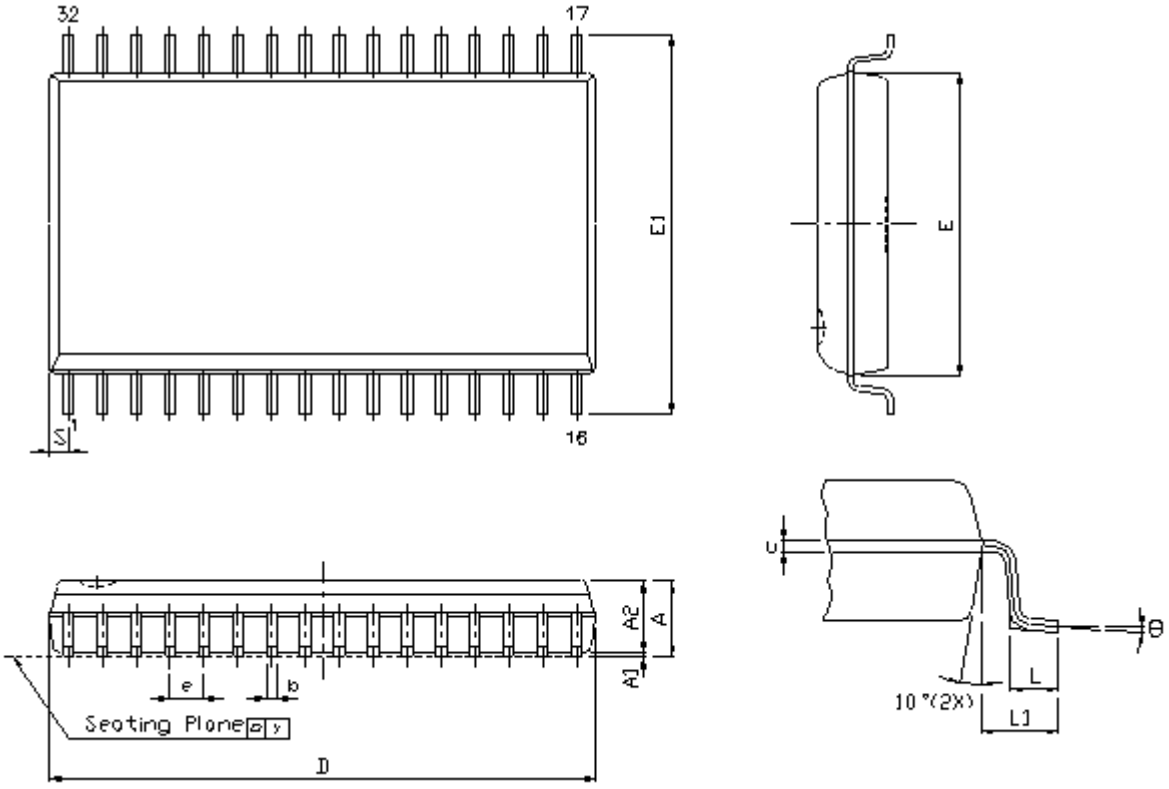
t_{RC*} = Read Cycle Time

DATA RETENTION WAVEFORM



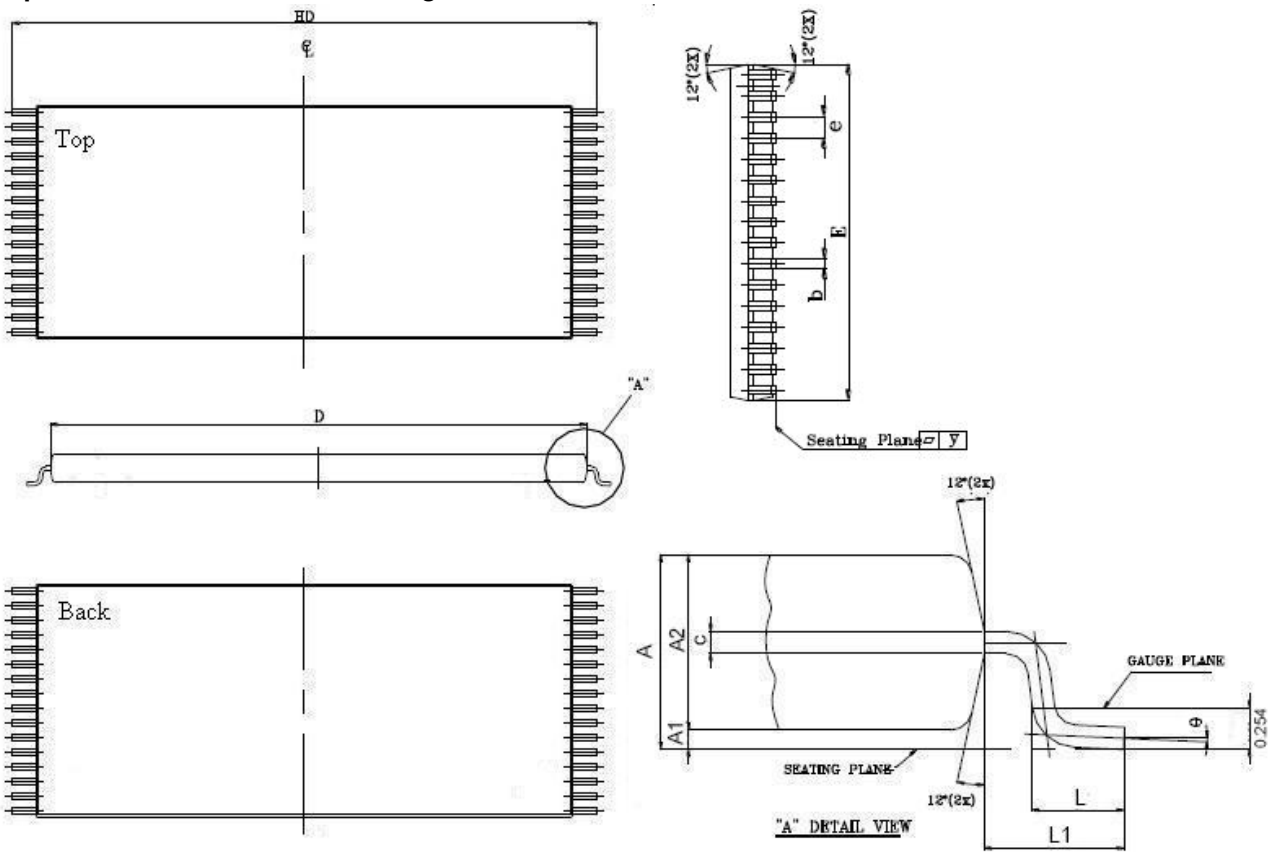
PACKAGE OUTLINE DIMENSION

32 pin 450 mil SOP Package Outline Dimension



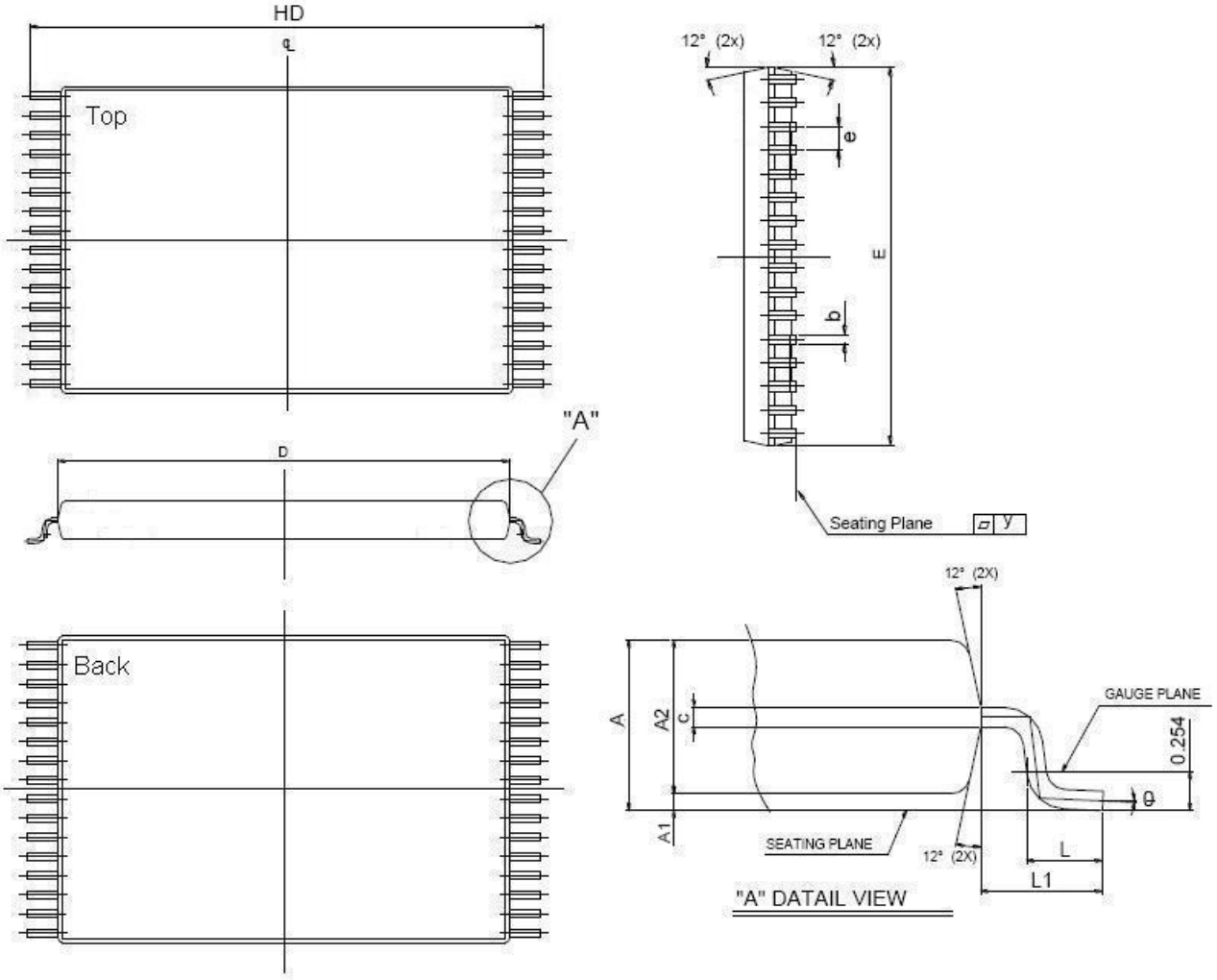
SYM. \ UNIT	INCH.(BASE)	MM(REF)
A	0.120(MAX)	3.048(MAX)
A1	0.004(MIN)	0.102(MIN)
A2	0.116(MAX)	2.946(MAX)
b	0.016(TYP)	0.406(TYP)
c	0.008(TYP)	0.203(TYP)
D	0.817(MAX)	20.75(MAX)
E	0.445±0.006	11.303±0.152
E1	0.555±0.025	14.097±0.635
e	0.050(TYP)	1.270(TYP)
L	0.033±0.017	0.838±0.432
L1	0.055±0.008	1.397±0.203
S	0.026(MAX)	0.660(MAX)
y	0.004(MAX)	0.101(MAX)
Θ	0^{o} -10^{o}	0^{o} -10^{o}

32 pin 8mm x 20mm TSOP-I Package Outline Dimension



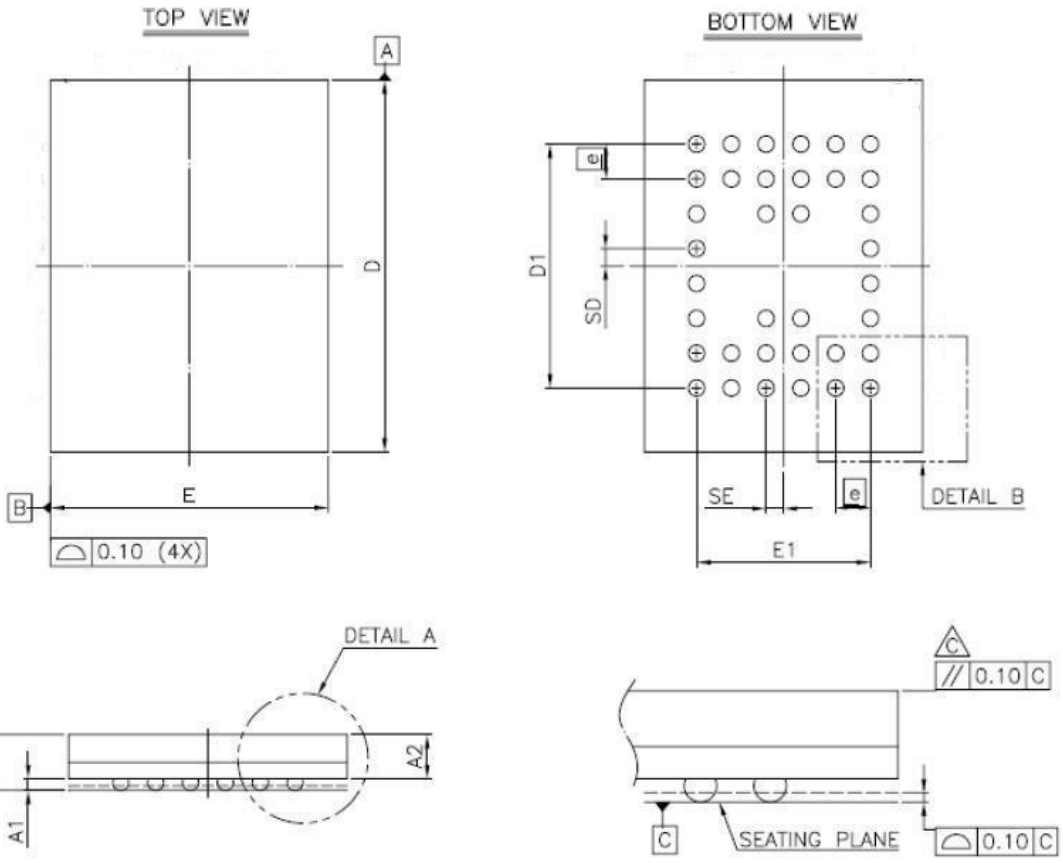
SYM. \ UNIT	INCH(BASE)	MM(REF)
A	0.047 (MAX)	1.20 (MAX)
A1	0.004 ±0.002	0.10 ±0.05
A2	0.039 ±0.002	1.00 ±0.05
b	0.009 ±0.002	0.22 ±0.05
c	0.006 ±0.002	0.155 ±0.055
D	0.724 ±0.008	18.40 ±0.20
E	0.315 ±0.008	8.00 ±0.20
e	0.020 (TYP)	0.50 (TYP)
HD	0.787 ±0.008	20.00 ±0.20
L	0.024 ±0.004	0.60 ±0.10
L1	0.0315 ±0.004	0.08 ±0.10
y	0.003 (MAX)	0.08 (MAX)
Θ	0^{o}～5^{o}	0^{o}～5^{o}

32 pin 8mm x 13.4mm STSOP Package Outline Dimension

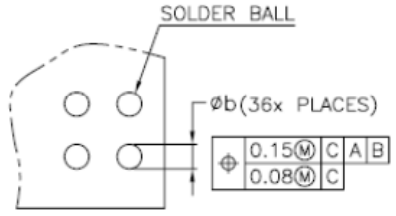


SYM. \ UNIT	INCH(BASE)	MM(REF)
A	0.049 (MAX)	1.25 (MAX)
A1	0.004 ±0.002	0.10 ±0.05
A2	0.039 ±0.002	1.00 ±0.05
b	0.009 ±0.002	0.22 ±0.05
c	0.006 ±0.002	0.155 ±0.055
D	0.465 ±0.008	11.80 ±0.20
E	0.315 ±0.008	8.00 ±0.20
e	0.020 (TYP)	0.50 (TYP)
HD	0.528±0.008	13.40 ±0.20.
L	0.02 ±0.008	0.50 ±0.20
L1	0.031 ±0.005	0.8 ±0.125
y	0.003 (MAX)	0.076 (MAX)
Θ	0°～5°	0°～5°

36 ball 6mm × 8mm TFBGA Package Outline Dimension

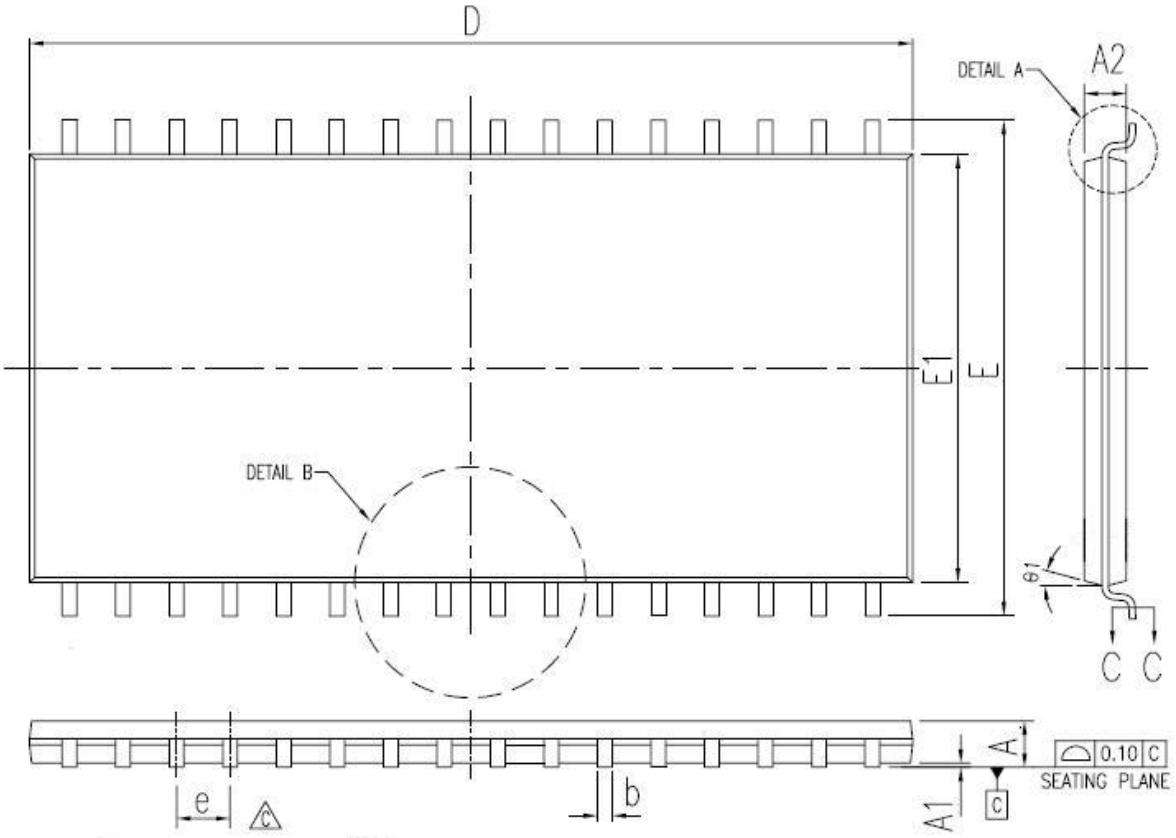


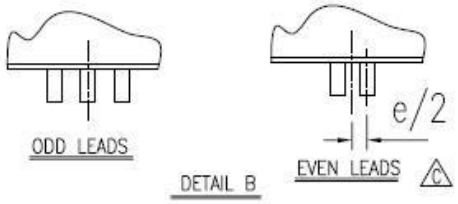
SYM.	DIMENSION (mm)			DIMENSION (inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.20	0.25	0.30	0.008	0.010	0.012
A2	—	—	0.94	—	—	0.037
b	0.30	0.35	0.40	0.012	0.014	0.016
B D	7.95	8.00	8.05	0.313	0.315	0.317
D1	5.25 BSC			0.207 BSC		
B E	5.95	6.00	6.05	0.234	0.236	0.238
E1	3.75 BSC			0.148 BSC		
SE	0.375 TYP			0.015 TYP		
SD	0.375 TYP			0.015 TYP		
e	0.75 BSC			0.030 BSC		

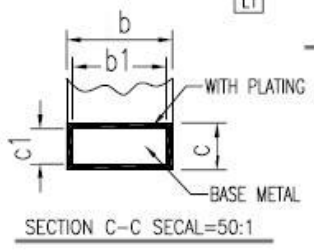


NOTE:
1. CONTROLLING DIMENSION : MILLIMETER.
2. REFERENCE DOCUMENT : JEDEC MO-207.

32-pin 400mil TSOP-Ⅱ Package Outline Dimension





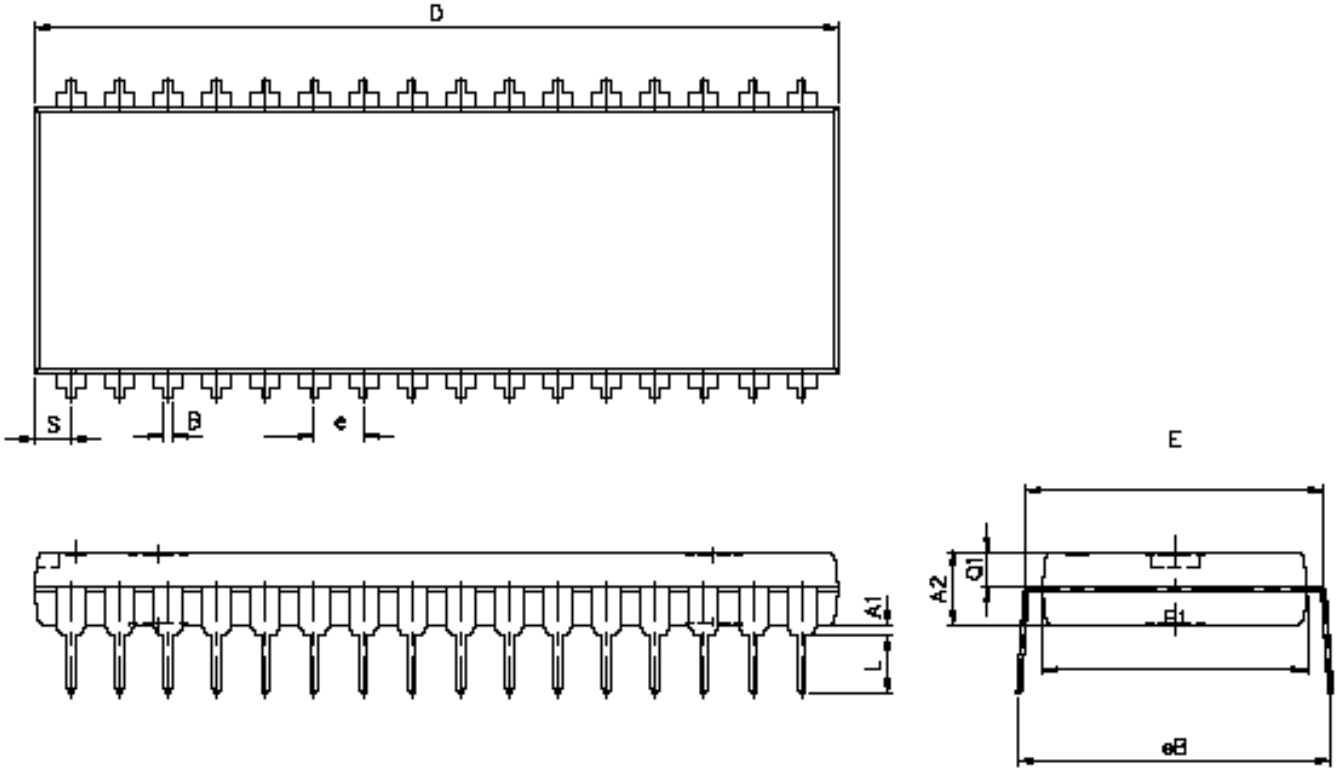


SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A			1.20			0.047
A1	0.05		0.15	0.002		0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
c	0.10	---	0.21	0.004	---	0.008
c1	0.10	---	0.16	0.004	---	0.006
D	20.82	20.95	21.08	0.820	0.825	0.830
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.405
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	0.25 BASIC			0.010 BASIC		
R	0.12	---	0.35	0.005	---	0.014
R1	0.12	---	---	0.005	---	---
θ	0		8	0		8
θ1	10	15	20	10	15	20

N	32L		
e	1.27 BASIC		
b	0.30	---	0.52
b1	0.30	0.40	0.45
JEDEC	MS-024(BA)		

NOTE : DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSIONS.
D AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

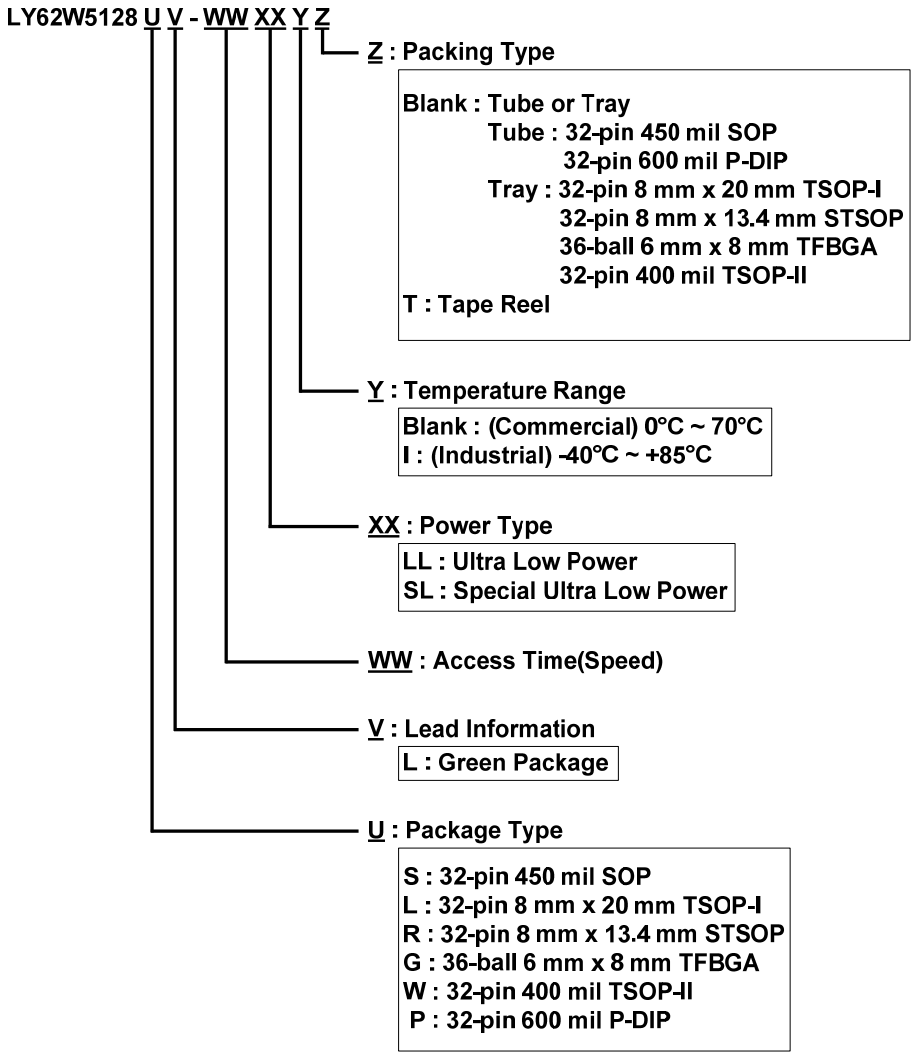
32 pin 600 mil P-DIP Package Outline Dimension



UNIT / SYM.	INCH(BASE)	MM(REF)
A1	0.015(MIN)	0.381(MIN)
A2	0.155±0.005	3.937±0.127
B	0.018±0.005	0.457±0.127
D	1.650±0.01	41.910±0.254
E	0.600±0.010	15.240±0.254
E1	0.545±0.005	13.843±0.127
e	0.100(TYP)	2.540(TYP)
eB	0.650±0.020	16.510±0.508.
L	0.158±0.043	4.013±1.092
S	0.075±0.010	1.905±0.254
Q1	0.070±0.005	1.778±0.127

Note : D/E1/S dimension do not include mold flash.

ORDERING INFORMATION



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