171021501/WPMDU1251501NT

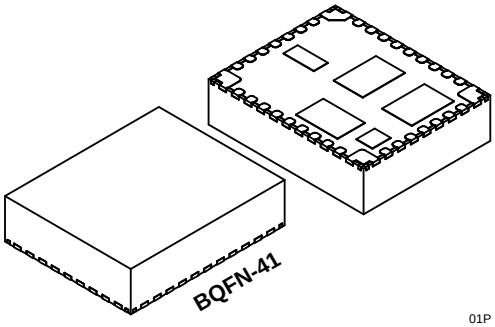
MagI³C Power Module Product Family
VDRM - Variable Step Down Regulator Module

A DESCRIPTION

The VDRM series of the MagI³C Power Modules Family comprises a fully integrated current mode DC/DC power supply with the switching power stage, control circuitry and passives all in one package. These devices also have a built-in compensation circuitry and soft-start feature for a smooth, safe power up. The small QFN package is easy to solder onto a printed circuit board where a low profile is demand. The MagI³C Power Module requires as few as five external components and eliminates loop compensation and magnetics part selection process.

The VDRM series offers high efficiency and delivers up to 2.5A of output current with accurate regulated output voltages. It operates from input voltage 7V to 50V.

The VDRM regulators also have on-board protection circuitry to avoid thermal and electrical damage. The MagI³C Power Module offers flexibility and the feature of a discrete point-of-load design. This is ideal for powering a wide area of systems and ICs.



01P

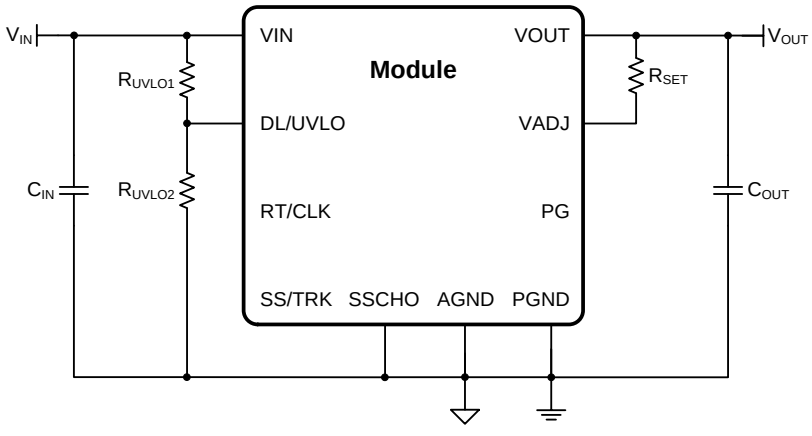
B FEATURES

- Peak efficiency up to 96%
- Current capability up to 2.5A
- Wide input voltage range: 7V-50V
- Regulated output voltages: 2.5V-15V
- 65V Line Transient Protection
- Switching frequency range: 400kHz-1MHz adjustable
- External clock synchronisation
- Built-in soft-start and tracking
- Power Good signal and pre-bias output
- Under voltage lockout protection (UVLO)
- Voltage overshoot and over-current protection
- Over temperature and current protection
- Operating ambient temperature: -40-85°C
- EN55022 Class B compliant

C APPLICATIONS

- Point of Load DC-DC applications
- Servers, Data and Telecom
- System power supplies
- DSPs, FPGAs, MCUs and MPUs
- I/O interface

D TYPICAL APPLICATION CIRCUIT



01S

V_{OUT}(V)	**3.3**	**5.0**	**12**
R_{SET}(kΩ)	31.6	52.3	140
R_{RT}(kΩ)	OPEN	1100	267
R_{UVLO1}(kΩ)	174	174	174
R_{UVLO2}(kΩ)	40.2	31.6	15.4
C_{IN}(µF)$_{min}$	4.7	2x2.2	2x2.2
C_{OUT}(µF)$_{min}$	2x47	2x47	2x47
V_{IN}(V)	7 to 36	8 to 50	15 to 50
f_{SW}(kHz)	400	500	800

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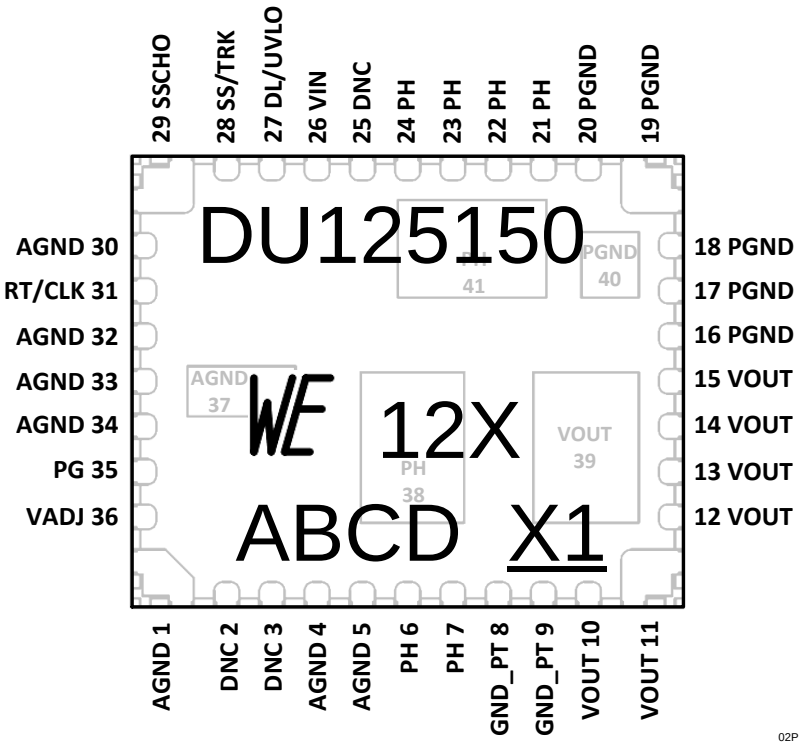
E PACKAGE MARKING



Top View BQFN-41

First row: Product number

Second row: Logo & Code

Third row: Product code

F PIN DESCRIPTION

PIN #	PIN SYMBOL	PIN DESCRIPTION
26	VIN	1I Input power supply
10, 11, 12, 13, 14, 15, 39	VOUT	2I Output power supply
1, 4, 5, 30, 32, 33, 34, 37	AGND	3I These pins are connected to the internal analog ground of the device.
16, 17, 18, 19, 20, 40	PGND	4I This is the return current path for the power stage of the device.
8, 9	GND_PT	5I Ground point. Connect AGND to PGND at these pins as shown in the Layout Considerations.
35	PG	6I Power Good flag pin.
36	VADJ	7I Sets the output voltage
31	RT/CLK	8I These pin set the internal frequency over a resistor and can also use to synchronize to an external clock.
27	DL/UVLO	9I Deadlock and UVLO adjust pin.
28	SS/TRK	10I Soft-start or tracking pin.
29	SSCHO	11I Soft-start and track feature select.
6, 7, 21, 22, 23, 24, 38, 41	PH	12I Phase switch node.
2, 3, 25	DNC	Do Not Connect.

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G ORDERING INFORMATION

ORDER CODE	PART DESCRIPTION	PACKAGE	PACKING UNIT
171021501	WPMDU1251501NT	BQFN-41	Tape and Reel with 250 Units
178021501	WPMDU1251501NEV	box	1

H SALES INFORMATION

SALES CONTACTS

Würth Elektronik eiSos GmbH & Co. KG
EMC & Inductive Solutions
Max-Eyth-Str. 1
74638 Waldenburg
Germany
Tel. +49 (0) 79 42 945 - 0
www.we-online.com
powermodules@we-online.de

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I ABSOLUTE MAXIMUM RATINGS (1)

Preventive Caution: Exceeding the listed absolute maximum ratings below may affect the device negatively and may cause permanent damage. Therefore operating ratings are conditions under which operation of the device is intended to be functional. All values are referenced to AGND. -40°C ≤ T_A ≤ +85°C, V_{IN} = 24 V, V_{OUT} = 5.0 V, I_{OUT} = 2.5 A, R_T = Open, C_{IN} = 2 x 2.2 µF ceramic, C_{OUT} = 2 x 47 µF ceramic, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{IN}	Input voltage V_{IN}	-0.3 to 65	V
DL/UVLO	Under voltage lockout	-0.3 to 5	V
VADJ	Adjustable output voltage	-0.3 to 3	V
PG	Power Good	-0.3 to 6	V
SS/TRK	Soft Start/Tracking	-0.3 to 3	V
SSCHO	Soft Start + Tracking Feature	-0.3 to 3	V
RT/CLK	Timer/ Clock	-0.3 to 3.6	V
PH	Phase switching node	-0.6 to 65	V
V_{OUT}	Output voltage V_{OUT}	-0.6 to V_{IN}	V
VDIFF	GND to exposed thermal pad	±200	mV
RT/CLK	Source current	100	µA
DL/UVLO	Source current	100	µA
SS/TRK	Sink current	200	µA
PG	Sink current	10	mA
T_J	Junction temperature	-40 to 105(2)	°C
T_{ST}	Storage temperature	-65 to 150	°C
T_{SOLR}	Soldering temperature reflow, leads(13) max. 30s	245	°C

J RECOMMENDED OPERATING CONDITIONS (1)

SYMBOL	PARAMETER	MIN (6)	TYP (7)	MAX (6)	UNIT
V_{IN}	Input voltage	7	-	50	V
V_{OUT}	Output voltage	2.5	-	15	V
f_{SW}	Switching Frequency	400	-	1000	kHz
T_A	Ambient operating temperature	-40	-	85	°C

K THERMAL SPECIFICATIONS

SYMBOL	PARAMETER	VALUE	UNIT
θ_{JA}	Thermal resistance junction to ambient (3)	14	°C/W
ϕ_{JT}	Thermal resistance junction to top (4)	3.3	°C/W
ϕ_{JB}	Thermal resistance junction to board (5)	6.8	°C/W
$T_{SD-HYST}$	Thermal shut down hysteresis, falling	15	°C
T_{SD}	Thermal shut down	180	°C

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L ELECTRICAL SPECIFICATIONS

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SYMBOL	PARAMETER	CONDITIONS	MIN [6]	TYP [7]	MAX [6]	UNIT
Specifications regarding input voltage pin V_{IN}						
V_{IN}	Input voltage range	Over output current range	7[8]	-	50[9]	V
Specifications regarding output voltage pin V_{OUT}						
V_{UVLO}	VIN under voltage lockout	No hysteresis, rising and falling	-	2.5	-	V
$V_{OUT(adj)}$	Output voltage range	Regulated output voltage	2.5[10]	-	15	V
I_{OUT}	Output current	Over output current range	0	-	2.5	A
V_{OUT}	Set-point voltage tolerance	T_A = 25°C; I_{OUT} = 100mA	-	-	±2.0[11]	%
	Temperature variation	-40°C ≤ T_A ≤ +85°C	-	±0.5	±1.0	%
	Line regulation	Over input voltage range	-	±0.1	-	%
	Load regulation	Over output current range	-	±0.4	-	%
	Total output voltage variation	Includes set-point, line, load, and temperature variation	-	-	±3.0[11]	%
$V_{PP\%}$	Output voltage ripple	20 MHz bandwidth, 0.25A ≤ I_{OUT} ≤ 2.5A, V_{OUT} ≥3.3V	-	1	-	%
I_{LIM}	Current limit threshold		-	5.1	-	A
Specifications regarding performance						
η	Efficiency	V_{IN} = 24 V, I_{OUT} = 1.5 A, V_{OUT} = 5 V, f_{SW} = 500 kHz	-	84	-	%
		V_{IN} = 48V I_{OUT} = 1.5A, V_{OUT} = 5 V, f_{SW} = 500 kHz	-	79	-	%
System specifications						
T_{TR}	Transient response Recovery time	1A/µs load step from 50 to 100%,	-	400	-	µs
V_{TR}	Transient response V_{OUT} over/undershooter	1A/µs load step from 50 to 100%,	-	90	-	mV
f_{SW}	Switching Frequency	RT/CLK pin open	300	400	500	kHz
f_{CLK}	Synchronization frequency	CLK Control	300		1000	kHz
D_{CLK}	Duty cycle CLK	CLK Control	25	50	75	%
V_{CLK-H}	High-Level Threshold CLK	CLK Control	-	1.9	2.2	V
V_{CLK-L}	Low-Level Threshold CLK	CLK Control	0.5	0.7	-	V
Specifications regarding Enable pin DL						
V_{DL}	Deadlock threshold current	No hysteresis	1.15	1.25	1.36[12]	V
I_{DL}	Deadlock Input current	V_{DL} < 1.15 V	-	-0.9	-	µA
		V_{DL} > 1.36 V	-	-3.8	-	µA
I_{SD}	Shut Down current	V_{DL} = 0 V	-	1.3	4	µA

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SYMBOL	PARAMETER	CONDITIONS	MIN (6)	TYP (7)	MAX (6)	UNIT
Specifications regarding Power Good pin PG						
PG	Power Good Thresholds	V_{OUT} rising	-	$_{good}$ 94	-	%
			-	$_{fault}$ 109	-	%
		V_{OUT} falling	-	$_{fault}$ 91	-	%
			-	$_{good}$ 106	-	%
	Power Good Low Voltage	I(PG) = 3.5mA	-	0.2	-	V

NOTES

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) See the temperature derating curves in the Typical Characteristics section for thermal information.

(3) The junction-to-ambient thermal resistance, θ_{JA}, applies to devices soldered directly to a 100 mm x 100 mm double-sided, 4-layer PCB with 35µm. copper and natural convection cooling. Additional airflow reduces θ_{JA}.

(4) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature, TJ, of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). TJ = ψJT * Pdis + TT; where Pdis is the power dissipated in the device and TT is the temperature of the top of the device.

(5) The junction-to-board characterization parameter, ψJB, estimates the junction temperature, TJ, of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). TJ = ψJB * Pdis + TB; where Pdis is the power dissipated in the device and TB is the temperature of the board 1mm from the device.

(6) Min and Max limits are 100 % production tested at 25 °C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).

(7) Typical numbers are at 25 °C and represent the most likely parametric norm.

(8) For output voltages ≤ 12 V, the minimum input voltage is 7 V or (V_{OUT}+ 3 V), whichever is greater. For output voltages > 12 V, the minimum input voltage is (1.33 x V_{OUT}).

(9) The maximum input voltage is 50 V or (15 x V_{OUT}), whichever is less.

(10) Output voltages < 3.3 V are subject to reduced V_{IN}(max) specifications and higher ripple magnitudes.

(11) The stated limit of the set-point voltage tolerance includes the tolerance of both the internal voltage reference and the internal adjustment resistor. The overall output voltage tolerance is affected by the tolerance of the external R_{SET} resistor.

(12) Value when no voltage divider is present at the DL/UVLO pin.

(13) JEDEC J-STD020

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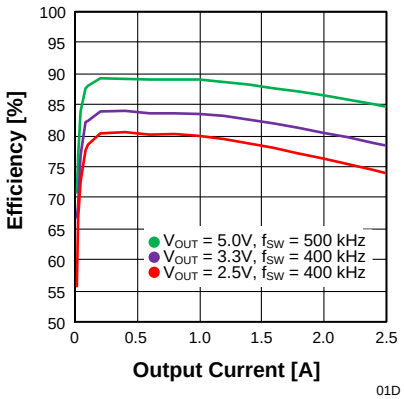
MagI³C Power Module Product Family
VDRM - Variable Step Down Regulator Module

M TYPICAL PERFORMANCE CURVES

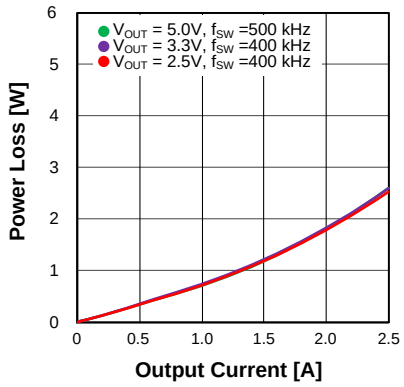
The electrical characteristic data has been developed from actual products tested at 25 °C. This data is considered typical for the converter. At light load the output voltage ripple may increase due to pulse skipping. See Light-Load Behavior for more information. The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to devices soldered directly to a 100 mm × 100 mm double-sided PCB with 35 mm copper.

Efficiency: V_{IN} = 12V @ T_{AMB} = 25°C



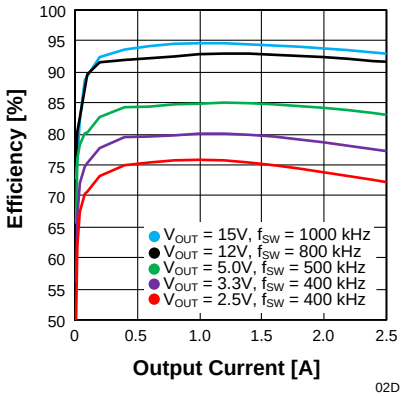
01D

Power Loss: V_{IN} = 12V @ T_{AMB} = 25°C



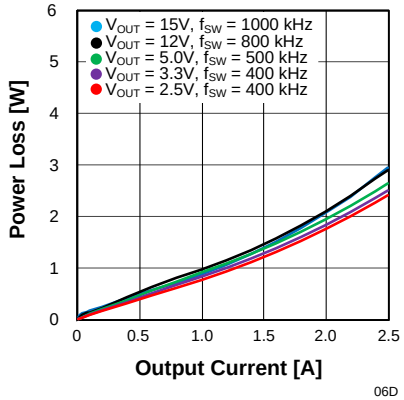
05D

Efficiency: V_{IN} = 24V @ T_{AMB} = 25°C



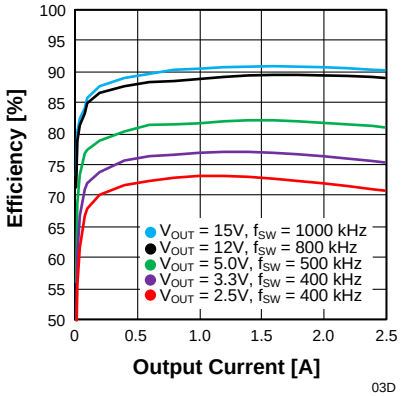
02D

Power Loss: V_{IN} = 24V @ T_{AMB} = 25°C



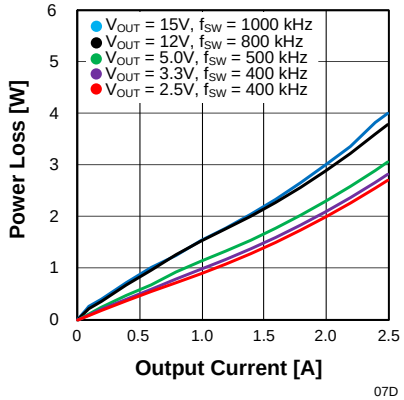
06D

Efficiency: V_{IN} = 36V @ T_{AMB} = 25°C



03D

Power Loss: V_{IN} = 36V @ T_{AMB} = 25°C



07D

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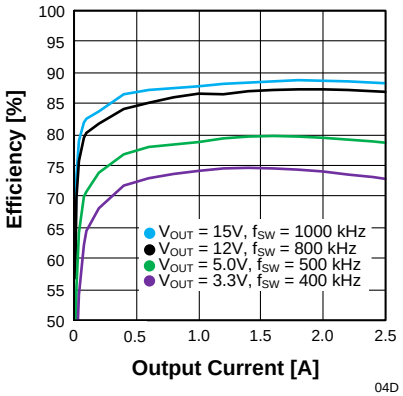
TYPICAL PERFORMANCE CURVES

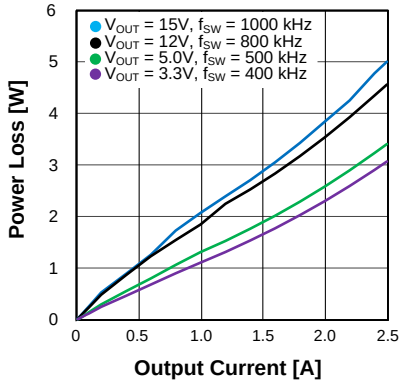
The electrical characteristic data has been developed from actual products tested at 25 °C. This data is considered typical for the converter. At light load the output voltage ripple may increase due to pulse skipping. See Light-Load Behavior for more information. The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to devices soldered directly to a 100 mm × 100 mm double-sided PCB with 35 mm copper.

Efficiency: V_{IN} = 48V @ T_{AMB} = 25°C



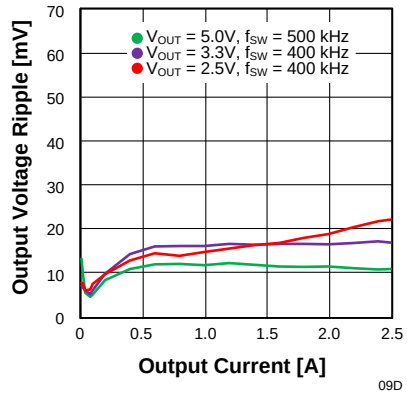
04D

Power Loss: V_{IN} = 48V @ T_{AMB} = 25°C



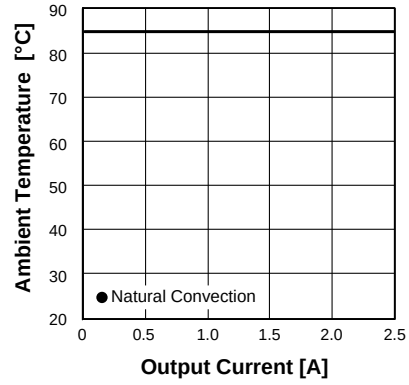
08D

Output Voltage Ripple: V_{IN} = 12V @ T_{AMB} = 25°C



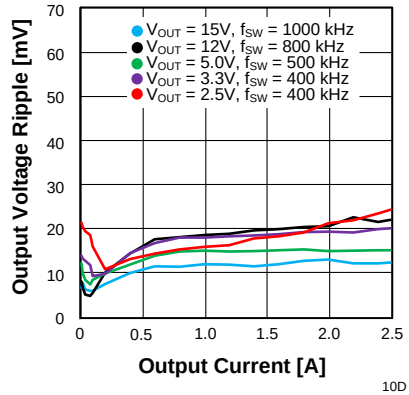
09D

Thermal Derating: V_{IN} = 12V; V_{OUT} = all voltages



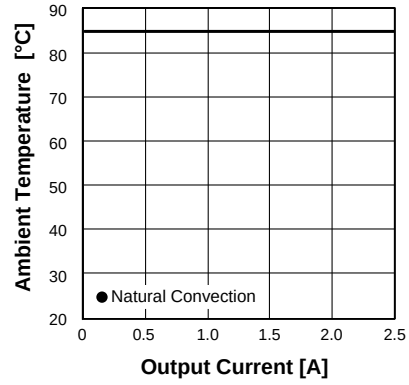
11D

Output Voltage Ripple: V_{IN} = 24V @ T_{AMB} = 25°C



10D

Thermal Derating: V_{IN} = 24V; V_{OUT} = all voltages



12D

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TYPICAL PERFORMANCE CURVES

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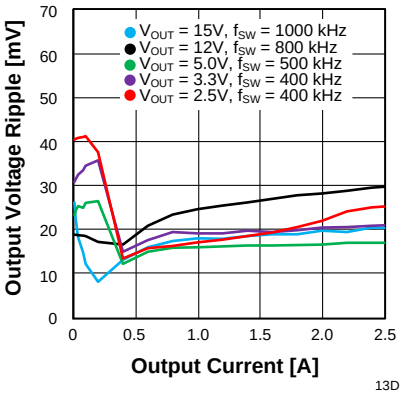
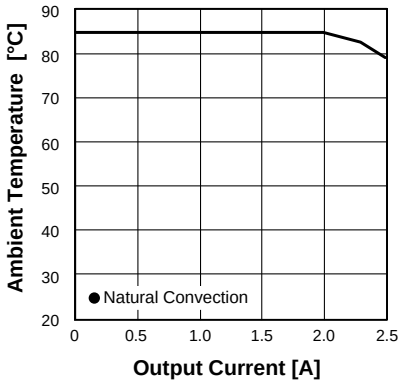
Output Voltage Ripple: V_{IN} = 36V @ T_{AMB} = 25°C



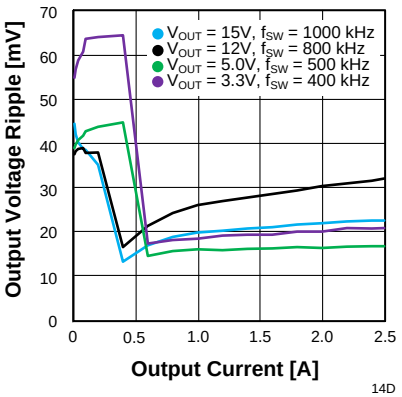
13D

Thermal Derating: V_{IN} = 36V; V_{OUT} = all voltages



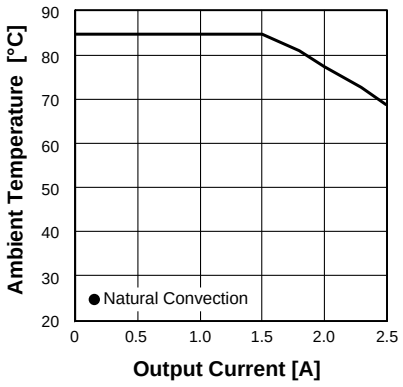
15D

Output Voltage Ripple: V_{IN} = 48V @ T_{AMB} = 25°C



14D

Thermal Derating: V_{IN} = 48V; V_{OUT} = all voltages



16D

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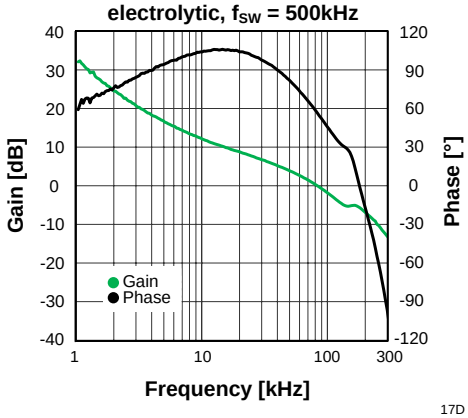
VDRM - Variable Step Down Regulator Module

TYPICAL PERFORMANCE CURVES

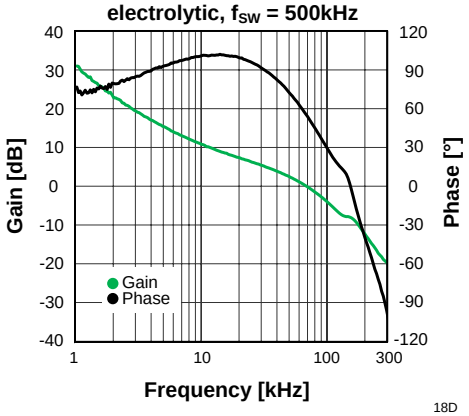
The electrical characteristic data has been developed from actual products tested at 25 °C. This data is considered typical for the converter. At light load the output voltage ripple may increase due to pulse skipping. See Light-Load Behavior for more information. The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to devices soldered directly to a 100 mm × 100 mm double-sided PCB with 35 mm copper.

Bode diagram: V_{IN} = 12V; V_{OUT} = 5V; I_{OUT} = 2A; C_{OUT1} = 44µF ceramic; C_{OUT2} = 56µF electrolytic, f_{SW} = 500kHz



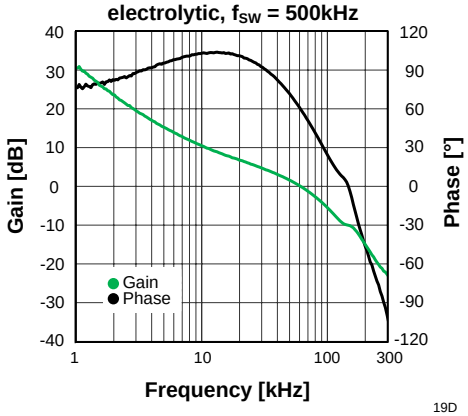
17D

Bode diagram: V_{IN} = 24V; V_{OUT} = 5V; I_{OUT} = 2A; C_{OUT1} = 44µF ceramic; C_{OUT2} = 56µF electrolytic, f_{SW} = 500kHz



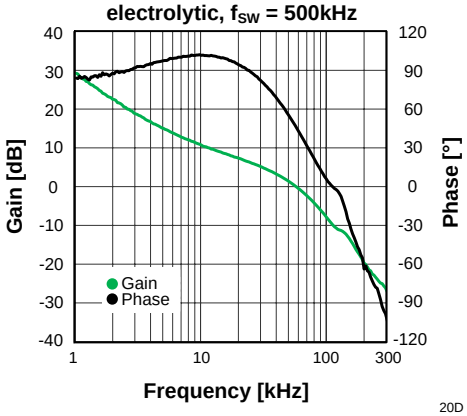
18D

Bode diagram: V_{IN} = 36V; V_{OUT} = 5V; I_{OUT} = 2A; C_{OUT1} = 44µF ceramic; C_{OUT2} = 56µF electrolytic, f_{SW} = 500kHz



19D

Bode diagram: V_{IN} = 48V; V_{OUT} = 5V; I_{OUT} = 2A; C_{OUT1} = 44µF ceramic; C_{OUT2} = 56µF electrolytic, f_{SW} = 500kHz



20D

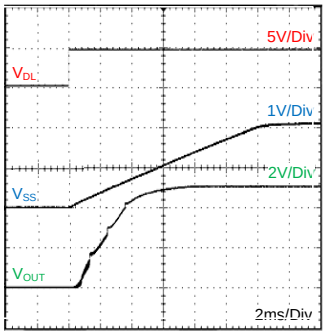
171021501/WPMDU1251501NT

MagI³C Power Module Product Family
VDRM - Variable Step Down Regulator Module

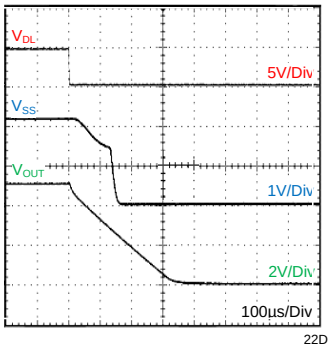
TYPICAL PERFORMANCE CURVES

The electrical characteristic data has been developed from actual products tested at 25 °C. This data is considered typical for the converter. At light load the output voltage ripple may increase due to pulse skipping. See Light-Load Behavior for more information. The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to devices soldered directly to a 100 mm × 100 mm double-sided PCB with 35 mm copper.

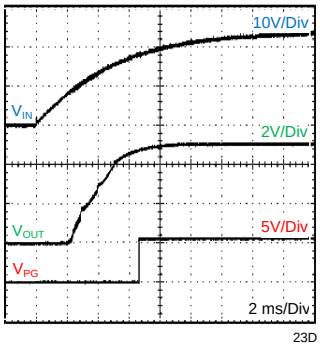
Deadlock start-up I_{OUT} = 2A



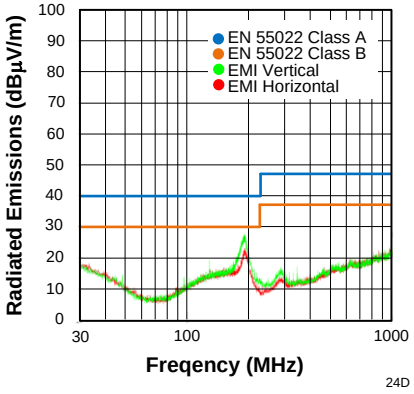
Deadlock shut-down I_{OUT} = 2A



Startup V_{IN} = 10V; I_{OUT} = 2A



Radiated Emissions EN55022 compliant:
V_{IN} = 24V;V_{OUT} = 5V Load = 2A



171021501/WPMDU1251501NT

MagI³C Power Module Product Family
VDRM - Variable Step Down Regulator Module

N CIRCUIT DESCRIPTION

N1 MagI³C 6 Steps to design the power application

The next 6 simple steps will show how to select the external components to design your power application:

1. **Program output voltage**
2. **Program under voltage lockout divider**
3. **Set operating frequency**
4. **Select Input Capacitor**
5. **Select Output Capacitor**
6. **Layout considerations**

The Typical Basic Schematic below shows a MagI³C Power Module schematic with the key parameter-setting resistors labeled.

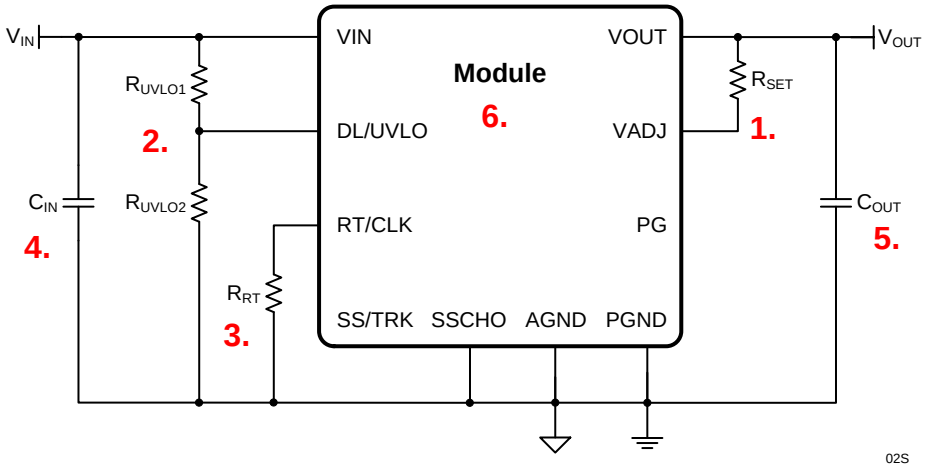


Figure 1. Typical Basic Schematic

Step 1. Program output voltage (R_{SET})
The MagI³C Power Module is designed to provide output voltages from 2.5 V to 15 V. The output voltage is determined by the value of R_{SET}, which must be connected between the V_{OUT} node and the V_{ADJ} pin (Pin 36). For output voltages higher than 5 V, improved operating performance can be obtained by increasing the operating frequency. This adjustment requires the addition of R_{RT} between RT/CLK (Pin 31) and AGND (Pin 30). See the Step 3 Set operating frequency section for more details. Table 1 gives the standard external R_{SET} resistor for a number of common bus voltages and also includes the recommended R_{RT} resistor for output voltages above 5 V.

Table 1: Recommended standard output voltages

V_{OUT}	R_{SET}	R_{RT}	f_{SW}
2.5V	21.5kΩ	Open	400kHz
3.3V	31.6kΩ	Open	400kHz
5V	52.3kΩ	1.1MΩ	500kHz
9V	102kΩ	365kΩ	700kHz
12V	140kΩ	267kΩ	800kHz
15V	178kΩ	178kΩ	1000kHz

For other output voltages the value of R_{SET} can be calculated using the following formula.

$$R_{SET} = 10 * \left(\frac{V_{OUT}}{0.798} - 1\right) k\Omega \qquad (1)$$

Step 2. Program under voltage lockout divider (R_{UVLO1} and R_{UVLO2})

At turn-on, the V_{ON} UVLO threshold determines the input voltage level where the device begins power conversion. During the power-down sequence, the V_{OFF} UVLO threshold determines the input voltage where power conversion ceases. The turn-on and turn-off thresholds are set by two resistors, R_{UVLO1} and R_{UVLO2} as shown in Figure 2. The V_{ON} UVLO threshold must be set to at least (V_{OUT} + 3 V) or 6.5 V whichever is higher to insure proper startup and reduce current surges on the host input supply as the voltage rises. If possible, it is recommended to set the UVLO threshold to approximately 80 to 85% of the minimum expected input voltage.

Use Equation 2 and Equation 3 to calculate the values of R_{UVLO1} and R_{UVLO2}. V_{ON} is the voltage threshold during power-up when the input voltage is rising. V_{OFF} is the voltage threshold during power-down when the input voltage is decreasing. V_{OFF} should be selected to be at least 500 mV less than V_{ON}. Table 2 lists standard resistor values for R_{UVLO1} and R_{UVLO2} for adjusting the V_{ON} UVLO threshold for several input voltages.

$$R_{UVLO1} = \frac{(V_{ON} - V_{OFF})}{2.9 * 10^{-3}}\ k\Omega \quad (2)$$

$$R_{UVLO2} = \frac{1.25}{\left(\frac{(V_{ON} - 1.25)}{R_{UVLO1}}\right) + 0.9 * 10^{-3}}\ k\Omega \quad (3)$$

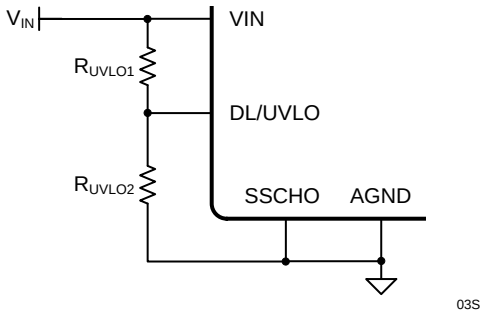


Figure 2. Under voltage Lockout (UVLO) Schematic

Table 2: Standard $V_{ON\ Threshold}$ Values

$V_{ON\ Threshold}$	R_{UVLO1}	R_{UVLO2}
6.5V	174kΩ	40.2kΩ
10V		24.3kΩ
15V		15.8kΩ
20V		11.5kΩ
25V		9.09kΩ
30V		7.5kΩ
35V		6.34kΩ
40V		5.62kΩ
45V		4.99kΩ

Step 3. Set operating frequency

Nominal switching frequency of the MagI³C Power Module is set from the factory at 400 kHz. This switching frequency is optimized for output voltages below 5 V. For output voltages of 5 V and above, better operating performance can be obtained raising the operating frequency. This is easily done by adding a resistor, R_{RT} in , from the RT/CLK pin (Pin 31) to the AGND pin (Pin 30). Raising the operating frequency reduces output voltage ripple, lowers the load current threshold where pulse skipping begins, and improves transient response. The recommended switching frequency for typical output voltages is listed in Table 1.

For the maximum recommended output voltage value of 15 V, the switching frequency computes to 1 MHz. Operation above 1 MHz is not recommended. Use Table 3 below to select the value of the timing resistor for the given values of switching frequencies.

Table 3: Standard Switching Frequencies

V_{OUT}	f_{SW}	R_{RT}
2.5V	**400kHz**	Open
3.3V	**400kHz**	Open
5V	**500kHz**	1,1MΩ
9V	**700kHz**	365kΩ
12V	**800kHz**	267kΩ
15V	**1MHz**	178kΩ

It is also possible to synchronize the switching frequency to an external clock signal. See the Step E Synchronization CLK option section for further details. While it is possible to set the operating frequency higher than 400 kHz when using the device at output voltages of 5 V or less, minimum duty cycle and pulse skipping issues restrict the maximum recommended input voltage under these conditions. The recommended operating conditions for the MagI³C Power Module can be summarized by Figure 3. The graph shows the maximum input voltage vs. output voltage restriction for several operating frequencies. The lower boundary of the graph shows the minimum input voltage as a function of the output voltage.

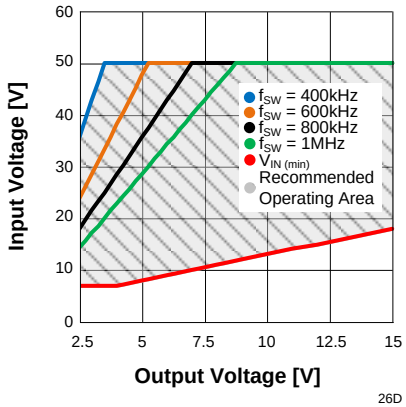


Figure 3. Input Voltage vs. Output Voltage Operating Area

Step 4. Select Input Capacitor (C_{IN})

The MagI³C Power Module requires a minimum input capacitance of 4.4 µF of ceramic type. The voltage rating of input capacitors must be higher than the maximum input voltage. The ripple current rating of the capacitor must be at least 450 mA_{rms}. Table 4 includes a preferred list of capacitors.

Table 4: Recommended input and output capacitors(1):

Series	Description	Case Size	ESR(2) mΩ
X5R	4.7µF; 50V; ±10%	1206	2
X5R	22µF; 16V; ±10%	1210	2
X5R	47µF; 6.3V; ±20%	1210	2
POSCAP	68µF; 16V; POSCAP		50
POSCAP	100µF; 6.3V;		25
T530	220µF; 6.3V;		6

(1) Capacitor Supplier Verification, RoHS, Lead-free and Material Details Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in this table.
(2) Maximum ESR @ 100 kHz, 25°C.

Step 5. Select Output Capacitor (C_{OUT})

The output capacitance of the MagI³C Power Module can be comprised of either all ceramic capacitors, or a combination of ceramic and bulk capacitors. The required output capacitance must include at least 100 µF of ceramic type (or 2 x 47 µF). When adding additional non-ceramic bulk capacitors, low-ESR devices like the ones recommended in Table 4 are required. Additional capacitance above the minimum is determined by actual transient deviation requirements. Table 4 includes a preferred list of capacitors.

Step 6. Layout considerations

To achieve optimal electrical and thermal performance, an optimized PCB layout is required. Figure 4 and Figure 5 show two layers of a typical PCB layout. Some considerations for an optimized layout are:

1. Use large copper areas for power planes (VIN, VOUT, and PGND) to minimize conduction loss and thermal stress.
2. Place ceramic input and output capacitors close to the module pins to minimize high frequency noise.
3. Locate additional output capacitors between the ceramic capacitor and the load.
4. Place a dedicated AGND copper area beneath the MagI³C Power Module.
5. Isolate the PH copper area from the VOUT copper area using the PGND copper area.
6. Connect the AGND and PGND copper area at one point; at pins 8 & 9.
7. Place R_{SET}, R_{RT}, and C_{SS} as close as possible to their respective pins.
8. Use multiple vias to connect the power planes to internal layers.
9. Use a dedicated sense line to connect R_{SET} to VOUT near the load for best regulation.

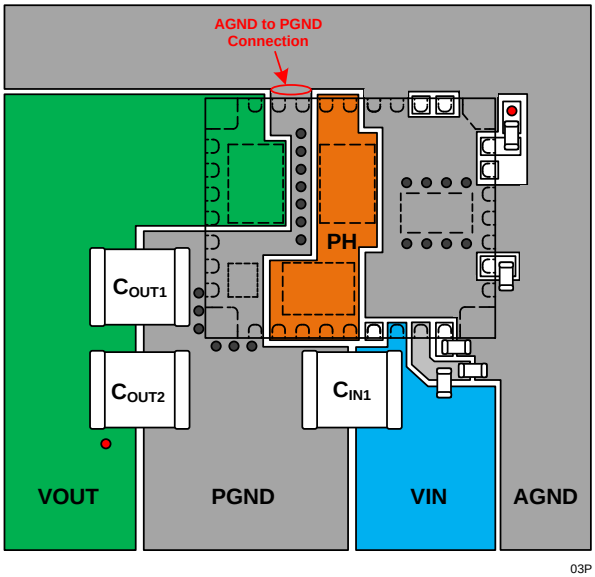


Figure 4. Layout top layer

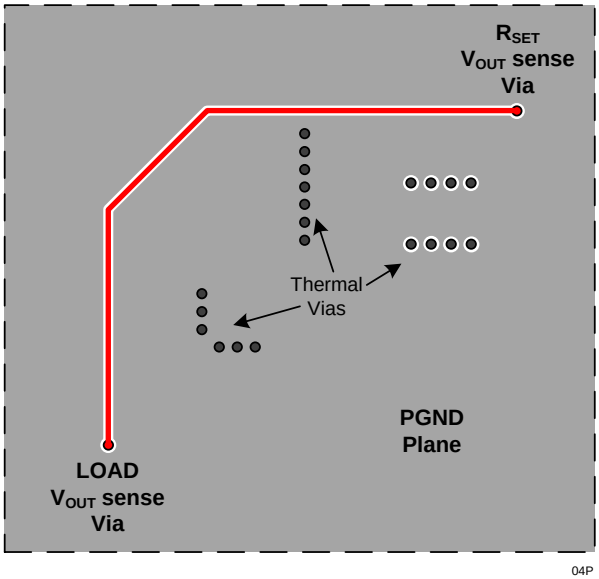


Figure 5. Layout bottom layer

N2 MagI³C optional Features:

The MagI³C Power Module can operate over a wide input voltage range of 7 V to 50 V and produce output voltages from 2.5 V to 15 V. The performance of the device varies over this wide operating range. There are some important considerations when operated near the boundary limits. This section offers guidance in selecting the optimum components depending on the application and operating conditions.

- **A Select soft-start capacitor**
- **B Output On/Off Deadlock**
- **C Synchronization CLK option**
- **D Power Good**

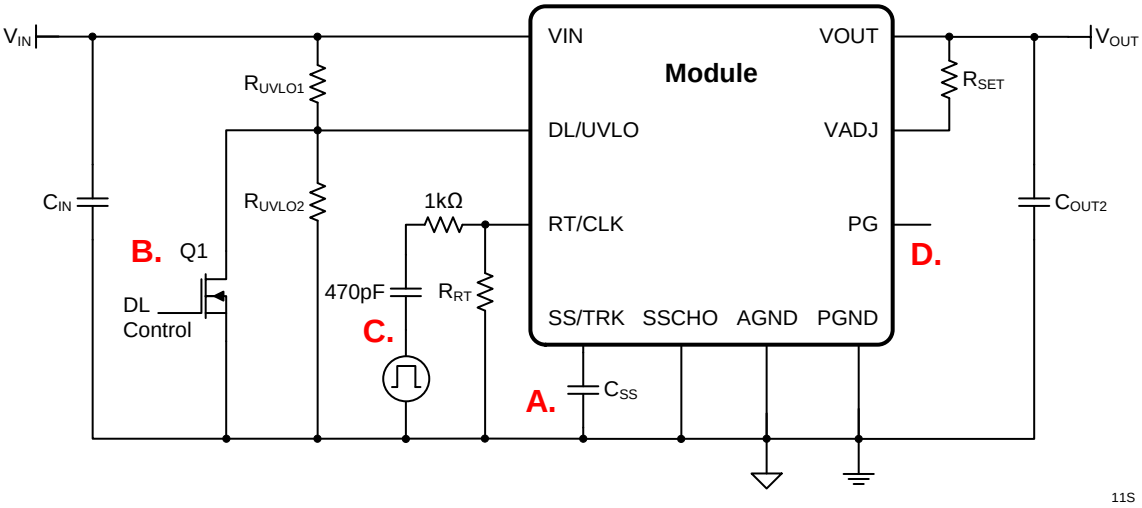


Figure 6. Schematic for optional functions

Step A. Select soft-start capacitor (C_{SS})
For output voltages of 5 V or less, the slow start capacitance built into the MagI³C Power Module is sufficient for a turn-on ramp rate that does not induce large surge currents while charging the output capacitors. Connecting the SSCHO pin (Pin 29) to AGND while leaving SS pin (Pin 28) open enables the internal SS capacitor with a slow start interval of approximately 5ms. For output voltages higher than 5 V, additional a slow start capacitance is recommended. For 12 V to 15 V output voltages, a 22 nF capacitor should be connected between the SS/TRK pin (Pin 28) and AGND, while connecting the SSCHO pin (Pin 29) to AGND as well. Figure 7 shows an additional SS capacitor connected to the SS pin and the SSCHO pin connected to AGND. See Table 5 below for SS capacitor values and timing interval.

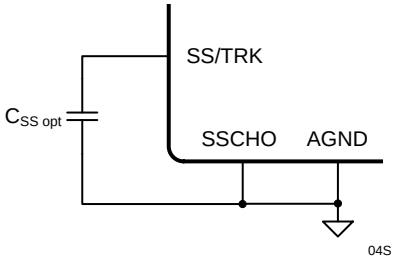


Figure 7. Soft-Start Capacitor Css and SSCHO connection

Table 5: Recommended Soft-Start Capacitors for typical Start times

Soft Start Time	Capacitor C_{SS}
5msec	Open
7msec	4.7nF
10msec	10nF
13msec	15nF
17msec	22nF

Step B. Output On/Off Deadlock (DL)
The DL pin provides electrical on/off control of the device. Once the DL pin voltage exceeds the threshold voltage, the device starts operation. If the DL pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low quiescent current state.
The DL pin has an internal pull-up current source, allowing the user to float the DL pin for enabling the device. If an application requires controlling the DL pin, use an open drain/collector device, or a suitable logic gate to interface with the pin.
Figure 8 shows the typical application of the deadlock function. The deadlock control has its own internal pull-up to V_{IN} potential. An open-collector or open-drain device is recommended to control this input.

Turning Q1 on applies a low voltage to the deadlock control (DL) pin and disables the output of the supply, shown in Figure 10. If Q1 is turned off, the supply executes a soft-start power-up sequence, as shown in Figure 9. A regulated output voltage is produced within 5 ms.

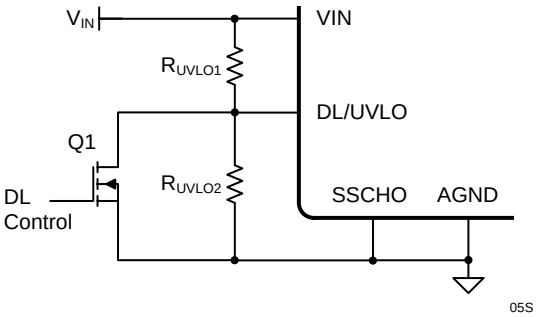


Figure 8. Typical Deadlock Control

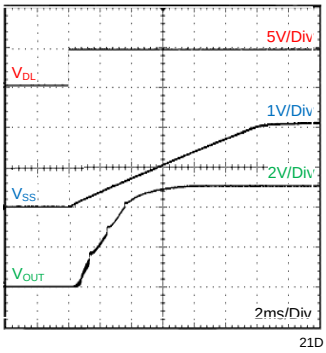


Figure 9. Deadlock start-up I_{OUT} = 2A

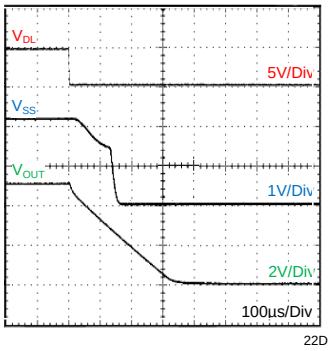


Figure 10. Deadlock shut-down I_{OUT} = 2A

Step C. Synchronization CLK option
An internal phase locked loop (PLL) allows synchronization between 300 kHz and 1 MHz, and to easily switch from RT mode to CLK mode. To implement the synchronization feature, connect a square wave clock signal to the RT/CLK pin with a duty cycle between 20 % to 80 %. The clock signal amplitude must transition lower than 0.8 V and higher than 2.0 V. The start of the switching cycle is synchronized to the falling edge of RT/CLK pin. In applications where both RT mode and CLK mode are needed, the device can be configured as shown in Figure 11.
Before the external clock is present, the device works in RT mode where the switching frequency is set by the R_{RT} resistor. When the external clock is present, the CLK mode overrides the RT mode. The first time the CLK pin is pulled above the RT/CLK high threshold (2.0 V), the device switches from RT mode to CLK mode and the RT/CLK pin becomes high impedance as the PLL starts to lock onto the frequency of the external clock. It is not recommended to switch from CLK mode back to RT mode because the internal switching frequency drops to 100 kHz first before returning to the switching frequency set by the R_{RT} resistor.

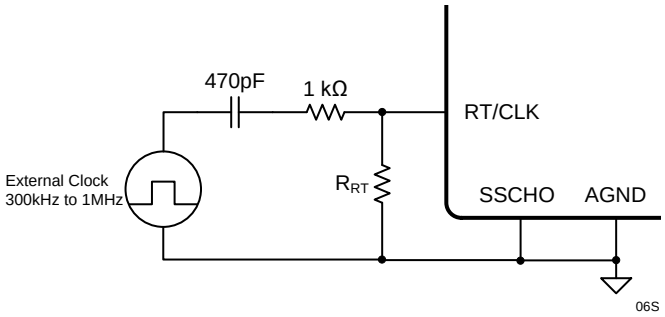


Figure 11. Synchronization Configuration

Step D. Power Good (PG)
The PG pin is an open drain output. Once the output voltage is between 94 % and 106 % of the set voltage, the PG pin pull-down is released and the pin floats. The recommended pull-up resistor value is between 10 kΩ and 100 kΩ to a voltage source that is 5.5 V or less. The PG pin is in a defined state once V_{IN} is higher than 1.0 V, but with reduced current sinking capability. The PG pin achieves full current sinking capability once the V_{IN} pin is above 4.5 V. The PG pin is pulled low when the output voltage is lower than 91 % or higher than 109 % of the nominal set voltage. Also, the PG pin is pulled low if the input UVLO or thermal shutdown is asserted, the DL pin is pulled low, or the SS/TRK pin is below 1.4 V.

N3 MagI³C inherent Characteristics:

The MagI³C Power Module can operate over a wide input voltage range of 7 V to 50 V and produce output voltages from 2.5 V to 15 V. The performance of the device varies over this wide operating range. There are some important considerations when operated near the boundary limits. This section offers guidance in selecting the optimum components depending on the application and operating conditions.

- **E Input voltage**
- **F Power up characteristic**
- **G Light load behaviour**
- **H EMI**

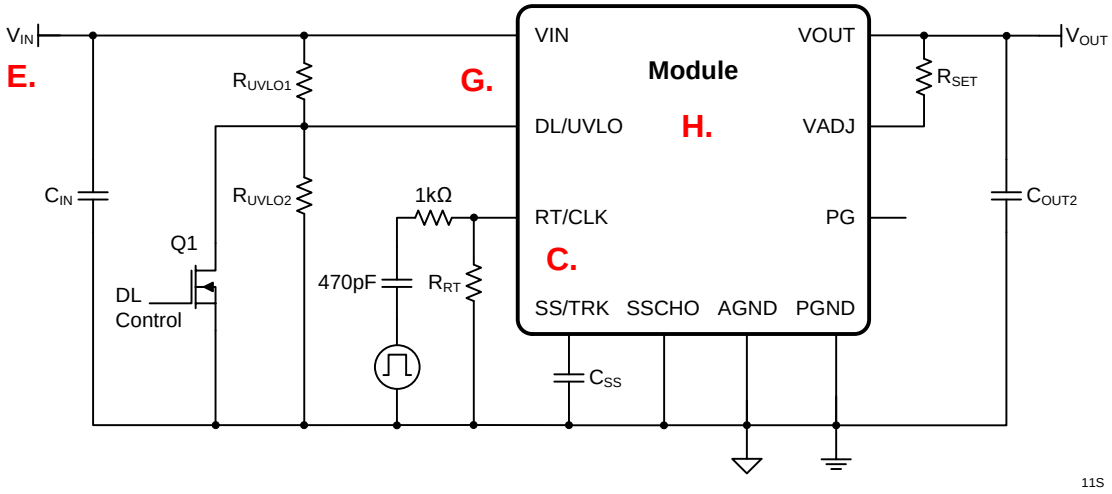


Figure 12. Schematic for inherent Characteristics

Step E. Input Voltage (V_{IN})
The MagI³C Power Module operates over the input voltage range of 7 V to 50 V. For reliable start-up and operation at light loads, the minimum input voltage depends on the output voltage. For output voltages ≤ 12 V, the minimum input voltage is 7 V or (V_{OUT} + 3 V), whichever is higher. For output voltages > 12 V, the minimum input voltage is (1.33 x V_{OUT}).
The maximum input voltage is (15 x V_{OUT}) or 50 V, whichever is less. While the device can safely handle input surge voltages up to 65 V, sustained operation at input voltages above 50 V is not recommended. See the Step 2. Under voltage Lockout (UVLO) Threshold section of this datasheet for more information.

Step F. Power-Up Characteristics
When configured as shown in the typical application on the front page, the MagI³C Power Module produces a regulated output voltage following the application of a valid input voltage. During the power-up, internal soft-start circuitry slows the rate that the output voltage rises, thereby limiting the amount of in-rush current that can be drawn from the input source. The soft-start circuitry introduces a short time delay from the point that a valid input voltage is recognized. Figure 13 shows the start-up waveforms for a MagI³C Power Module, operating from a 24 V input and the output voltage adjusted to 5 V.

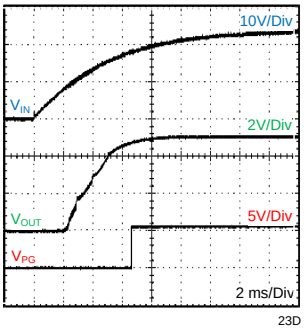


Figure 13. Startup V_{IN}=10V; I_{OUT}=2A

Step G. Light load behaviour

The MagI³C Power Module is a non-synchronous converter. One of the characteristics of a non-synchronous converter is that as the load current on the output is decreased, a point is reached where the energy delivered by a single switching pulse is more than the load can absorb. This causes the output voltage to rise slightly. This rise in output voltage is sensed by the feedback loop and the device responds by skipping one or more switching cycles until the output voltages falls back to the set point. At very light loads or no load, many switching cycles are skipped. The observed effect during this pulse skipping mode of operation is an increase in the peak to peak ripple voltage, and a decrease in the ripple frequency. The load current at which pulse skipping begins is a function of the input voltage, the output voltage, and the switching frequency. A plot of the pulse skipping threshold current as a function of input voltage is given in Figure 14 for a number of popular output voltage and switching frequency combinations.

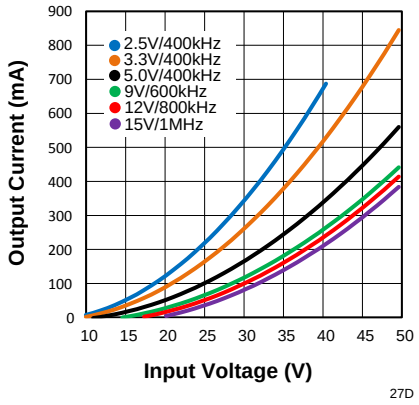


Figure 14. Pulse Skipping Load Threshold

Step H. Electromagnetic Interference

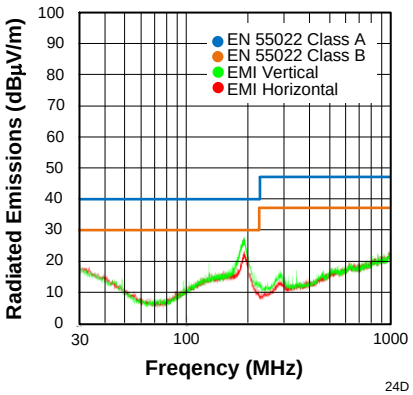


Figure 15. Radiated Emissions EN55022 complaint: V_{IN} = 24V; V_{OUT} = 5V ; Load 2A

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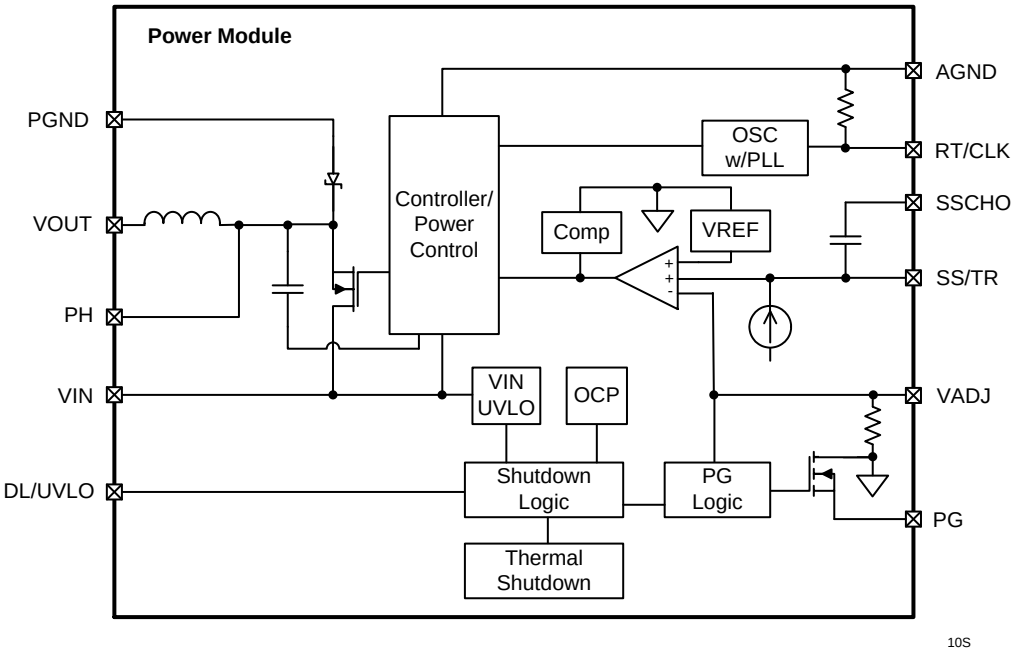
MagI³C Power Module Product Family
VDRM - Variable Step Down Regulator Module

O BLOCK DIAGRAM



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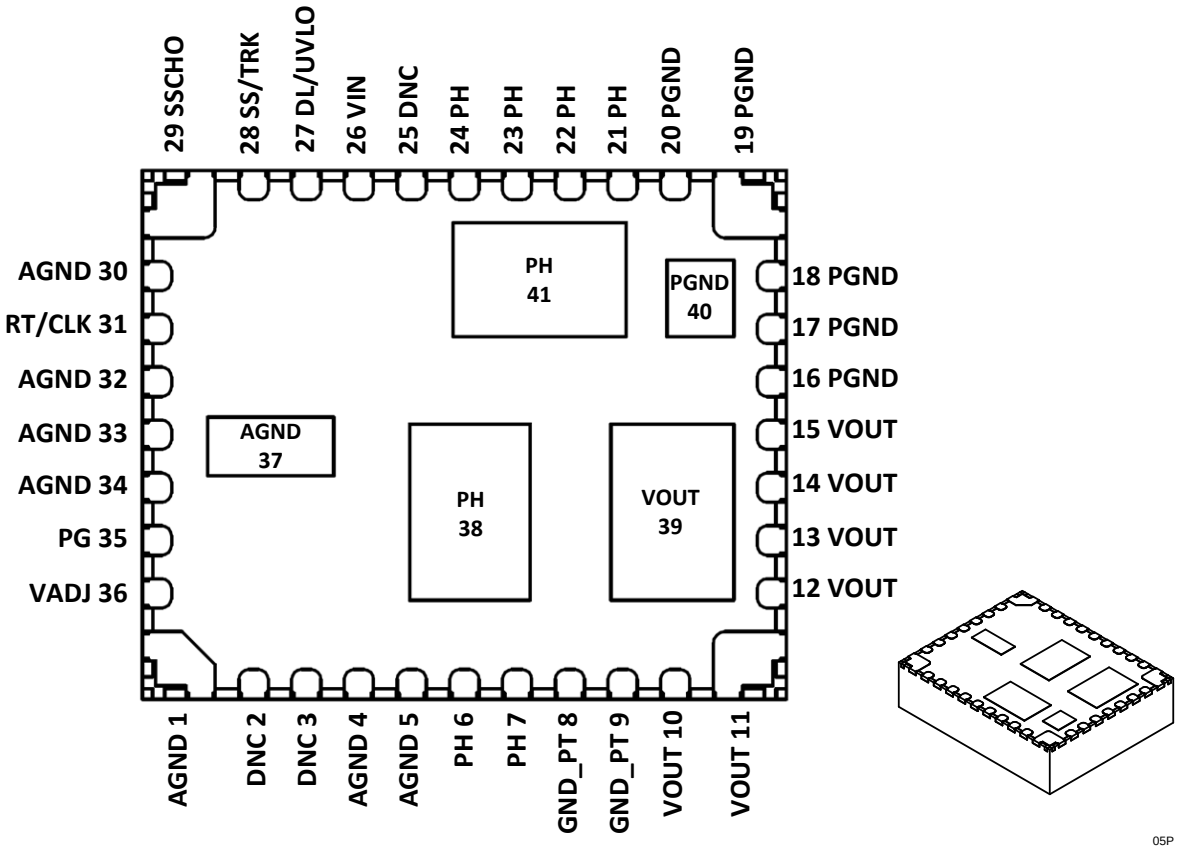
MagI³C Power Module Product Family
VDRM - Variable Step Down Regulator Module

P PIN CONFIGURATION



Bottom view mirrored BQFN 41 (page 22 detail PIN description)

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MagI³C Power Module Product Family
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Q DETAILED PIN DESCRIPTION

PIN #	PIN SYMBOL	PIN DESCRIPTION
26	VIN	1I Input voltage. This pin supplies all power to the converter. Connect this pin to the input supply and connect bypass capacitors between this pin and PGND.
10, 11, 12, 13, 14, 15, 39	VOUT	2I Output voltage. These pins are connected to the internal output inductor. Connect these pins to the output load and connect external bypass capacitors between these pins and PGND. Connect a resistor from these pins to VADJ to set the output voltage.
1, 4, 5, 30, 32, 33, 34, 37	AGND	3I These pins are connected to the internal analog ground (AGND) of the device. This node should be treated as the zero volt ground reference for the analog control circuitry. Pad 37 should be connected to PCB ground planes using multiple vias for good thermal performance. Not all pins are connected together internally. All pins must be connected together externally with a copper plane or pour directly under the module. Connect AGND to PGND at a single point (GND_PT; pins 8 & 9). See Layout Recommendations.
16, 17, 18, 19, 20, 40	PGND	4I This is the return current path for the power stage of the device. Connect these pins to the load and to the bypass capacitors associated with VIN and VOUT. Pad 40 should be connected to PCB ground planes using multiple vias for good thermal performance.
8, 9	GND_PT	5I Ground Point. Connect AGND to PGND at these pins as shown in the Step 6. Layout Considerations. These pins GND_PT are not connected to internal circuitry, and are not connected to one another.
35	PG	6I Power Good flag pin. This open drain output asserts low if the output voltage is more than approximately ±6% out of regulation. A pull-up resistor is required.
36	VADJ	7I Connecting a resistor between this pin and VOUT sets the output voltage.
31	RT/CLK	8I This pin is connected to an internal frequency setting resistor which sets the default switching frequency. An external resistor can be connected from this pin to AGND to increase the frequency. This pin can also be used to synchronize to an external clock.
27	DL/UVLO	9I Deadlock and UVLO adjust pin. Use an open drain or open collector logic device to ground this pin to control the INH function. A resistor divider between this pin, AGND, and VIN sets the UVLO voltage.
28	SS/TRK	10I Slow-start and tracking pin. Connecting an external capacitor to this pin adjusts the output voltage rise time. A voltage applied to this pin allows for tracking and sequencing control.
29	SSCHO	11I Slow-start or track feature select. Connect this pin to AGND to enable the internal SS capacitor. Leave this pin open to enable the TR feature.
6, 7, 21, 22, 23, 24, 38, 41	PH	12I Phase switch node. Do not place any external component on these pins or tie them to a pin of another function.
2, 3, 25	DNC	Do Not Connect. Do not connect these pins to AGND, to another DNC pin, or to any other voltage. These pins are connected to internal circuitry. Each pin must be soldered to an isolated pad.

R PROTECTIVE FEATURES

Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 180 °C typically. The device reinitiates the power up sequence when the junction temperature drops below 165 °C typically.

Overcurrent Protection

For protection against load faults, the MagI³C Power Module incorporates cycle-by-cycle current limiting. During an overcurrent condition the output current is limited and the output voltage is reduced, as shown in Figure 15. As the output voltage drops more than 8% below the set point, the PG signal is pulled low. If the output voltage drops more than 25%, the switching frequency is reduced to reduce power dissipation within the device. When the overcurrent condition is removed, the output voltage returns to the established voltage. The MagI³C Power Module is not designed to endure a sustained short circuit condition. The use of an output fuse, voltage supervisor circuit, or other overcurrent protection circuit is recommended. A recommended overcurrent protection circuit is shown in Figure 16. This circuit uses the PG signal as an indication of an overcurrent condition. As PG remains low, the TLC555 timer operates as a low frequency oscillator, driving the DL/UVLO pin low for approximately 400ms, halting the power conversion of the device. After the inhibit interval, the DL/UVLO pin is released and the MagI³C Power Module restarts. If the overcurrent condition is removed, the PG signal goes high, resetting the oscillator and power conversion resumes, otherwise the inhibit cycle repeats.

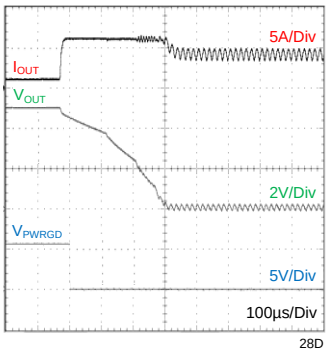

Figure 15. Overcurrent Limiting

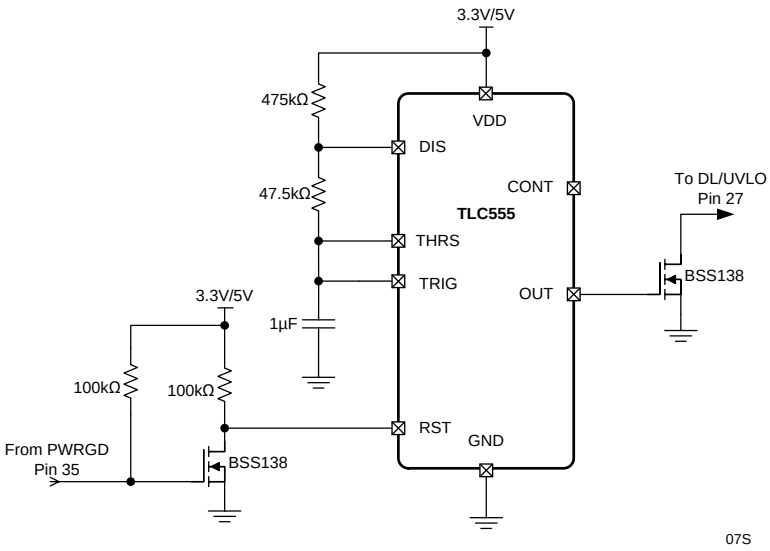

Figure 16. Over-Current Protection Circuit

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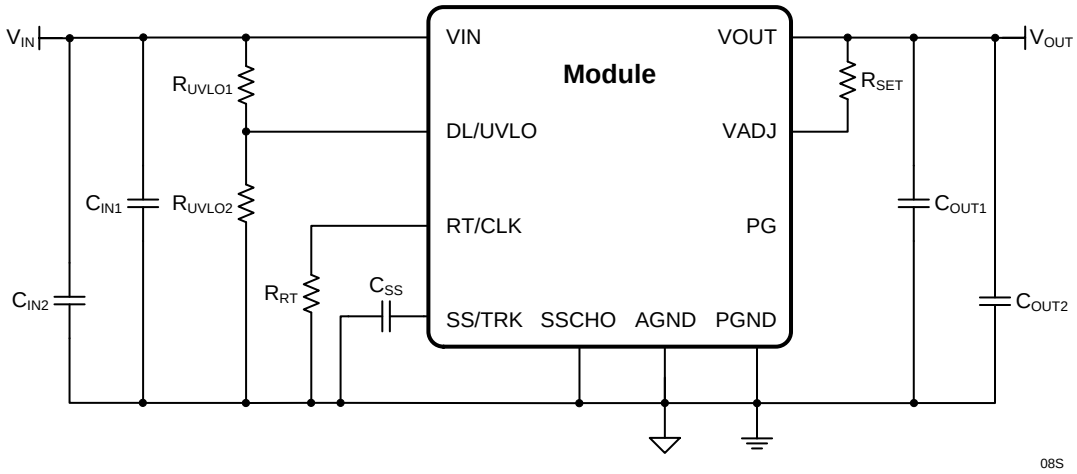
MagI³C Power Module Product Family
VDRM - Variable Step Down Regulator Module

S APPLICATIONS

The MagI³C Power Module for high output voltage is easy-to-use DC-DC solutions capable of driving up to a 2.5A load with exceptional power conversion efficiency, output voltage accuracy, line and load regulation. They are available in an innovative package that enhances thermal performance. Following application circuits show possible operating configurations.

S1 APPLICATION CIRCUIT



S1a Recommended Parameters for Design Example:

Recommended component values: T_A = 25°C

V_{OUT}	3.3V	5V	12V
V_{IN}	7V to 36V	8V to 50V	15V to 50V
R_{SET}	31.6kΩ	52.3kΩ	140kΩ
R_{UVLO1}	174kΩ	174kΩ	174kΩ
R_{UVLO2}	40.2kΩ	31.6kΩ	15.4kΩ
R_{RT}	Open	1.1MΩ	267kΩ
$C_{IN1\ min}$	4.7µF; 50V	2.2µF; 100V	2.2µF; 100V
C_{IN2}	Open	2.2µF; 100V	2.2µF; 100V
$C_{OUT1\ min}$	47µF; 6.3V	47µF; 6.3V	47µF; 16V
C_{OUT2}	47µF; 6.3V	47µF; 6.3V	47µF; 16V
C_{SS}	Open	Open	22nF

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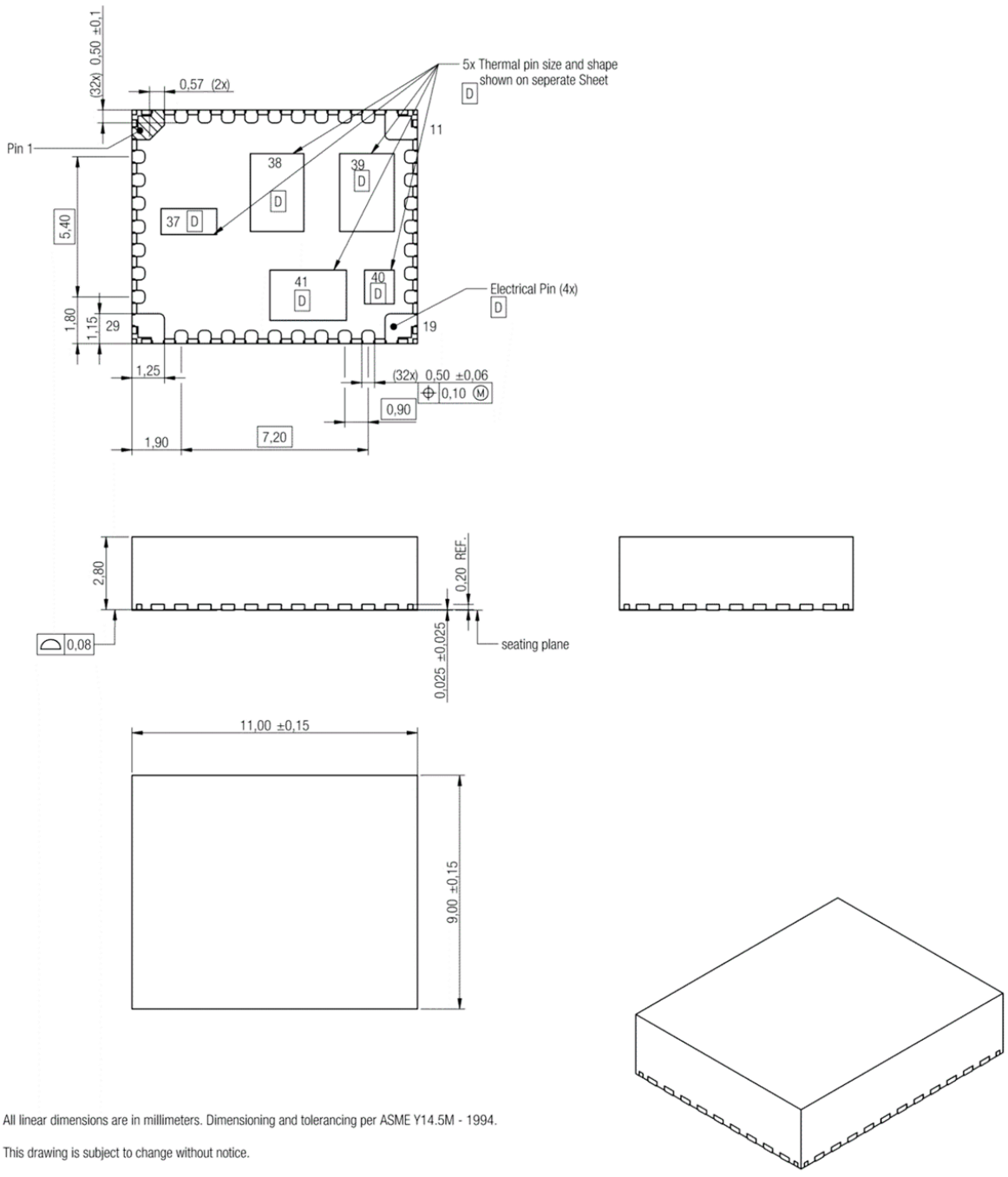
VDRM - Variable Step Down Regulator Module

T PHYSICAL DIMENSIONS (mm)



A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M - 1994.

B. This drawing is subject to change without notice.

C. Quad Flatpack, No-leads (QFN) package configuration.

D. The package thermal must be soldered to the board for thermal and mechanical performance.

E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

F. The package thermal performance may be enhanced by bonding the thermal pad to an external plane.

Scale - 5:1

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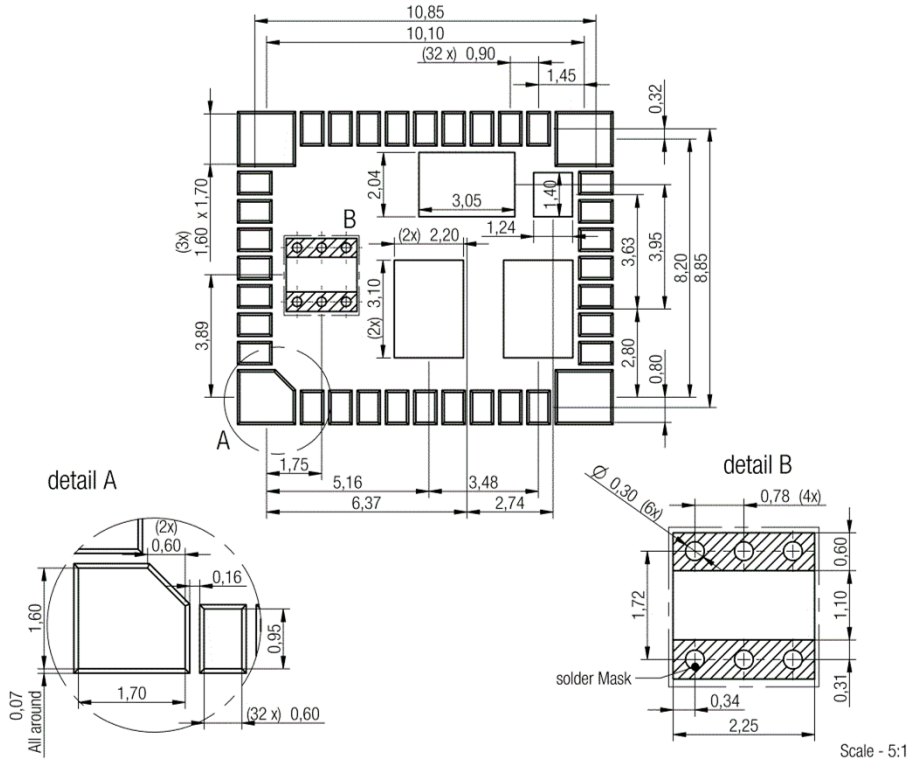

recommended soldering pad
solder past recommendation 150 µm

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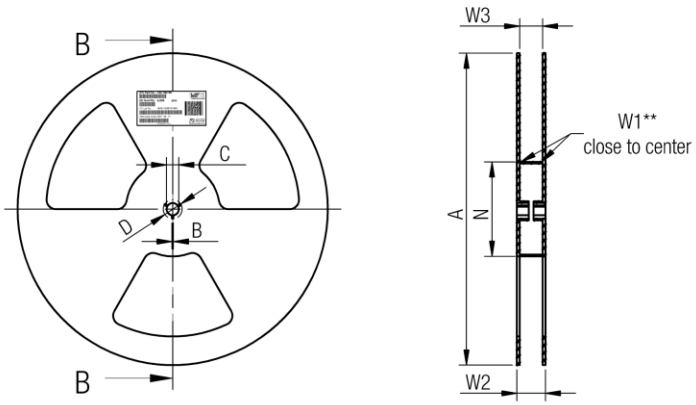
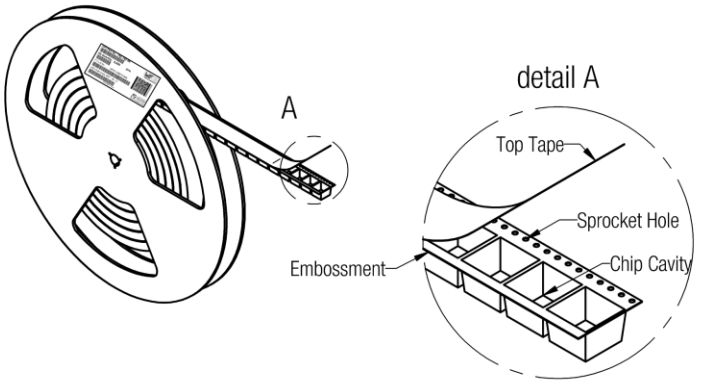
U Packaging

U1 Reel (mm)



		A	B	C	D	N	W1	W2	W3	W3
tolerance		± 2,0	min.	± 0,8	min.	± 2,0	+ 2	max.	min.	max.
Tape width	**24mm**	330,00	1,50	13,00	20,20	60,00	24,40	30,40	23,90	27,40



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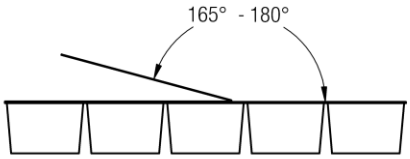
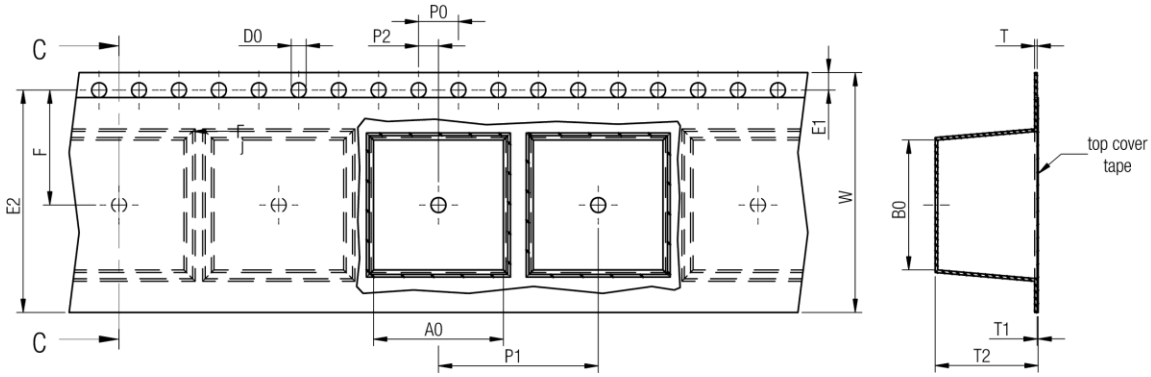
U2 Tape (mm)

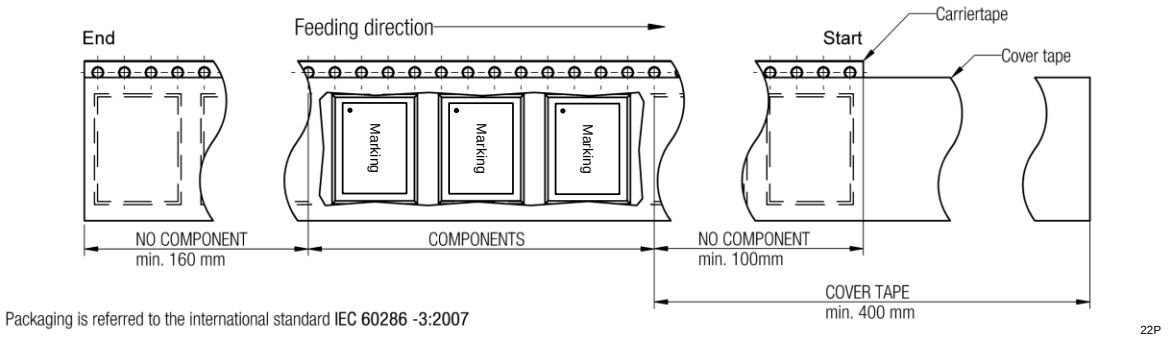


		Pull-of force
Tape width	**24 mm**	0,1 N - 1,3 N

21P



		A0	B0	W	P1	T	T1	T2	D0	E1	E2	F	P0	P2	Tape	VPE / packaging unit
tolerance		±0,1	±0,1	+0,3 -0,1	± 0,1	±0,05	max.	±0,1	±0,05	± 0,1	min.	± 0,05	± 0,1	±0,10		
size	**BQFN-41**	9,35	11,35	24,00	16,00	0,30	0,10	3,10	1,55	1,75	22,25	11,50	4,00	2,00	Polystyrene	250



Packaging is referred to the international standard IEC 60286 -3:2007

22P

V DOCUMENT HISTORY

DOCUMENT HISTORY

Revision	Date	Description	Responsible
0.1	15.04.2014	First draft	Michael Berger

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MagI³C Power Module Product Family
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CAUTIONS AND WARNINGS

The following conditions apply to all goods within the product series of MagI³C of Würth Elektronik eiSos GmbH & Co. KG:

General:
All recommendations according to the general technical specifications of the data-sheet have to be complied with.

The disposal and operation of the product within ambient conditions which probably alloy or harm the component surface has to be avoided.

If the product is potted in customer applications, the potting material might shrink during and after hardening. Accordingly to this the product is exposed to the pressure of the potting material with the effect that the body and termination is possibly damaged by this pressure and so the electrical as well as the mechanical characteristics are endanger to be affected. After the potting material is cured, the body and termination of the product have to be checked if any reduced electrical or mechanical functions or destructions have occurred.

The responsibility for the applicability of customer specific products and use in a particular customer design is always within the authority of the customer. All technical specifications for standard products do also apply for customer specific products.

Washing varnish agent that is used during the production to clean the application might damage or change the characteristics of the body, pins or termination. The washing varnish agent could have a negative effect on the long turn function of the product.
Direct mechanical impact to the product shall be prevented as the material of the body, pins or termination could flake or in the worst case it could break. As these devices are sensitive to electrostatic discharge customer shall follow proper IC Handling Procedures.

Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Würth Elektronik eiSos GmbH & Co. KG components in its applications, notwithstanding any applications-related information or support that may be provided by Würth Elektronik eiSos GmbH & Co. KG. Customer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Customer will fully indemnify Würth Elektronik eiSos and its representatives against any damages arising out of the use of any Würth Elektronik eiSos GmbH & Co. KG components in safety-critical applications.

Product specific:
Follow all instructions mentioned in the datasheet, especially:

- The solder profile has to be complied with according to the technical reflow/ or wave soldering specification, otherwise no warranty will be sustained.
- All products are supposed to be used before the end of the period of 12 months based on the product date-code, if not a 100% solderability can´t be warranted.
- Violation of the technical product specifications such as exceeding the absolute maximum ratings will result in the loss of warranty.
- It is also recommended to return the body to the original moisture proof bag and reseal the moisture proof bag again.
- ESD prevention methods need to be followed for manual handling and processing by machinery.

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IMPORTANT NOTES

The following conditions apply to all goods within the product range of Würth Elektronik eiSos GmbH & Co. KG:

1. General Customer Responsibility
Some goods within the product range of Würth Elektronik eiSos GmbH & Co. KG contain statements regarding general suitability for certain application areas. These statements about suitability are based on our knowledge and experience of typical requirements concerning the areas, serve as general guidance and cannot be estimated as binding statements about the suitability for a customer application. The responsibility for the applicability and use in a particular customer design is always solely within the authority of the customer. Due to this fact it is up to the customer to evaluate, where appropriate to investigate and decide whether the device with the specific product characteristics described in the product specification is valid and suitable for the respective customer application or not. Accordingly, the customer is cautioned to verify that datasheet are current before placing orders.

2. Customer Responsibility related to Specific, in particular Safety-Relevant Applications
It has to be clearly pointed out that the possibility of a malfunction of electronic components or failure before the end of the usual lifetime cannot be completely eliminated in the current state of the art, even if the products are operated within the range of the specifications. In certain customer applications requiring a very high level of safety and especially in customer applications in which the malfunction or failure of an electronic component could endanger human life or health it must be ensured by most advanced technological aid of suitable design of the customer application that no injury or damage is caused to third parties in the event of malfunction or failure of an electronic component.

3. Best Care and Attention
Any product-specific notes, warnings and cautions must be strictly observed.

4. Customer Support for Product Specifications
Some products within the product range may contain substances which are subject to restrictions in certain jurisdictions in order to serve specific technical requirements. Necessary information is available on request. In this case the field sales engineer or the internal sales person in charge should be contacted who will be happy to support in this matter.

5. Product R&D
Due to constant product improvement product specifications may change from time to time. As a standard reporting procedure of the Product Change Notification (PCN) according to the JEDEC-Standard inform about minor and major changes. In case of further queries regarding the PCN, the field sales engineer or the internal sales person in charge should be contacted. The basic responsibility of the customer as per Section 1 and 2 remains unaffected.

6. Product Life Cycle
Due to technical progress and economical evaluation we also reserve the right to discontinue production and delivery of products. As a standard reporting procedure of the Product Termination Notification (PTN) according to the JEDEC-Standard we will inform at an early stage about inevitable product discontinuance. According to this we cannot guarantee that all products within our product range will always be available. Therefore it needs to be verified with the field sales engineer or the internal sales person in charge about the current product availability expectancy before or when the product for application design-in disposal is considered. The approach named above does not apply in the case of individual agreements deviating from the foregoing for customer-specific products.

7. Property Rights
All the rights for contractual products produced by Würth Elektronik eiSos GmbH & Co. KG on the basis of ideas, development contracts as well as models or templates that are subject to copyright, patent or commercial protection supplied to the customer will remain with Würth Elektronik eiSos GmbH & Co. KG. Würth Elektronik eiSos GmbH & Co. KG does not warrant or represent that any license, either expressed or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, application, or process in which Würth Elektronik eiSos GmbH & Co. KG components or services are used.

8. General Terms and Conditions
Unless otherwise agreed in individual contracts, all orders are subject to the current version of the “General Terms and Conditions of Würth Elektronik eiSos Group”, last version available at www.we-online.com.