

ATM2N65TD

N-Channel Enhancement Mode Power MOSFET

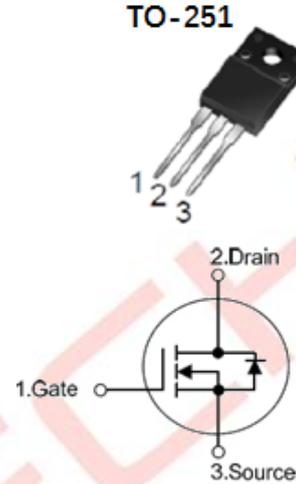
Drain-Source Voltage: 650V Continuous Drain Current: 2A

DESCRIPTION

The ATM2N65TD is a high voltage power MOSFET and is designed to have better characteristics, such as fast switching time, low gate charge, low on-state resistance and have a high rugged avalanche characteristics. This power MOSFET is usually used at high speed switching applications in power supplies, PWM motor controls, high efficient DC to DC converters and bridge circuits.

FEATURES

- ◆ $R_{DS(ON)} < 5.0\Omega$ @ $V_{GS} = 10V$
- ◆ Ultra Low gate charge (typical 45nC)
- ◆ Low reverse transfer capacitance ($C_{RSS} =$ typical 9 pF)
- ◆ Fast switching capability
- ◆ Avalanche energy specified
- ◆ Improved dv/dt capability, high ruggedness



ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT	
Drain-Source Voltage	V _{DSS}	650	V	
Gate-Source Voltage	V _{GSS}	±30	V	
Avalanche Current (Note 2)	I _{AR}	2.0	A	
Drain Current	Continuous	I _D	2.0	A
	Pulsed (Note 2)	I _{DM}	8.0	A
Avalanche Energy	Single Pulsed (Note 3)	E _{AS}	140	mJ
	Repetitive (Note 2)	E _{AR}	4.5	mJ
Peak Diode Recovery dv/dt (Note 4)	dv/dt	4.5	V/ns	
Power Dissipation	TO-251	P _D	28	W
Junction Temperature	T _J	+150	°C	
Operating Temperature	T _{OPR}	-55 ~ +150	°C	
Storage Temperature	T _{STG}	-55 ~ +150	°C	

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating : Pulse width limited by T_J.

3. L=64mH, I_{AS}=2.0A, V_{DD}=50V, R_G=25Ω, Starting T_J = 25°C

4. I_{SD}≤2.4A, di/dt≤200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C

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ELECTRICAL CHARACTERISTICS (T_J = 25°C, unless otherwise specified)

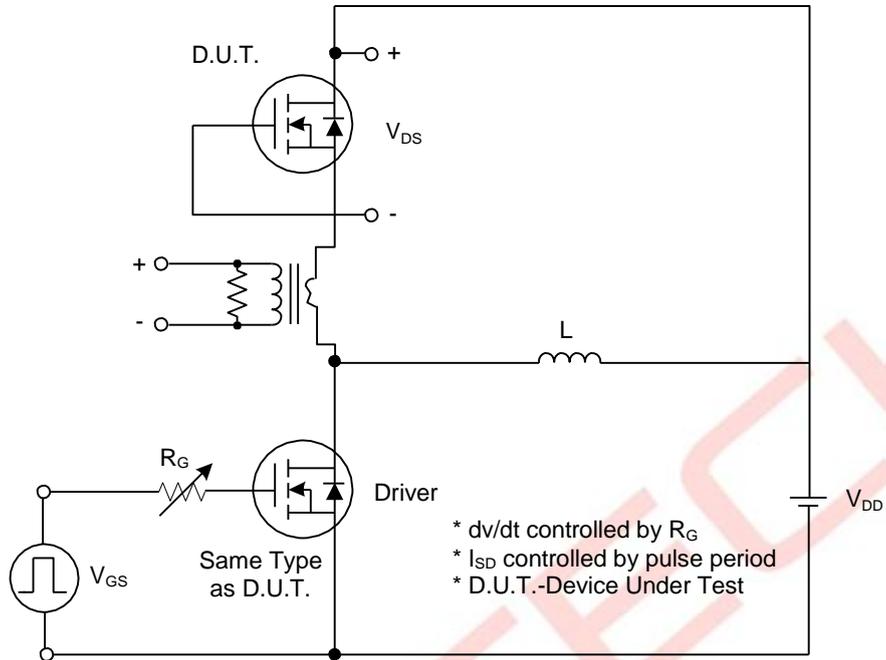
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D = 250μA	650			V
Drain-Source Leakage Current	I _{DSS}	V _{DS} = 650V, V _{GS} = 0V			10	μA
Gate-Source Leakage Current	Forward	V _{GS} = 30V, V _{DS} = 0V			100	nA
	Reverse		V _{GS} = -30V, V _{DS} = 0V			-100
Breakdown Voltage Temperature Coefficient	ΔBV _{DSS} /ΔT _J	I _D = 250μA, Referenced to 25°C		0.4		V/°C
ON CHARACTERISTICS						
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} = V _{GS} , I _D = 250μA	2.0		4.0	V
Static Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} = 10V, I _D = 1A		3.9	5.0	Ω
DYNAMIC CHARACTERISTICS						
Input Capacitance	C _{ISS}	V _{DS} = 25V, V _{GS} = 0V, f = 1MHz		320	370	pF
Output Capacitance	C _{OSS}			40	50	pF
Reverse Transfer Capacitance	C _{RSS}			9	12	pF
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	t _{D(ON)}	V _{DD} = 325V, I _D = 2.4A, R _G = 25Ω (Note 1, 2)		35	50	ns
Turn-On Rise Time	t _R			40	60	ns
Turn-Off Delay Time	t _{D(OFF)}			130	160	ns
Turn-Off Fall Time	t _F			40	60	ns
Total Gate Charge	Q _G	V _{DS} = 520V, V _{GS} = 10V, I _D = 2.4A (Note 1, 2)		45	55	nC
Gate-Source Charge	Q _{GS}			4		nC
Gate-Drain Charge	Q _{GD}			8.4		nC
DRAIN-SOURCE DIODE CHARACTERISTICS						
Drain-Source Diode Forward Voltage	V _{SD}	V _{GS} = 0 V, I _{SD} = 2.0 A			1.4	V
Continuous Drain-Source Current	I _{SD}				2.0	A
Pulsed Drain-Source Current	I _{SM}				8.0	A
Reverse Recovery Time	t _{rr}	V _{GS} = 0 V, I _{SD} = 2.4A,		180		ns
Reverse Recovery Charge	Q _{RR}	di/dt = 100 A/μs (Note1)		0.72		μC

Notes: 1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%

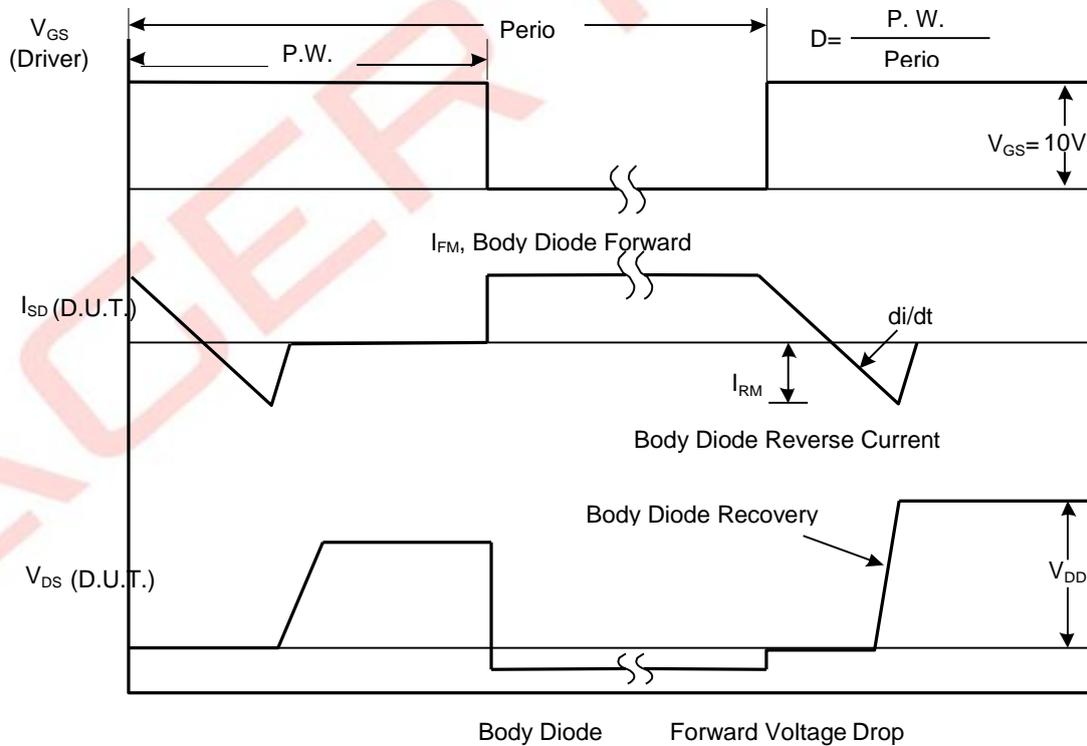
2. Essentially independent of operating temperature

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TEST CIRCUITS AND WAVEFORMS



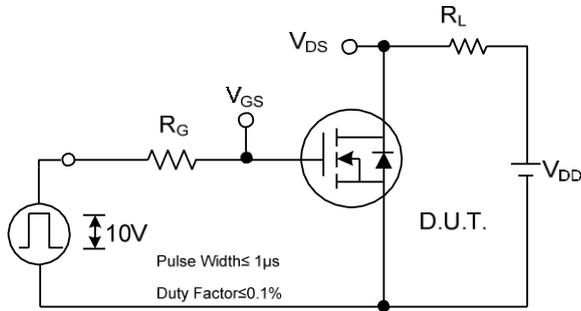
Peak Diode Recovery dv/dt Test Circuit



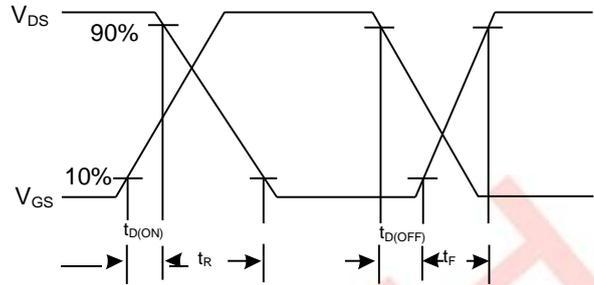
Peak Diode Recovery dv/dt Waveforms

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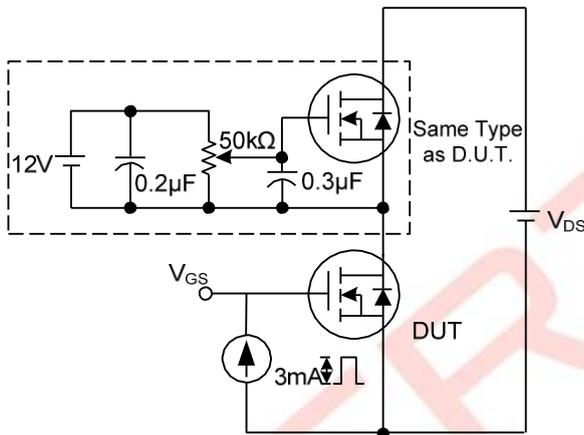
TEST CIRCUITS AND WAVEFORMS (Cont.)



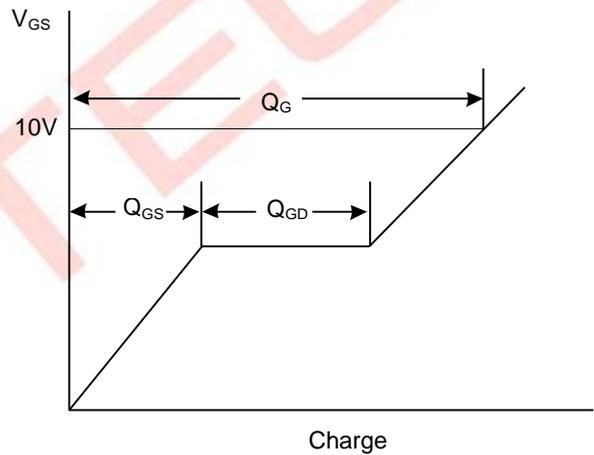
Switching Test Circuit



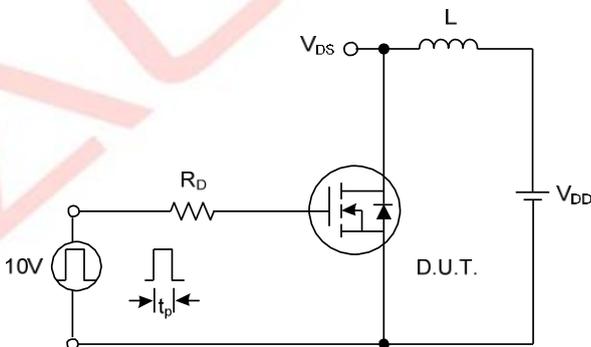
Switching Waveforms



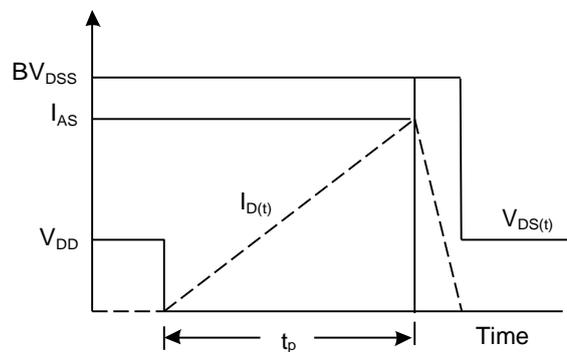
Gate Charge Test Circuit



Gate Charge Waveform



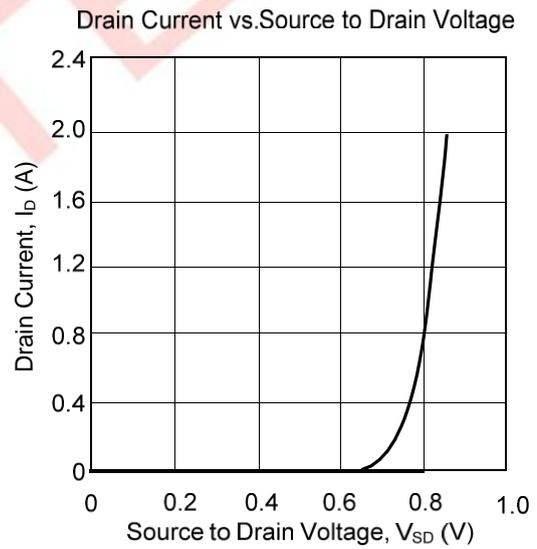
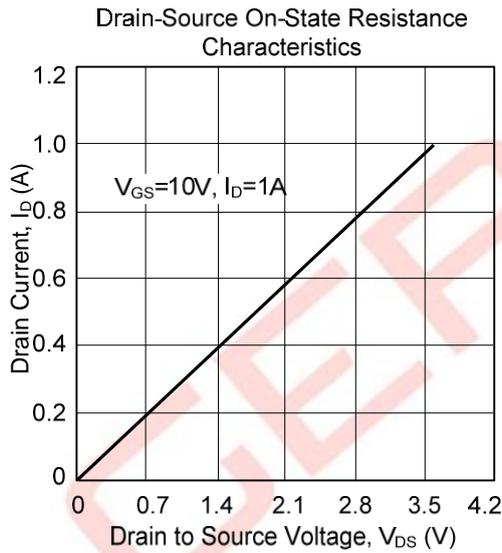
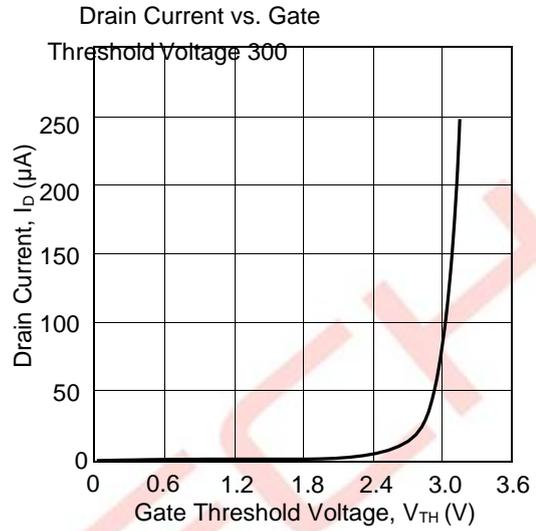
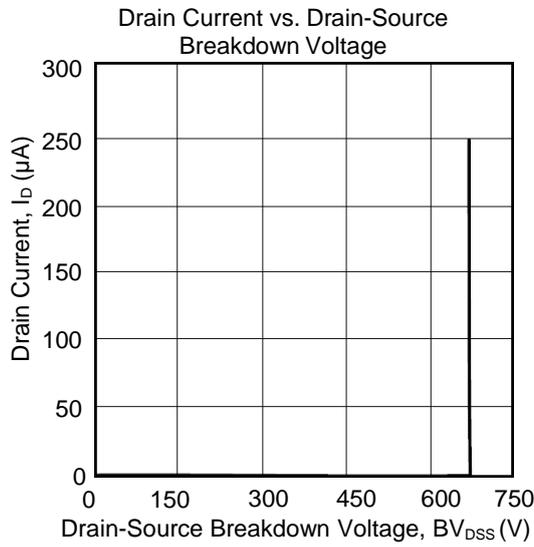
Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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TYPICAL CHARACTERISTICS CURVES



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Package Outline

TO-251

