BK3437 Datasheet

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1. Features

Bluetooth Low Energy

- Bluetooth 5.2 Low Energy (LE)
- Supports Bluetooth LE 1 Mbps and 2 Mbps
- TX power up to +10 dBm
- RX sensitivity -96 dBm

Core

- 32-bit MCU at 32 MHz
- UART Flash download
- JTAG debug interface

Memory

- 2 Mbit SiP Flash
- 32 KB RAM
- 32 KB ROM

Clock Management

- External oscillator: 16 MHz crystal oscillator (XTALH), 32.768 kHz crystal oscillator (XTALL)
- Internal oscillator: 32 kHz ring oscillator (ROSC)
- 32/48 MHz PLL (DPLL)

Power Management

- 1.7 to 3.6 V VBAT supply
- On-chip Power-On Reset (POR) and Brown-Out Detector (BOD)
- Embedded LDO regulators
- Low power consumption:
  - Active mode RX: 10.5 mA
  - Active mode TX: 15 mA
  - Normal sleep mode: 10.4 µA
  - Low-voltage sleep mode: 3.6 µA
  - Deep sleep mode: 0.6 µA

- Shutdown mode: 0.4 μA

Peripherals

- 20 GPIOs
- 1x SPI
- 2x UART: 1 with flash download support
- 1x I2C
- 1x general-purpose DMA controller (GDMA) with 5 channels
- 6x 32-bit PWM channel
- 1x I2S
- 12-bit AUX ADC, up to 8 channels
- 6x 32-bit general-purpose timer
- 2x watchdog timer (WDT)
- 1x real-time counter (RTC)
- 1x IrDA
- 1x temperature sensor

Packaging

- QFN32 package, 4 x 4 mm
- Operating temperature range: -40 up to +125 °C

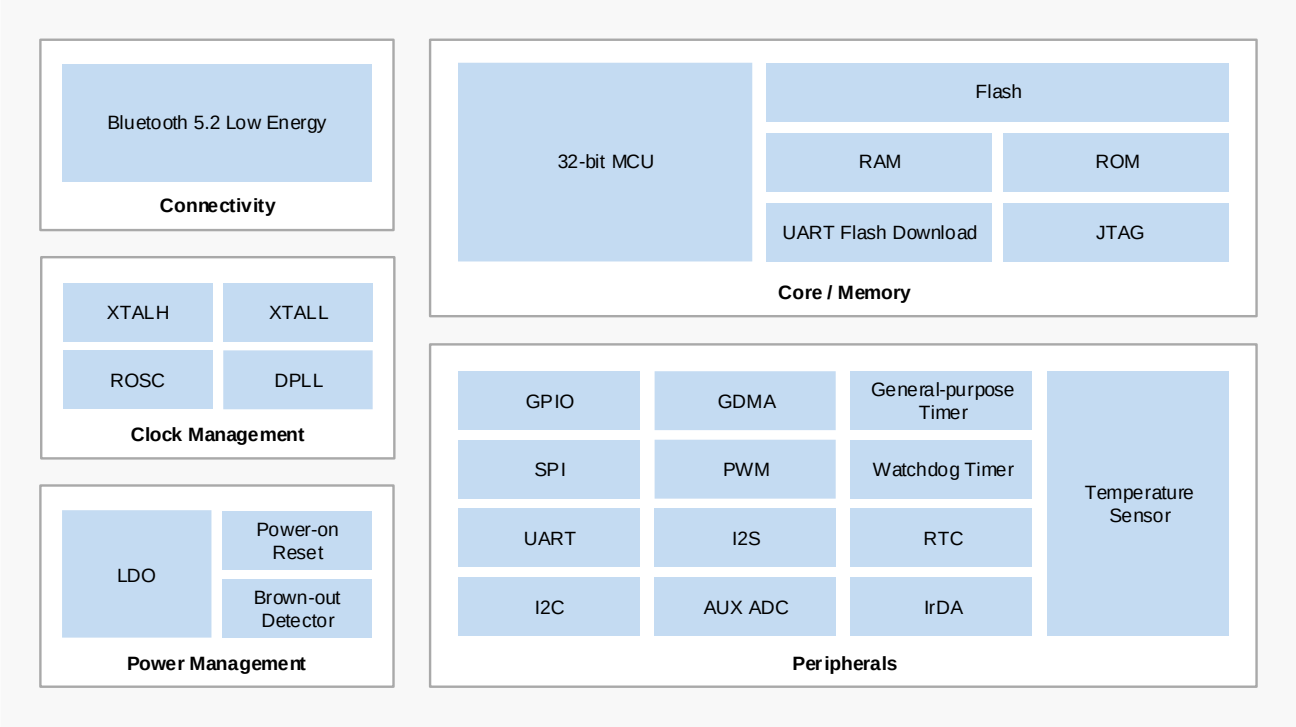
2. Overview

The BK3437 is a highly integrated single-chip Bluetooth 5.2 Low Energy (LE) system-on-chip (SoC). It integrates a high-performance Bluetooth RF transceiver, a feature-rich baseband processor, a memory controller, multiple analog and digital peripherals, and Bluetooth protocol stacks.

Using advanced design techniques and ultra-low power process technology, the BK3437 delivers high integration and minimal power consumption for a wide range of IoT (Internet of Things) applications such as voice remotes and smart lighting.

Figure 2-1 shows the general block diagram of BK3437.

Figure 2-1 BK3437 Block Diagram



3. Pin Description

The BK3437 provides Bluetooth LE functionality in a 4 x 4 mm, 32-pin QFN package.

3.1 QFN32 Pin Description

Figure 3-1 shows the pin assignments of the QFN32 package.

Figure 3-1 QFN32 Pin Assignments

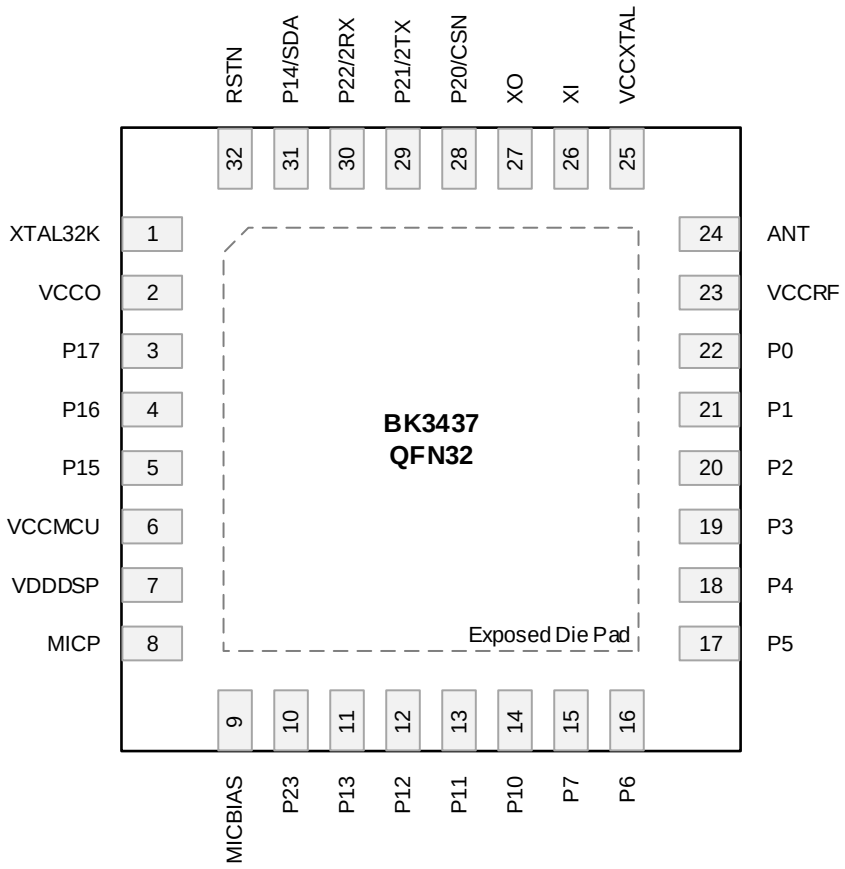


Table 3-1 shows the pin descriptions of the QFN32 package.

Table 3-1 QFN32 Pin Descriptions

Pin #	Name	I/O	Type	Description
1	XTAL32K	-	Analog input	32.768 kHz crystal input
2	VCCO	-	Power	Analog power supply

Pin #	Name	I/O	Type	Description
3	P17	I/O	Digital	• GPIO17: general-purpose I/O • SPI_MISO: master in slave out
4	P16	I/O	Digital	• GPIO16: general-purpose I/O • SPI_MOSI: master out slave in
5	P15	I/O	Digital	• GPIO15: general-purpose I/O • SPI_SCK: serial clock
6	VCCMCU	-	Power	MCU power supply
7	VDDDSP	-	Analog output	Digital LDO output
8	MICP	-	Analog input	Microphone positive input
9	MICBIAS	-	Analog output	Microphone bias output
10	P23	I/O	Digital	• GPIO23: general-purpose I/O • PWMG0_PWM3: PWMG0 channel PWM3 • PWMG1_PWM3: PWMG1 channel PWM3
11	P13	I/O	Digital	• GPIO13: general-purpose I/O • I2C_SCL: serial clock
12	P12	I/O	Digital	• GPIO12: general-purpose I/O • PWMG0_PWM4: PWMG0 channel PWM4
13	P11	I/O	Digital	• GPIO11: general-purpose I/O • PWMG0_PWM5: PWMG0 channel PWM5 • PWMG1_PWM5: PWMG1 channel PWM5
14	P10	I/O	Digital	• GPIO10: general-purpose I/O • PWMG0_PWM3: PWMG0 channel PWM3 • PWMG1_PWM3: PWMG1 channel PWM3
15	P7	I/O	Digital	• GPIO7: general-purpose I/O • SPI_CSN: chip select • PWMG0_PWM2: PWMG0 channel PWM2 • I2S_MCLK: master clock

Pin #	Name	I/O	Type	Description
				• JTAG_TMS: test mode select
16	P6	I/O	Digital/Analog	• GPIO6: general-purpose I/O • DL_SCK: SCK (SPI flash download) • SPI_MISO: master in slave out • PWMG1_PWM3: PWMG1 channel PWM1 • CLK_OUT: 16 MHz clock output (divide by 1/2/4/8) • ADC5: analog input channel • JTAG_TCK: test clock
17	P5	I/O	Digital/Analog	• GPIO5: general-purpose I/O • SPI_MOSI: master out slave in • PWMG0_PWM0: PWMG0 channel PWM0 • I2S_SYNC: frame synchronization • ADC4: analog input channel • JTAG_TDO: test data output
18	P4	I/O	Digital/Analog	• GPIO4: general-purpose I/O • SPI_SCK: serial clock • I2S_CLK: serial clock • ADC3: analog input channel • JTAG_TDI: test data input
19	P3	I/O	Digital/Analog	• GPIO3: general-purpose I/O • I2C_SDA: serial data • UART1_RX: receive data input • I2S_DOUT: serial data output • ADC2: analog input channel
20	P2	I/O	Digital/Analog	• GPIO2: general-purpose I/O • I2C_SCL: serial clock • UART1_TX: transmit data output • I2S_DIN: serial data input • ADC1: analog input channel • IRDA: infrared data
21	P1	I/O	Digital/Analog	• GPIO1: general-purpose I/O • DL_UART_RX: UART Flash download receive data input

Pin #	Name	I/O	Type	Description
				• UART0_RX: receive data input • ADC0: analog input channel
22	P0	I/O	Digital	• GPIO0: general-purpose I/O • DL_UART_TX: UART Flash download transmit data output • UART0_TX: transmit data output
23	VCCRF	-	Power	RF power supply
24	ANT	-	RF	2.4 GHz RF signal port
25	VCCXTAL	-	Power	Crystal power supply
26	XI	-	Analog input	16 MHz crystal input
27	XO	-	Analog output	16 MHz crystal output
28	P20	I/O	Digital	• GPIO20: general-purpose I/O • SPI_CSN: chip select
29	P21	I/O	Digital	• GPIO21: general-purpose I/O • UART1_TX: transmit data output
30	P22	I/O	Digital	• GPIO22: general-purpose I/O • UART1_RX: receive data input
31	P14	I/O	Digital	• GPIO14: general-purpose I/O • I2C_SDA: serial data
32	RSTN	-	Digital input	Reset input, active low
Die pad	GND_SLUG	-	GND	Ground

3.2 Pin Multiplexing

Table 3-2 shows the pin mux functions of GPIOs.

Table 3-2 Pin Multiplexing

GPIO	Flash Download	Alternate Functions					Additional Function
		AF1	AF2	AF3	AF4	AF5	Analog1
	UART	UART0/I2C/SPI/ UART1/PWM	UART1/PWM/ I2C/SPI/	I2S/Clock	AUX ADC	JTAG	IrDA
GPIO0	DL_UART_TX	UART0_TX					
GPIO1	DL_UART_RX	UART0_RX			ADC0		
GPIO2		I2C_SCL	UART1_TX	I2S_DIN	ADC1		IRDA
GPIO3		I2C_SDA	UART1_RX	I2S_DOUT	ADC2		
GPIO4		SPI_SCK		I2S_CLK	ADC3	JTAG_TDI	
GPIO5		SPI_MOSI	PWMG0_PWM0	I2S_SYNC	ADC4	JTAG_TDO	
GPIO6		SPI_MISO	PWMG0_PWM1/ PWMG1_PWM1	CLK_OUT	ADC5	JTAG_TCK	
GPIO7		SPI_CSN	PWMG0_PWM2	I2S_MCLK		JTAG_TMS	
GPIO10			PWMG0_PWM3/ PWMG1_PWM3				
GPIO11			PWMG0_PWM5/ PWMG1_PWM5				
GPIO12			PWMG0_PWM4				
GPIO13			I2C_SCL				
GPIO14			I2C_SDA				
GPIO15			SPI_SCK				
GPIO16			SPI_MOSI				
GPIO17			SPI_MISO				
GPIO20			SPI_CSN				
GPIO21		UART1_TX					
GPIO22		UART1_RX					
GPIO23		PWMG0_PWM3/ PWMG1_PWM3					

4. Functional Description

4.1 RF Transceiver

The BK3437 integrates a high-performance Bluetooth LE transceiver. The incorporated low noise amplifier (LNA) amplifies the single-ended inputs and converts the amplified signals into differential outputs to achieve a better noise and linearity trade-off. On the transmit side, the differential outputs of the power amplifier (PA) are combined and converted to single-ended outputs using the on-chip balun, enabling transmit and receive operations with only one ANT pin connected to the antenna. The device is able to output +10 dBm of transmit output power, allowing users to develop a LE class 1.5 (+10 dBm) device with small printed circuit board (PCB) antennas. The frequency synthesizer is fully integrated, eliminating the need for any external components.

4.2 Bluetooth Baseband

The BK3437 Bluetooth baseband implements the Bluetooth 5.2 modem, providing Low Energy (LE) 1 Mbps and 2 Mbps data rate.

Table 4-1 Bluetooth Modulation Format

Data Rate	Modulation	Bits/Symbol
LE: 1 Mbps	GFSK	1
LE: 2 Mbps	GFSK	1

The Bluetooth baseband utilizes a combination of hardware blocks and firmware for the frequency hopping sequence generator, access code generation, detection and correlation, encryption and decryption for security, forward error correction, 16-bit CRC, packet construction, as well as Bluetooth clocks and timers to optimize power consumption and user programmability.

4.3 Beken Bluetooth Stack

The BK3437 comes with Bluetooth LE 5.2 compliant protocol stacks running on the internal 32-bit RISC MCU. The SoC also runs the application, eliminating the need for an external host controller. An external host can be connected via the UART interface for debugging, but is not required to run the application. Beken provides a development kit that customers can use to configure their applications. The development kit includes software configuration tools and reference software code. If you are interested, please contact your local Beken representative for more information.

4.4 Clock Management

The primary clock sources available in the BK3437 are as follows:

- 16 MHz crystal oscillator: it outputs clock signal XTALH
- 32 kHz crystal oscillator: it outputs clock signal XTALL
- 32 kHz internal ring oscillator (ROSC): it outputs clock signal CLK_ROSC
- Digital PLL (DPLL): it generates 32 MHz clock and 48 MHz clock

The system generates a low-power clock source CLK32K for standby. The CLK32K can be selected from the following clocks:

- 32 kHz crystal oscillator XTALL
- 32 kHz internal oscillator ROSC
- 32 kHz clock signal derived from 16 MHz crystal oscillator

The BK3437 also has a clock output capability, which allows clock signals to be output to external components through GPIOs. GPIO6 can output the following clock signal:

- CLK_OUT: 16 MHz clock output (divide by 1/2/4/8)

4.5 Reset

A reset can be triggered by the following sources: power-on reset, brown-out reset, watchdog reset, low level on RSTN pin (external reset), software reset, and wake-up from shutdown mode or deep sleep mode.

System power-on, digital power-on, and watchdog resets have the same reset effect on major blocks, except for the always-on logic. Any of these three resets can reset the whole chip to its initial state. The always-on logic has a 32-bit timer and 32-bit retention registers, which can only be reset to initial values by a system power-on reset.

Wake-up from either shutdown mode or deep sleep mode will power on digital from power-down mode, which triggers the whole system reset procedure.

4.6 Power Management

4.6.1 Power Scheme

The power management system on BK3437 includes several internal LDO regulators to provide voltage and noise isolation to various parts of the chip.

The BK3437 is powered by an external VBAT power supply ranging from 1.7 to 3.6 V through VCC pins. VCC pins refer to any pins among VCCO pin, VCCMCU pin, VCCRF pin, and VCCXTAL pin.

Note: Outputs from the LDO regulators require proper bypass capacitors to reduce supply noise. Please refer to BK3437 EVB User Guide and the application note for more details about choosing the proper bypass capacitors.

4.6.2 Power Modes

The BK3437 supports four low-power modes except active mode, namely shutdown mode, deep sleep mode, low-voltage sleep mode, and normal sleep mode, where shutdown mode has the lowest power consumption.

Shutdown Mode: All circuits are turned off. An active level applied on any GPIO will bring the system to active mode.

Deep Sleep Mode: All circuits are powered down except the always-on (AON) logic. A GPIO interrupt or an RTC interrupt can power up the system again. Retention registers can keep their contents.

Low-voltage Sleep Mode: The MCU and all digital logic stop their clocks, and their power supply decreases to a much lower retention voltage, which results in a much lower current. GPIO interrupts, RTC interrupts, or interrupts triggered by Bluetooth MAC low-power counter can bring the system back to active mode with normal voltage.

Normal Sleep Mode: The MCU stops running, and all peripheral interrupts can resume the MCU.

Active Mode: The MCU is active, and all peripherals are available.

4.7 General-purpose I/Os (GPIO)

The BK3437 has up to 20 GPIOs, which can be configured as either input or output. All GPIOs are shared with alternate functions. Table 3-2 Pin Multiplexing provides the mux functions of GPIOs.

The main features of GPIOs include:

- Push-pull
- Internal pull-up/down resistors
- Configurable drive strength
- Alternate function
- Interrupt generation:
  - High or low level
  - Rising or falling edge

4.8 SPI Interface (SPI)

The BK3437 integrates an SPI interface that can operate in master or slave mode. The SPI interface allows a clock frequency up to 32 MHz in both master and slave modes.

The SPI interface supports the following features:

- 4-wire or 3-wire full-duplex synchronous communication
- Configurable 8-bit or 16-bit data width
- Programmable clock polarity and phase
- Programmable data order with MSB-first or LSB-first shifting
- Embedded 64-depth RX FIFO and 64-depth TX FIFO with DMA capability

4.9 UART Interface (UART)

The BK3437 includes two universal asynchronous receiver/transmitter (UART) interfaces, which offer full-duplex, asynchronous serial communication at a baud rate up to 2 Mbps.

The UART interfaces offer the features below:

- Configurable data length (5, 6, 7, or 8 bits)
- Even, odd, or none parity check
- Programmable stop bits (1 or 2 bits)
- Each UART embeds a 128-byte TX FIFO and a 128-byte RX FIFO. FIFO mode is disabled by default and can be enabled by software.
- Flash download (UART0)

4.10 I2C Interface (I2C)

I2C is a popular inter-IC interface that requires only two bus lines, the serial data line (SDA) and the serial clock line (SCL). The BK3437 embeds an I2C interface, which can operate in master or slave mode.

The features of the I2C interface are listed below:

- Master and slave modes
- Standard mode (up to 100 kbps)
- Fast mode (up to 400 kbps)
- 7-bit and 10-bit addressing
- Bus idle and SCL low timeout condition detection

4.11 GDMA Controller (GDMA)

The BK3437 has a general-purpose DMA controller (GDMA) with five DMA channels to unload CPU activity. The five channels are shared by peripherals that have DMA capabilities.

The GDMA controller can perform single block transfers and repeated block transfers. Data width for destination and source can be configured as 8 bits (byte), 16 bits (half-word), or 32 bits (word). It allows peripheral to memory, memory to memory, and memory to peripheral data transfers at a high speed.

A selection of peripherals on the BK3437 have DMA capabilities, including SPI, UART0, UART1, I2S, and AUX ADC.

4.12 PWM Group (PWMG)

The BK3437 has two advanced-control PWM groups (PWMG). Each PWMG consists of three independent 32-bit auto-reload counters driven by three programmable prescalers. The PWMGs can generate pulse width modulated signals for a variety of purposes, including input capture, pulse edge counting, or generation of output waveforms (output compare).

The PWMG features are listed here:

- Three 32-bit up, down, or up-and-down auto-reload counters per PWMG
- Three 8-bit programmable prescalers per PWMG capable of dividing the clock frequency of each counter by any factor between 1 and 256
- Six independent channels of two PWMGs for:
  - Input capture
  - Pulse edge counting
  - PWM generation (edge or center-aligned modes)
- Complementary outputs with programmable dead-time and configurable dead-time mode
- Synchronization circuit to control the counter with external signals and to interconnect several counters together
- Repetition counter to update the registers only after a given number of cycles of the counter
- Interrupt generation on the following events:
  - Update: counter overflow or underflow, counter initialization (by software or internal/external trigger)
  - Counter start
  - Input capture
  - Output compare
- Change of polarity, duty cycle, and base frequency on every PWM period
- Supports incremental (quadrature) encoder and Hall-sensor circuitry for positioning purposes

PWM1/3/5 of PWMG0 are multiplexed with PWM1/3/5 of PWMG1. PWMG0_PWM1/3/5 can only be coupled with PWMG0_ PWM0/2/4 to generate coupled waveforms (reverse or identical). Table 4-2 below provides the description of PWM signals.

Table 4-2 PWM Signals

GPIO	PWM Pin Name	Signal Type	Description
PWMG0			
GPIO5	PWMG0_PWM0	I/O	PWMG0 channel PWM0
GPIO6	PWMG0_PWM1	I/O	PWMG0 channel PWM1 PWM1 is coupled with PWM0 (with deadtime insertion) to generate reverse or identical waveforms of PWM0.
GPIO7	PWMG0_PWM2	I/O	PWMG0 channel PWM2
GPIO10/GPIO23	PWMG0_PWM3	I/O	PWMG0 channel PWM3 PWM3 is coupled with PWM2 (with deadtime insertion) to generate reverse or identical waveforms of PWM2.
GPIO12	PWMG0_PWM4	I/O	PWMG0 channel PWM4
GPIO11	PWMG0_PWM5	I/O	PWMG0 channel PWM5 PWM5 is coupled with PWM4 (with deadtime insertion) to generate reverse or identical waveforms of PWM4.
PWMG1			
GPIO6	PWMG1_PWM1	I/O	PWMG1 channel PWM1
GPIO10/GPIO23	PWMG1_PWM3	I/O	PWMG1 channel PWM3
GPIO11	PWMG1_PWM5	I/O	PWMG1 channel PWM5

4.13 I2S Interface (I2S)

The BK3437 integrates an I2S interface that supports slave mode with a sampling rate from 8 kHz to 384 kHz. The I2S interface supports both PCM mono channel and I2S stereo channel modes. The data width can be 1 to 32 bits.

Listed here are the I2S features:

- Slave mode
- Full duplex or half-duplex communication
- Various sampling rates
- 12-bit programmable prescaler

- Programmable clock polarity
- Multiple I2S protocols supported:
  - I2S Philips standard
  - MSB-Justified standard (Left-Justified)
  - LSB-Justified standard (Right-Justified)
  - PCM standard
- Programmable data order with LSB first or MSB first
- Programmable data width between 1 and 32 bits
- Integrated 32-bit RX FIFO and 32-bit TX FIFO, both with a depth of 32 x 3 channels
- Master clock can be output to drive external audio devices.

4.14 Auxiliary ADC (AUX ADC)

The auxiliary ADC (AUX ADC) is a 12-bit sigma-delta (ΣΔ) analog-to-digital converter designed for audio and DC measurements with a sampling rate from 4 kHz to 16 kHz. The ADC consists of a PGA, a sigma-delta modulator, and a digital filter that together produce a high-resolution data-stream output. It is capable of converting analog signals over a wide range of frequencies, from DC to several kilohertz.

The ADC supports six external analog input channels as shown in Table 4-3. It can operate in one-shot or continuous mode.

Table 4-3 AUX ADC Input Channel

Channel Number	Detected Voltage	Description
0	ADC0/temperature sensor	GPIO1 voltage/temperature sensor output voltage
1	ADC1	GPIO2 voltage
2	ADC2	GPIO3 voltage
3	ADC3	GPIO4 voltage
4	ADC4	GPIO5 voltage
5	ADC5	GPIO6 voltage
6	VCC	Monitor battery voltage
7	MICP	Microphone input voltage

4.15 Timer Group (TIMG)

The BK3437 includes two general-purpose timer groups (TIMG). Each group has three 32-bit timers. Each group consists of three 32-bit counters driven by a 4-bit prescaler.

Each TIMG module has the following features:

- Three timers (Timer0/1/2)
- Three 32-bit up counters
- 4-bit prescaler, factor between 1 and 16
- Capable of reading the real-time value of the counter

4.16 Watchdog Timers (WDT)

The BK3437 has two watchdog timers, the main domain watchdog timer (DWDT) and the always-on domain watchdog timer (AWDT). The purpose of the watchdog timers is to detect and recover from failures or malfunctions. The watchdog timers trigger a reset on expiry of a specified time period.

The DWDT runs on the 32 kHz CLK32K clock and has a maximum programmable period up to 32.768 (2^16/2 kHz) seconds. The AWDT also runs on the 32 kHz CLK32K clock and has a maximum programmable period up to 524 (2^24/32 kHz) seconds.

4.17 Real-Time Counter (RTC)

The real-time counter (RTC) module features a 32-bit counter and a tick event generator. The RTC runs on the 32 kHz CLK32K clock. It is used for low-power timing, and it can keep running even when the system is in deep sleep mode.

4.18 IrDA Interface (IrDA)

The BK3437 embeds a hardware IrDA interface to encode and decode signals. In addition, the interface has a capture timer capability that allows software decoding of the input signal.

The IrDA has the following features:

- Single-duplex mode
- Carrier modulation for transmission
- Integrated 512-byte RX FIFO and 512-byte TX FIFO

4.19 Temperature Sensor

The BK3437 integrates an on-chip temperature sensor that can measure on-chip temperature over -40 to +125 °C with an accuracy of ±2 °C. The digital results can be read by the ADC.

Usually, the software initiates the calibration of a specific module based on the temperature value, narrowing the difference in chip performance at different temperatures. The host can also read the on-chip temperature and decide whether to reduce transmit power or suspend operation at high temperatures.

5. Electrical Characteristics

Note: Values currently listed in this section are preliminary measurements and are subject to change.

5.1 Absolute Maximum Ratings

Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute-maximum-rated conditions for prolonged periods may affect the reliability of the device.

Parameter	Description	Min.	Max.	Unit
VCCO	Supply voltage for analog	-0.3	3.6	V
VCCMCU	Supply voltage for MCU	-0.3	3.6	V
VCCRF	Supply voltage for RF	-0.3	3.6	V
VCCXTAL	Supply voltage for crystal	-0.3	3.6	V
VDDDSP	Digital LDO output voltage	-0.3	1.2	V
MICBIAS	Microphone bias output voltage	-0.3	1.8	V
P_{RX}	RX input power	-	0	dBm
T_{STR}	Storage temperature range	-55	150	℃

5.2 ESD Ratings

Parameter	Description	Test Condition	Value	Unit
ESD HBM	Electrostatic discharge voltage (human body model), per ANSI/ESDA/JEDEC JS-001-2017	-	TBD	V
ESD CDM	Electrostatic discharge voltage (charge device model), per ANSI/ESDA/JEDEC JS-002-2018	-	TBD	V

5.3 Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
VCCO	Supply voltage for analog	1.7	3.0	3.6	V
VCCMCU	Supply voltage for MCU	1.7	3.0	3.6	V

Parameter	Description	Min.	Typ.	Max.	Unit
VCCRF	Supply voltage for RF	1.7	3.0	3.6	V
VCCXTAL	Supply voltage for crystal	1.7	3.0	3.6	V
VDDDSP	Digital LDO output voltage	-	-	1.2	V
MICBIAS	Microphone bias output voltage	-	-	1.8	V
T_{OPR}	Operating temperature range	-40	-	125	℃

5.4 Digital I/O Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VIH	High-level input voltage	-	0.7 VCC	-	1.1 VCC	V
VIL	Low-level input voltage	-	-0.3	-	0.3 VCC	V
VOH	High-level output voltage	-	0.9 VCC	-	-	V
VOL	Low-level output voltage	-	-	-	0.1 VCC	V
I_{DRV}	I/O output drive strength	-	4.5	-	18	mA
R_{PU}	Weak pull-up resistor	-	-	50	-	kΩ
R_{PD}	Weak pull-down resistor	-	-	50	-	kΩ

5.5 16 MHz Crystal Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
F0	Nominal Frequency	-	-	16	-	MHz
ΔF/F0	Frequency tolerance	25 ℃	-10	-	+10	ppm
TC	Frequency stability over operating temperature	-40 to 105 ℃ crystal	-20	-	+20	ppm
		-30 to 85 ℃ crystal	-10	-	+10	ppm
CL	Load capacitance	-	7	7	9	pF
TS	Trim sensitivity	-	-	22	-	ppm/pF

5.6 Current Consumption

Measured with T = 25 °C, VCC = 3.3 V unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
Active Mode					
RX current	-	-	10.5	-	mA
TX current	0 dBm	-	15	-	mA
	10 dBm	-	32	-	mA
Sleep Mode					
Normal sleep	1.2 V digital voltage	-	10.4	-	µA
Low-voltage sleep	ROSC and AON on	-	3.6	-	µA
Deep sleep	ROSC off, AON on, bandgap off	-	0.6	-	µA
	ROSC and AON on, bandgap off	-	0.9	-	µA
Shutdown Mode					
Shutdown	ROSC on, AON off	-	0.4	-	µA

5.7 Bluetooth LE RF Receiver Characteristics

Measured with T = 25 °C, VCC = 3.3 V unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
General					
Frequency range	-	2402	-	2480	MHz
Bluetooth LE 1 Mbps					
Sensitivity	30.8% PER	-	-96	-	dBm
Maximum input level	30.8% PER	-	TBD	-	dBm
C/I co-channel	-	-	TBD	-	dB
C/I 1 MHz adjacent channel	-	-	TBD	-	dB
C/I -1 MHz adjacent channel	-	-	TBD	-	dB
C/I 2 MHz adjacent channel	-	-	TBD	-	dB

Parameter	Condition	Min.	Typ.	Max.	Unit
C/I -2 MHz adjacent channel	-	-	TBD	-	dB
C/I 3 MHz adjacent channel	-	-	TBD	-	dB
C/I -3 MHz adjacent channel	-	-	TBD	-	dB
C/I > 3 MHz adjacent channel	-	-	TBD	-	dB
C/I < -3 MHz adjacent channel	-	-	TBD	-	dB
C/I image channel	-	-	TBD	-	dB
C/I 1 MHz adjacent to image channel	-	-	TBD	-	dB
C/I -1 MHz adjacent to image channel	-	-	TBD	-	dB
Out-of-band blocking	30–2000 MHz	-	TBD	-	dBm
	2003–2399 MHz	-	TBD	-	dBm
	2484–2997 MHz	-	TBD	-	dBm
	3000 MHz–12.75 GHz	-	TBD	-	dBm
Intermodulation	-	-	TBD	-	dBm
Bluetooth LE 2 Mbps					
Sensitivity	30.8% PER	-	TBD	-	dBm
Maximum input level	30.8% PER	-	TBD	-	dBm
C/I co-channel	-	-	TBD	-	dB
C/I 2 MHz adjacent channel	-	-	TBD	-	dB
C/I -2 MHz adjacent channel	-	-	TBD	-	dB
C/I 4 MHz adjacent channel	-	-	TBD	-	dB
C/I -4 MHz adjacent channel	-	-	TBD	-	dB
C/I 6 MHz adjacent channel	-	-	TBD	-	dB
C/I -6 MHz adjacent channel	-	-	TBD	-	dB
C/I > 6 MHz adjacent channel	-	-	TBD	-	dB
C/I < -6 MHz adjacent channel	-	-	TBD	-	dB
C/I image channel	-	-	TBD	-	dB

Parameter	Condition	Min.	Typ.	Max.	Unit
C/I 2 MHz adjacent to image channel	-	-	TBD	-	dB
C/I -2 MHz adjacent to image channel	-	-	TBD	-	dB
Out-of-band blocking	30–2000 MHz	-	TBD	-	dBm
	2003–2399 MHz	-	TBD	-	dBm
	2484–2997 MHz	-	TBD	-	dBm
	3000 MHz–12.75 GHz	-	TBD	-	dBm
Intermodulation	-	-	TBD	-	dBm

5.8 Bluetooth LE RF Transmitter Characteristics

Measured with T = 25 °C, VCC = 3.3 V unless otherwise stated.

Parameter		Condition	Min.	Typ.	Max.	Unit
General						
Frequency range		-	2402	-	2480	MHz
TX power		-	-20	-	10	dBm
Bluetooth LE 1 Mbps						
In-band emissions	±2 MHz offset	-	-	TBD	-	dBm
	±3 MHz offset	-	-	TBD	-	dBm
	> ±3 MHz offset	-	-	TBD	-	dBm
Modulation characteristics	Δf1avg	-	-	TBD	-	kHz
	Δf2max	-	-	TBD	-	kHz
	Δf2avg/Δf1avg	-	-	TBD	-	-
Carrier frequency offset and drift	Max $\|f_n\|$ n = 0, 1, 2, 3…k	-	-	TBD	-	kHz
	Max $\|f_0 - f_n\|$ n = 2, 3, 4…k	-	-	TBD	-	kHz
	$\|f_1 - f_0\|$	-	-	TBD	-	kHz
	Max $\|f_n - f_{n-5}\|$ n = 6, 7, 8…k	-	-	TBD	-	kHz/50 µs

Parameter		Condition	Min.	Typ.	Max.	Unit
Bluetooth LE 2 Mbps						
In-band emissions	±4 MHz offset	-	-	TBD	-	dBm
	±5 MHz offset	-	-	TBD	-	dBm
	> ±5 MHz offset	-	-	TBD	-	dBm
Modulation characteristics	Δf1avg	-	-	TBD	-	kHz
	Δf2max	-	-	TBD	-	kHz
	Δf2avg/Δf1avg	-	-	TBD	-	-
Carrier frequency offset and drift	Max $\|f_n\|$ n = 0, 1, 2, 3…k	-	-	TBD	-	kHz
	Max $\|f_0 - f_n\|$ n = 2, 3, 4…k	-	-	TBD	-	kHz
	$\|f_1 - f_0\|$	-	-	TBD	-	kHz
	Max $\|f_n - f_{n-5}\|$ n = 6, 7, 8…k	-	-	TBD	-	kHz/50 μs

5.9 AUX ADC Characteristics

Parameter	Condition	Min.	Typ.	Max.	Unit
Current consumption	-	-	0.3	-	mA
ADC Core					
ADC reference voltage (VREF)	-	-	1.1	-	V
ADC sampling clock	-	-	16	-	MHz
Absolute error	Includes gain error, offset and distortion. Without factory calibration.	-	TBD	-	%
	Includes gain error, offset and distortion. After factory calibration.	-	TBD	-	%
ENOB	For audio application	12	-	-	Bit
	For static measurement	11	-	-	Bit
ADC input full scale	For audio application	-	1.6	-	V
	For static measurement	-	2	4	V
Conversion rate	For audio application	-	TBD	-	kHz
Signal bandwidth	For audio application	-	TBD	-	Hz

Parameter	Condition	Min.	Typ.	Max.	Unit
	For static measurement	-	DC	-	Hz
Input impedance	For audio application	10	-	-	kΩ
	For static measurement	160	-	-	kΩ
Startup time	For audio application	20	-	-	ms
	For static measurement	20	-	-	ms
ADC SNR	A-weighted 0 dB PGA gain, Temperature = 25 ℃	-	70	-	dB
ADC THD + N	-3 dBFS input 0 dB PGA gain, Temperature = 25 ℃	-	-60	-	dB
MIC PGA					
MIC PGA gain range	-	0	-	10	dB
MIC PGA gain step	-	-	1	-	dB

6. Package Information

Figure 6-1 QFN32 4 x 4 mm Package Outline

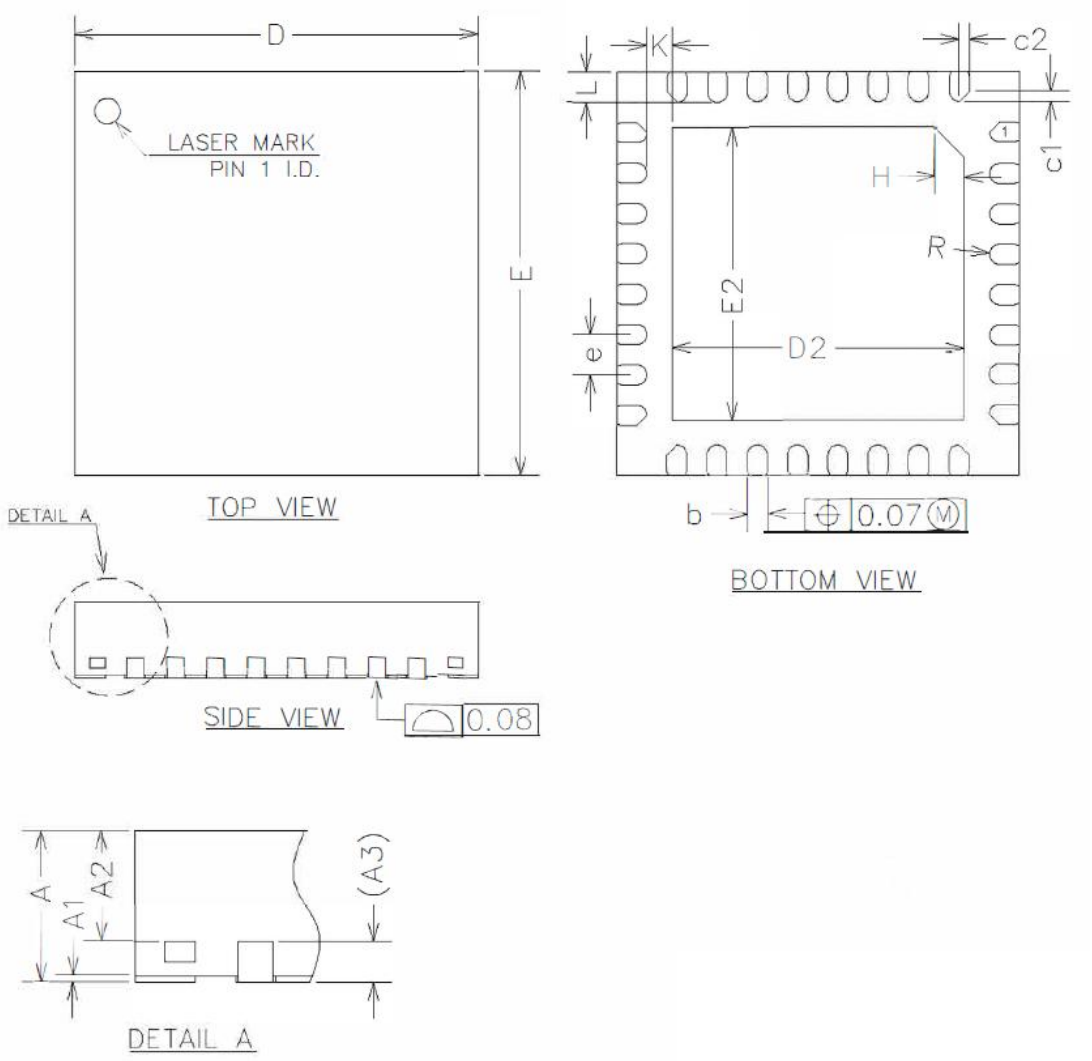


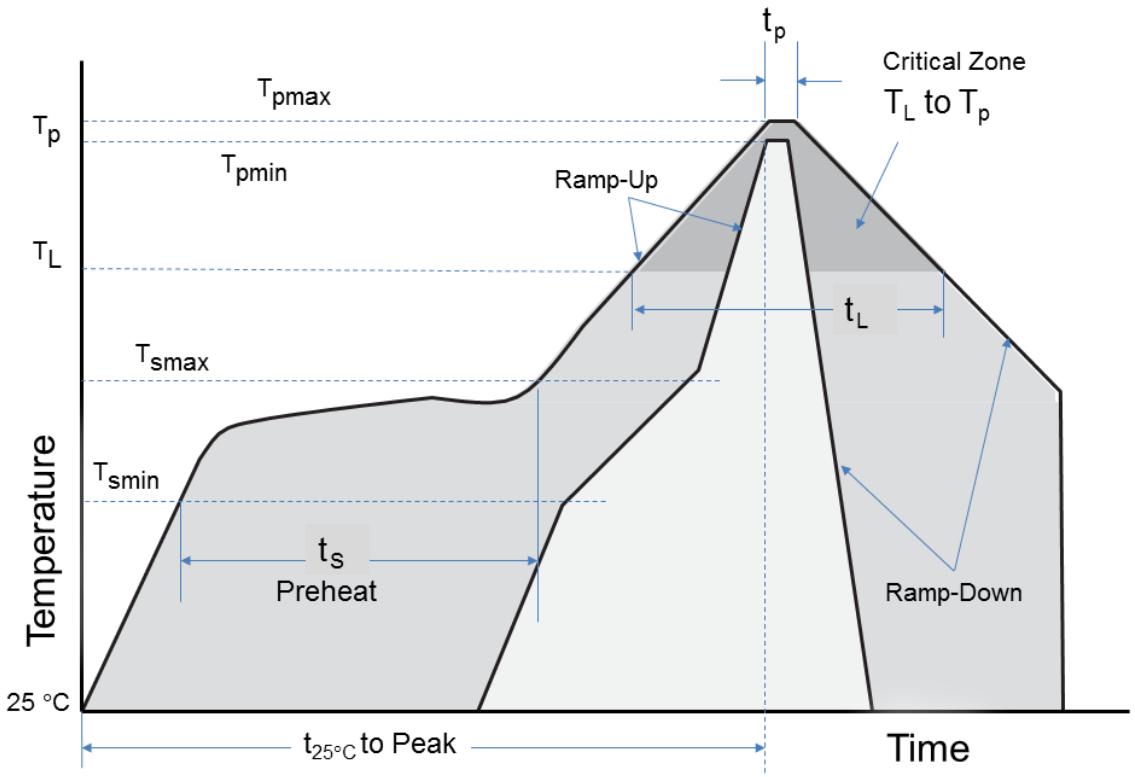
Table 6-1 QFN32 Package Dimensions

Symbol	Dimensions in Millimeters		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.50	0.55	0.60
A3	0.20 REF		

Symbol	Dimensions in Millimeters		
	Min.	Nom.	Max.
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.80	2.90	3.00
E2	2.80	2.90	3.00
e	0.30	0.40	0.50
H	0.30 REF		
K	0.25 REF		
L	0.25	0.30	0.35
R	0.09	-	-
c1	-	0.10	-
c2	-	0.10	-

7. Reflow Soldering Profile

Figure 7-1 Reflow Soldering Profile



Profile Feature		Specification
Average ramp-up rate (T_{smax} to T_p)		3 ℃/s max.
Preheat	Temperature min. (T_{smin})	150 ℃
	Temperature max. (T_{smax})	200 ℃
	Time (t_s)	60 s to 180 s
Time maintained above	Temperature (T_L)	217 ℃
	Time (t_L)	60 s to 150 s
Peak/classification temperature (T_p)		260 ℃
Time within 5 ℃ of actual peak temperature (t_p)		20 s to 40 s
Ramp-down rate		6 ℃/s max.

Profile Feature	Specification
Time 25 ℃ to peak temperature	8 minutes max.

RoHS Compliant

The product does not contain lead, mercury, cadmium, hexavalent chromium, PBB&PBDE content in accordance with directive 2002/95/EC (RoHS).

ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electricity. Proper ESD techniques should be used when handling these devices.

Moisture Sensitivity Level

The product is qualified to moisture sensitivity level MSL3 in accordance with IPC/JEDEC J-STD-020.

8. Ordering Information

Figure 8-1 Part Number Scheme

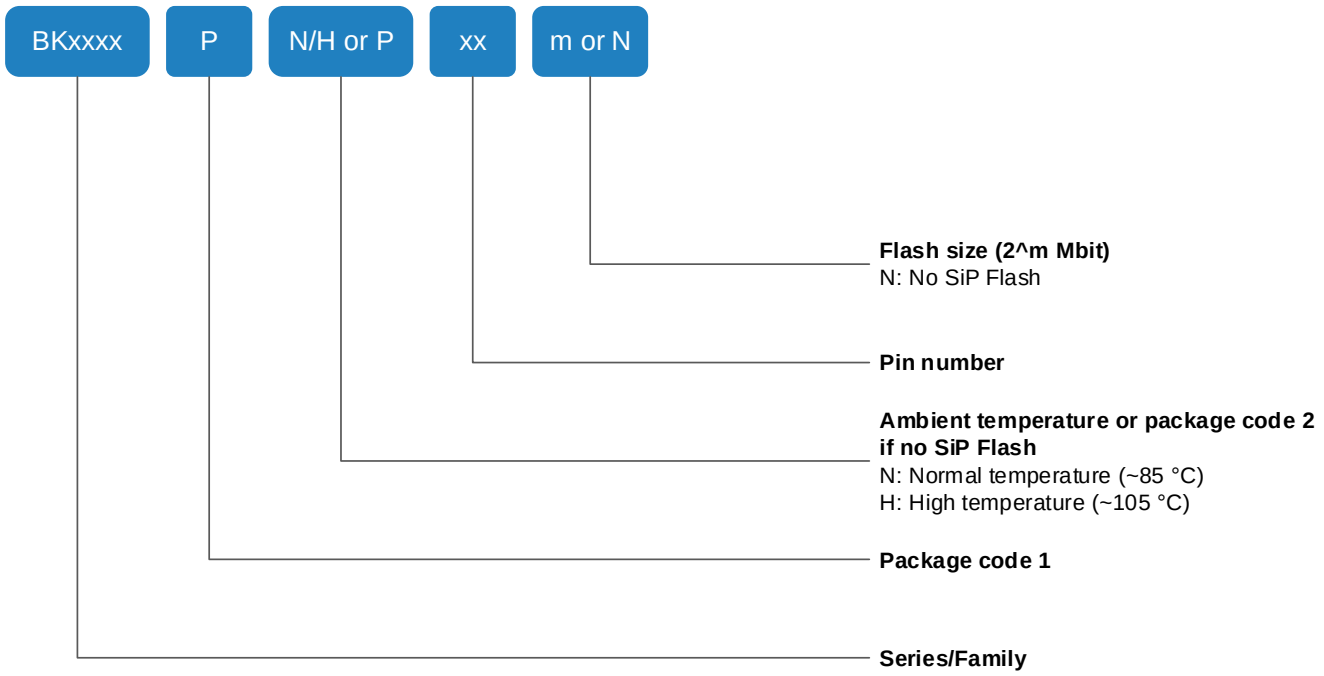


Table 8-1 Ordering Information

Ordering Code	Package	SiP[a] Flash	Packing	Minimum Ordering Qty (MOQ)
BK3437QN321	4 mm x 4 mm QFN32	2 Mbit	Tape and Reel	3000

a. A system in a package (SiP) refers to Flash enclosed in the package.

Revision History

Version	Date	Description
1.0	2022/12/9	Initial release
1.1	2023/8/28	• Updated wording throughout document • Updated Flash size in Section 1 Features • Renamed some interfaces and peripherals • Renamed standby modes to sleep modes • Updated information for QFN32 package • Updated Section 4.4 Clock Management • Renamed Section Modes of Operation as Section Power Modes and reorganized the section as a subsection of Section 4.6 Power Management • Updated Section 4.12 PWM Group (PWMG) • Updated storage temperature range in Section 5.1 Absolute Maximum Ratings • Added Section 5.2 ESD Ratings • Added Section 5.4 Digital I/O Characteristics • Updated and added values in Section 5.5 16 MHz Crystal Characteristics • Updated ordering information in Section 8 Ordering Information

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Beken Corporation

Building 41, 1387 Zhangdong Rd

Shanghai 201203

China

http://www.bekencorp.com