# EVAL6482H

## High power microstepping motor driver with the L6482H

**Data brief**


## Features

- Voltage range from 10.5 V to 85 V
- Low $R_{ds(ON)}$ MOSFETs in DPAK package
- SPI with daisy chain feature
- FLAG and BUSY LED indicators
- Flexible supply voltage management
- Suitable for use in combination with the STEVAL-PCC009V2

## Applications

- High power bipolar stepper motor driving

## Description

The EVAL6482H demonstration board is a high power microstepping motor driver. In combination with the STEVAL-PCC009V2 communication board and the evaluation software, the board allows the user to investigate all the features of the L6482 device. In particular, the board can be used to check the advanced current control and to regulate the L6482 parameters in order to fit the application requirements.

The EVAL6482H supports the daisy chain configuration making it suitable for the evaluation of the L6482 in multi motor applications.

# Board description

**Table 1. EVAL6482H electrical specifications**

| Parameter | Value |
|---|---|
| Supply voltage (VS) | 10.5 to 85 V |
| Maximum output current (each phase) | 6 $A_{r.m.s.}$ at 25 °C(1) |
| External MOSFET $R_{ds(ON)}$ | 33 mΩ typical at 25 °C(2) |
| Gate driver supply voltage (VCC) | 7.5 V to 15 V |
| Logic supply voltage | 3.3 V |
| Logic interface supply voltage | 3.3 V or 5 V |
| Low level logic input | 0 V |
| High level logic input | VDD(3) |
| Operating temperature | -25 °C to +125 °C |

1. Limited by the mounted sensing resistors.
2. Refer to STD25NF10 datasheet for details.
3. All logic inputs are 5 V tolerant.

**Figure 1. Jumper and connector location**

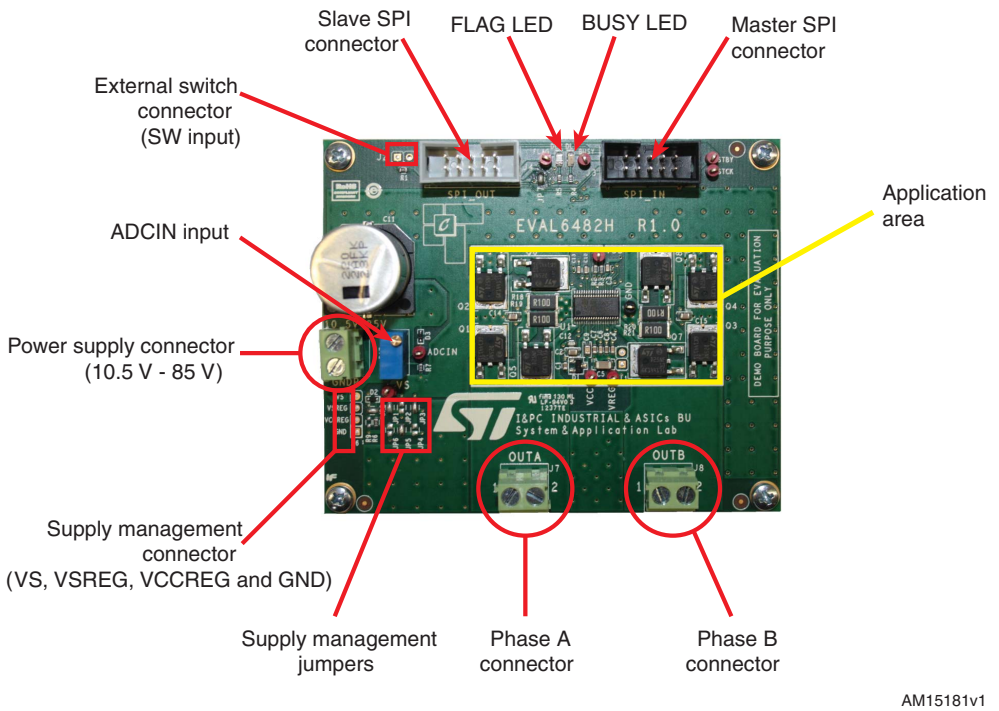


**Table 2. Jumper and connector description**

| Name | Type | Function |
|---|---|---|
| J5 | Power supply | Main supply voltage |
| J7 | Power output | Power bridge A outputs |
| J8 | Power output | Power bridge B outputs |
| J6 | Power supply | Integrated voltage regulator inputs |
| J3 | SPI | Master SPI connector |
| J4 | SPI | Slave SPI connector |
| JP1 | Jumper | VS to VSREG jumper |
| JP2 | Jumper | VSREG to VCC jumper |
| JP3 | Jumper | VCC to VCCREG jumper |
| JP4 | Jumper | VCCREG to VREG jumper |
| JP5 | Jumper | VREG to VDD jumper |
| JP6 | Jumper | VDD to 3.3 V from SPI connector jumper |
| JP7 | Jumper | Daisy chain termination jumper |
| JP8 | Jumper | STBY to VS pull-up jumper |

**Table 3. Master SPI connector pinout (J3)**

| Pin number | Type | Description |
|---|---|---|
| 1 | Open drain output | L6482 BUSY output |
| 2 | Open drain output | L6482 FLAG output |
| 3 | Ground | Ground |
| 4 | Supply | EXT_VDD (can be used as external logic power supply) |
| 5 | Digital output | SPI “Master In Slave Out” signal (connected to the L6482 SDO output through daisy chain termination jumper JP7) |
| 6 | Digital input | SPI serial clock signal (connected to L6482 CK input) |
| 7 | Digital input | SPI “Master Out Slave In” signal (connected to L6482 SDI input) |
| 8 | Digital input | SPI slave select signal (connected to L6482 CS input) |
| 9 | Digital input | L6482 step-clock input |
| 10 | Digital input | L6482 standby/reset input |

**Table 4. Slave SPI connector pinout (J4)**

| Pin number | Type | Description |
|---|---|---|
| 1 | Open drain output | L6482 BUSY output |
| 2 | Open drain output | L6482 FLAG output |
| 3 | Ground | Ground |
| 4 | Supply | EXT_VDD (can be used as external logic power supply) |
| 5 | Digital output | SPI “Master In Slave Out” signal (connected to pin 5 of J3) |
| 6 | Digital input | SPI serial clock signal (connected to L6482 CK input) |
| 7 | Digital input | SPI “Master Out Slave In” signal (connected to L6482 SDO output) |
| 8 | Digital input | SPI slave select signal (connected to L6482 CS input) |
| 9 | Digital input | L6482 step-clock input |
| 10 | Digital input | L6482 standby/reset input |

**Figure 2. EVAL6482H schematic - part 1/2**

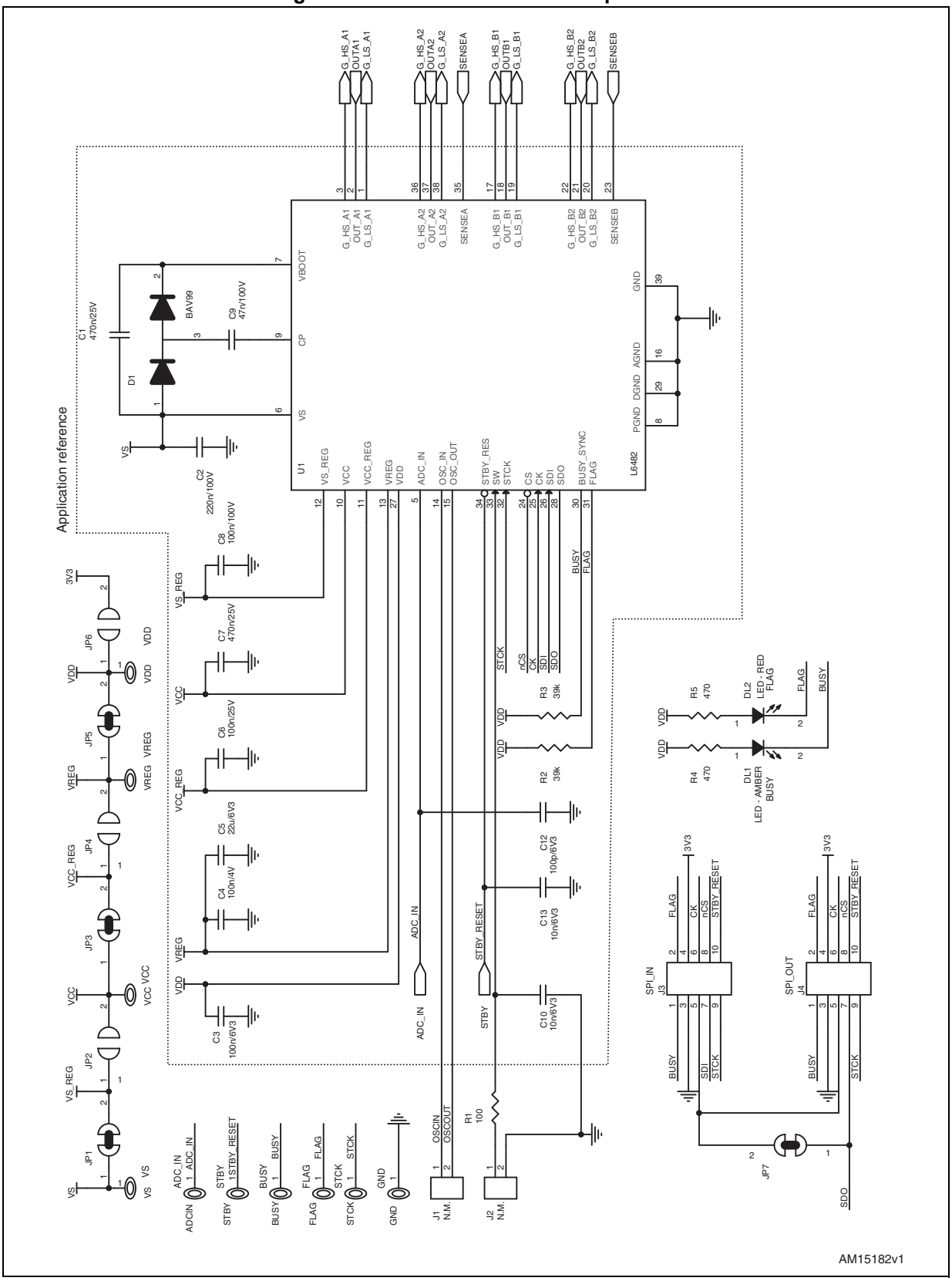


**Figure 3. EVAL6482H schematic - part 2/2**

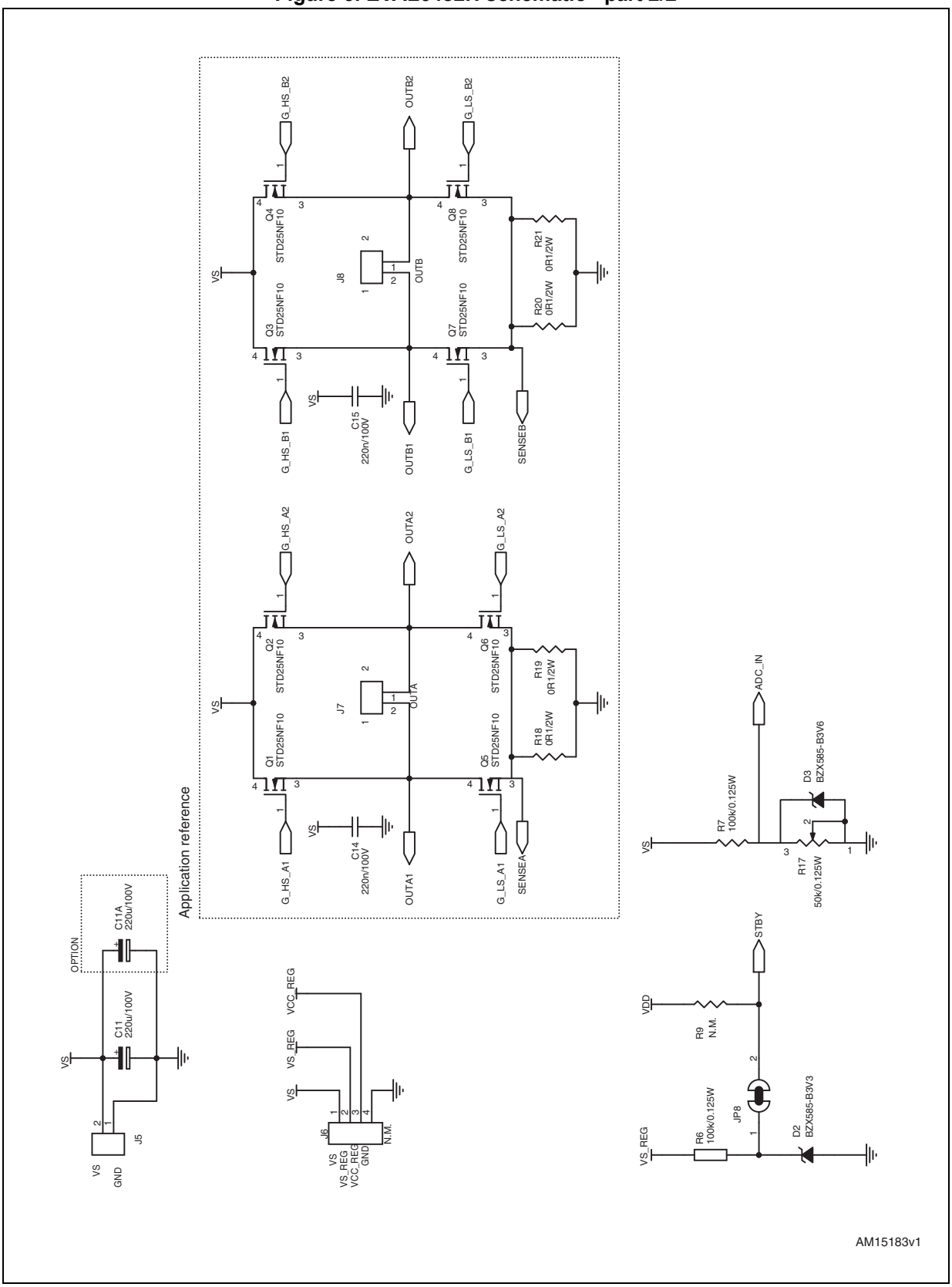


**Table 5. EVAL6482H - bill of material**

| Item | Quantity | Reference | Value | Package |
|---|---|---|---|---|
| 1 | 9 | VS, VREG, VDD, VCC, STCK, STBY, FLAG, BUSY, ADCIN | TPTH-RING (red) | TPTH-RING-1MM |
| 2 | 1 | GND | TP-RING (black) | TPTH-RING-1MM |
| 3 | 2 | C1,C7 | 470 nF/25 V | CAPC-0603 |
| 4 | 3 | C2, C14, C15 | 220 nF/100 V | CAPC-0805 |
| 5 | 1 | C3 | 100 nF/6.3 V | CAPC-0603 |
| 6 | 1 | C4 | 100 nF/4 V | CAPC-0603 |
| 7 | 1 | C5 | 22 µF/6.3 V | CAPC-1206 |
| 8 | 1 | C6 | 100 nF/25 V | CAPC-0603 |
| 9 | 1 | C8 | 100 nF/100 V | CAPC-0603 |
| 10 | 1 | C9 | 47 nF/100 V | CAPC-0805 |
| 11 | 2 | C10, C13 | 10 nF/6.3 V | CAPC-0603 |
| 12 | 1 | C11 | 220 µF/100 V | CAPES-R18H17 |
| 13 | 1 | C11A | 220 µF/100 V | CAPE-R16H21-P75 |
| 14 | 1 | C12 | 100 pF/6.3 V | CAPC-0603 |
| 15 | 1 | DL1 | LED amber | LEDC-0805 |
| 16 | 1 | DL2 | LED red | LEDC-0805 |
| 17 | 1 | D1 | BAV99 | SOT-23 |
| 18 | 1 | D2 | BZX585-B3V3 | SOD523 |
| 19 | 1 | D3 | BZX585-B3V6 | SOD523 |
| 20 | 5 | JP1, JP3, JP5, JP7, JP8 | Jumper CLOSED | JP2SO |
| 21 | 3 | JP2, JP4, JP6 | Jumper OPEN | JP2SO |
| 22 | 2 | J1, J2 | N. M. | STRIP254P-M-2 |
| 23 | 1 | J3 | Pol. IDC male header vertical 10 poles (black) | CON-FLAT-5X2-180M |
| 24 | 1 | J4 | Pol. IDC male header vertical 10 poles (gray) | CON-FLAT-5X2-180M |
| 25 | 3 | J5, J7, J8 | Screw connector 2 poles | MORSV-508-2P |
| 26 | 1 | J6 | N. M. | STRIP254P-M-4 |
| 27 | 8 | Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8 | STD25NF10 | DPAK |
| 28 | 1 | R1 | 100 Ω | RESC-0603 |
| 29 | 2 | R2, R3 | 39 kΩ | RESC-0603 |
| 30 | 2 | R4, R5 | 470 Ω | RESC-0603 |
| 31 | 2 | R6, R7 | 100 kΩ / 0.125 W | RESC-0603 |

Table 5. EVAL6482H - bill of material (continued)

| Item | Quantity | Reference | Value | Package |
|---|---|---|---|---|
| 32 | 1 | R9 | N. M. | RESC-0603 |
| 33 | 1 | R17 | 50 kΩ / 0.125 W | TRIMM-100X50X110-64W |
| 34 | 4 | R18, R19, R20, R21 | 0.1 Ω /2 W | RESC-2010 |
| 35 | 1 | U1 | L6482 | HTSSOP050P-660X110-38-EP |

Figure 4. EVAL6482H - layout (top layer)

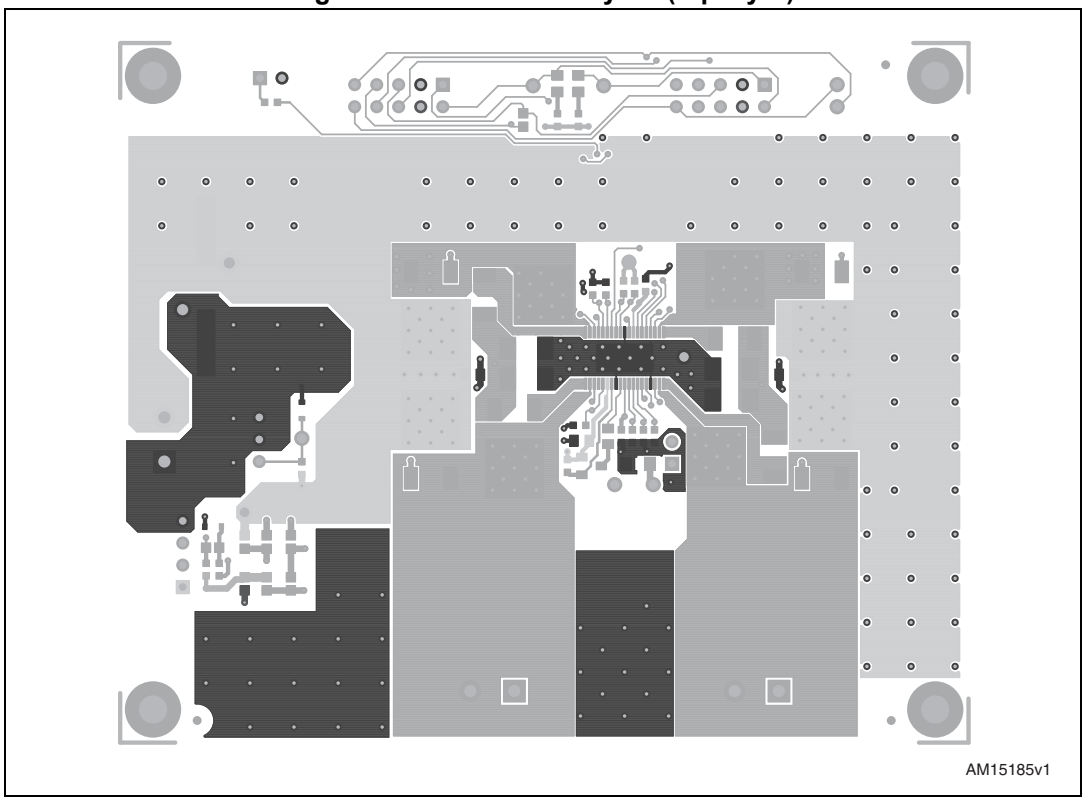



Figure 5. EVAL6482H - layout (inner layer 2)

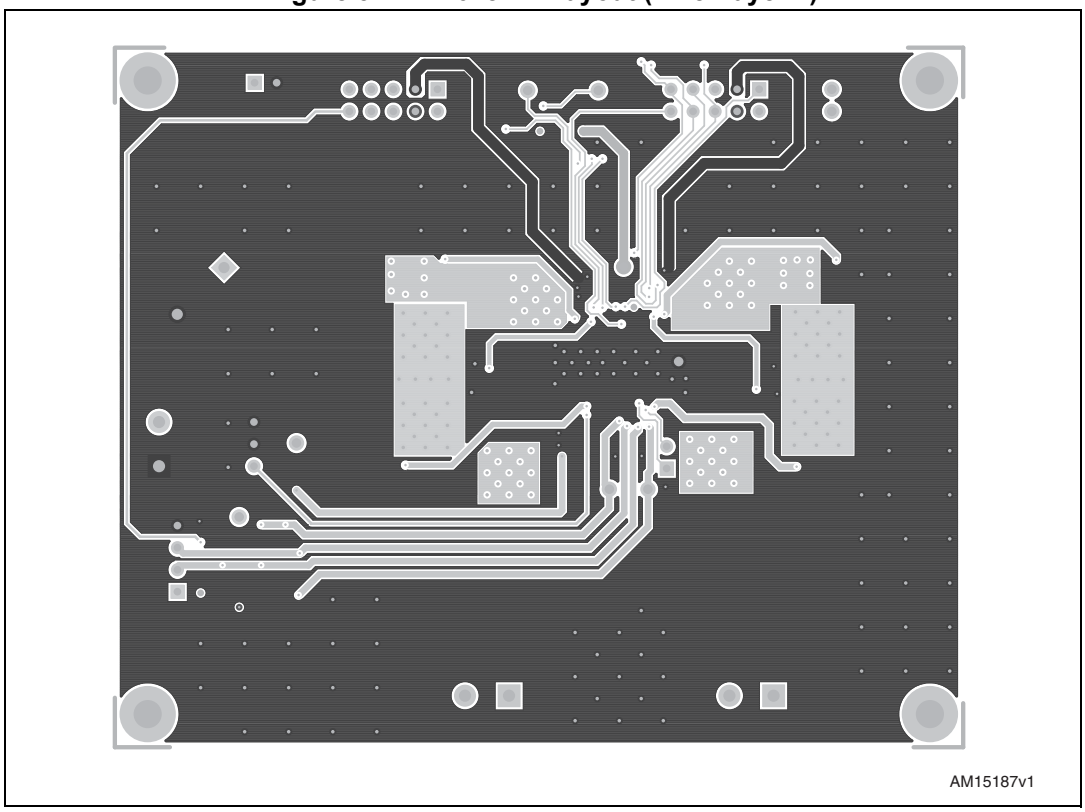


Figure 6. EVAL6482H - layout (inner layer 3)

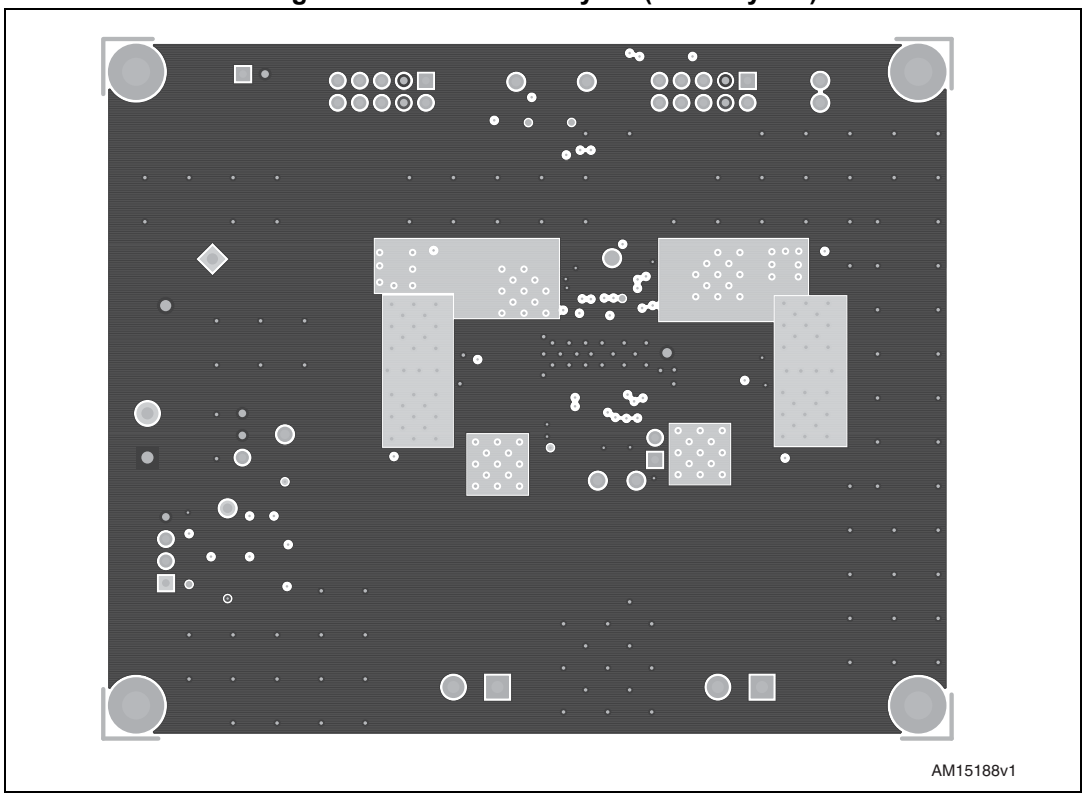
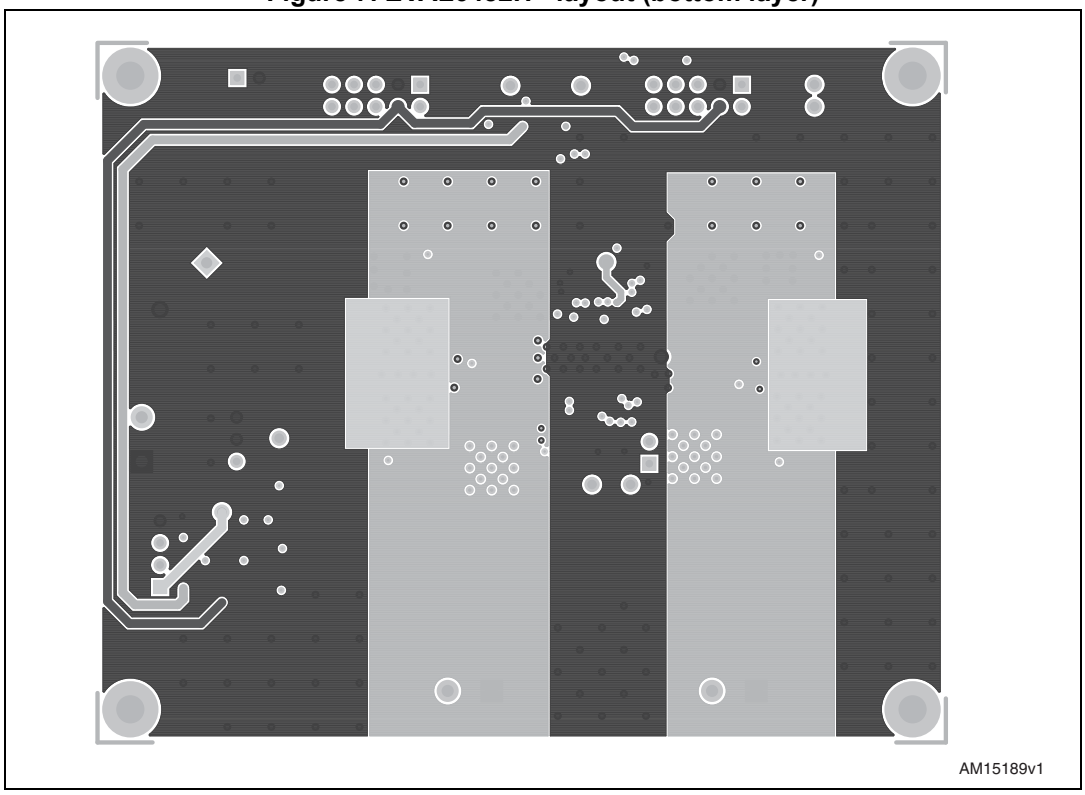



Figure 7. EVAL6482H - layout (bottom layer)



# Revision history

Table 6. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 30-Oct-2012 | 1 | Initial release. |
| 03-Apr-2015 | 2 | Removed Figure 4. EVAL6482H - layout (silkscreen) from page 8.<br>Minor modifications throughout document. |