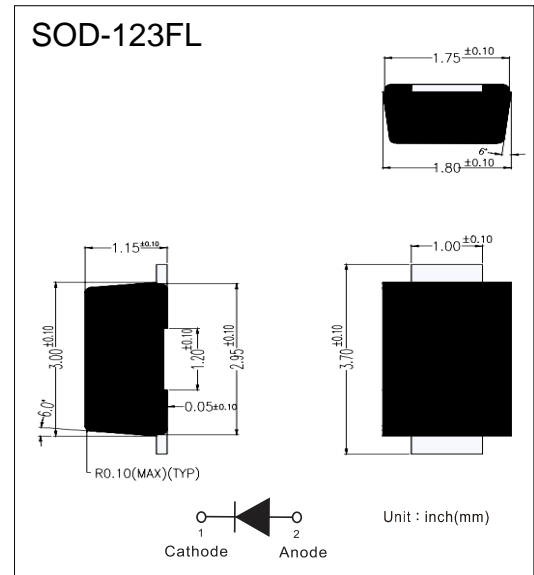


## ■ Features

- Glass passivated junction chip
- Ideal for automated placement
- Super fast recovery time for high efficiency
- Built-in strain relief
- Comply with RoHS standard, halogen-free

## ■ Mechanical Data

- package:SOD-123FL
- Polarity: Indicated by cathode band
- Epoxy: UL 94V-0 rate flame retardant
- Mounting Position : Any



## ■ Maximum Ratings And Electrical Characteristics( $T_A=25^{\circ}\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	ES1A	ES1B	ES1C	ES1D	ES1F	ES1G	ES1H	ES1J	UNIT
Maximum repetitive peak reverse voltage	$V_{RRM}$	50	100	150	200	300	400	500	600	V
Maximum RMS voltage	$V_{RMS}$	35	70	105	140	210	280	350	420	V
Maximum DC blocking voltage	$V_{DC}$	50	100	150	200	300	400	500	600	V
Maximum average forward rectified current	$I_F(AV)$	1								A
Peak forward surge current, 8.3 ms single half sine-wave superimposed on rated load	$I_{FSM}$	30								A
Maximum instantaneous forward voltage (Note 1) @ 1 A	$V_F$	0.95			1.3		1.7			V
Maximum reverse current @ rated $V_R$ $T_J=25^{\circ}\text{C}$ $T_J=125^{\circ}\text{C}$	$I_R$	5 100								$\mu\text{A}$
Maximum reverse recovery time (Note 2)	$t_{rr}$	35								ns
Typical junction capacitance (Note 3)	$C_J$	16				18				pF
Typical thermal resistance	$R_{\theta JL}$ $R_{\theta JA}$	35 85								$^{\circ}\text{C/W}$
Operating junction temperature range	$T_J$	- 55 to +150								$^{\circ}\text{C}$
Storage temperature range	$T_{STG}$	- 55 to +150								$^{\circ}\text{C}$

Note 1: Pulse test with  $PW=300\mu\text{s}$ , 1% duty cycle

Note 2: Reverse Recovery Test Conditions:  $I_F=0.5\text{A}$ ,  $I_R=1.0\text{A}$ ,  $I_{RR}=0.25\text{A}$

Note 3: Measured at 1 MHz and Applied  $V_R=4.0$  Volts



■ Ratings And Characteristics Curves( $T_A=25^{\circ}\text{C}$  unless otherwise noted)

FIG.1 MAXIMUM FORWARD CURRENT DERATING CURVE

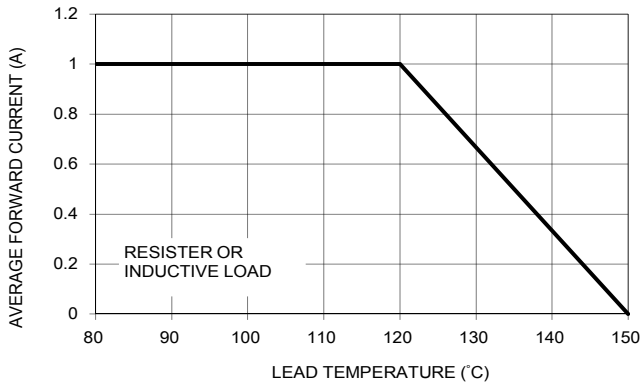


FIG. 2 TYPICAL INSTANTANEOUS FORWARD CHARACTERISTICS

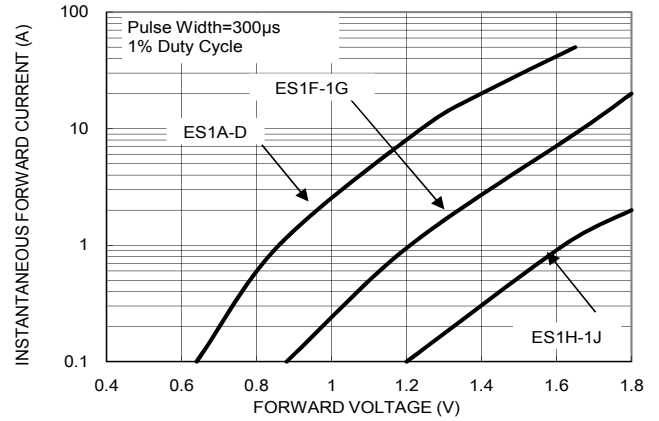


FIG. 3 MAXIMUM NON-REPETITIVE FORWARD PEAK SURGE CURRENT

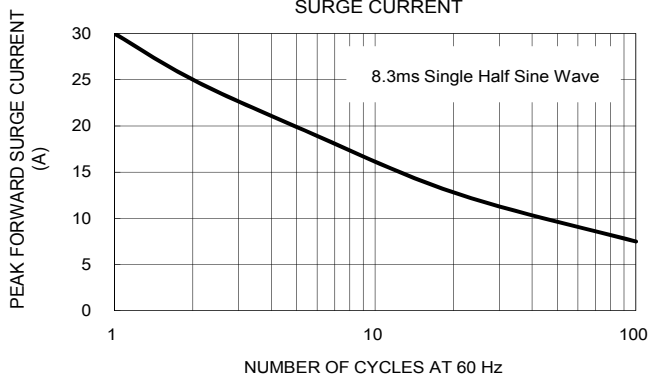


FIG. 4 TYPICAL REVERSE CHARACTERISTICS

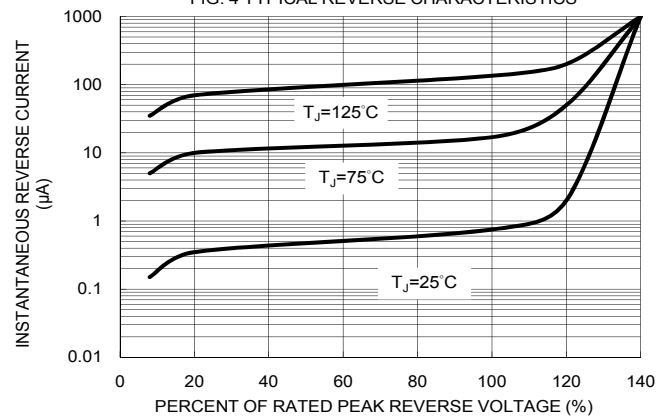


FIG. 5 TYPICAL JUNCTION CAPACITANCE

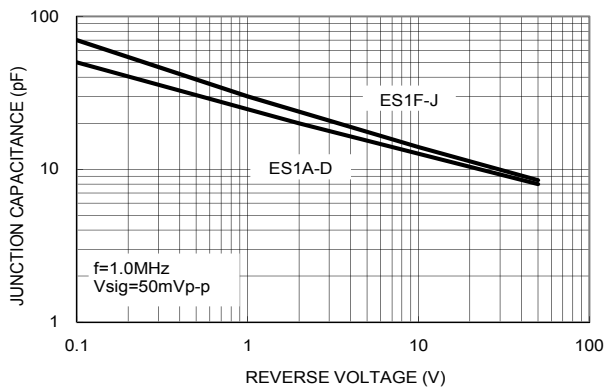


FIG.6- REVERSE RECOVERY TIME CHARACTERISTIC AND TEST CIRCUIT DIAGRAM

