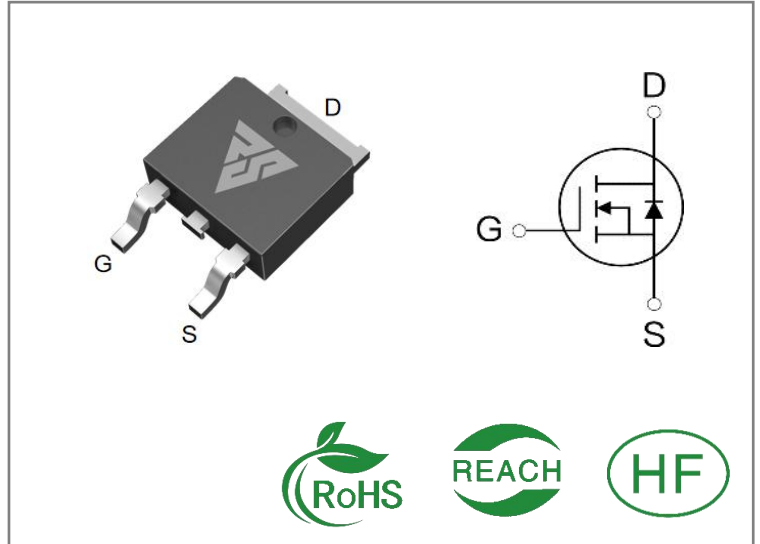


ID	R <sub>DS(ON)</sub> (Typ)	VDSS
60A	4.8mΩ	20V


**Applications:**

- Load Switch
- PWM Applications
- Power Management

**Features:**

- Fast switching speed
- 100% avalanche tested
- Improved dv/dt capability

**Ordering Information**

Part Number	Package	Marking	Packing	Qty.
RS20N60D	T0-252	RS20N60D	Tape&reel	2500 PCS

**Absolute Maximum Ratings** T<sub>c</sub>= 25°C unless otherwise specified

Symbol	Parameter	RS20N60D	Units
VDSS	Drain-to-Source Voltage	20	V
ID	Continuous Drain Current TC=25°C	60	A
ID	Continuous Drain Current TC=100°C	39	
IDM	Pulsed Drain Current	240	
PD	Power Dissipation	38	W
VGS	Gate- to- Source Voltage	±12	V
EAS	Single Pulse Avalanche Energy L = 0.5mH, VDD = 15V, R <sub>G</sub> = 25Ω, T <sub>j</sub> = 25°C	65	mJ
TL TPKG	Maximum Temperature for Soldering	300	°C
	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds	260	
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

\* Drain Current Limited by Maximum Junction Temperature

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" Table may cause permanent damage to the device.  
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**Thermal Resistance**

Symbol	Parameter	RS20N60D	Units	Test Conditions
R $\theta$ JC	Junction-to-Case	3.3	°C / W	Drain lead soldered to water cooled heatsink, PD adjusted for a peak junction temperature of + 1 5 0 °C
R $\theta$ JA	Junction-to-Ambient	32		1 cubic foot chamber, free air.

**OFF Characteristics** TJ= 25°C unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BVDSS	Drain- to- source Breakdown Voltage	20	--	--	V	VGS=0V, ID=250 $\mu$ A
IDSS	Drain- to- Source Leakage Current	--	--	1	$\mu$ A	VDS=20V, VGS=0V
IGSS	Gate- to- Source Forward Leakage	--	--	100	nA	VGS=12V, VDS=0V
	Gate- to- Source Reverse Leakage	--	--	-100		VGS=-12V, VDS=0V

**ON Characteristics** TJ=25°C unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
RDS(on)	Static Drain- to- Source On-Resistance	--	4.8	6.2	m $\Omega$	VGS=4.5V, ID=25A
		--	6.5	8.5	m $\Omega$	VGS=2.5V, ID=15A
VGS(TH)	Gate Threshold Voltage	0.5	0.9	1.1	V	VGS=VDS, ID=250 $\mu$ A

**Resistive Switching Characteristics** Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
td(ON)	Turn- on Delay Time	--	12	--	nS	VDS=10V ID=20A RG=3 $\Omega$ VGS=4.5V
trise	Rise Time	--	32	--		
td(OFF)	Turn- OFF Delay Time	--	48	--		
tfall	Fall Time	--	93	--		

**Dynamic Characteristics** Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ciss	Input Capacitance	--	2007	--	pF	VGS= 0V VDS=10V f=1.0MHz
Coss	Output Capacitance	--	278	--		
Crss	Reverse Transfer Capacitance	--	252	--		
Qg	Total Gate Charge	--	23	--	nC	VDS= 10V ID=20A VGS=4.5V
Qgs	Gate- to- Source Charge	--	4	--		
Qgd	Gate-to-Drain(" Miller") Charge	--	7	--		

**Source- Drain Diode Characteristics**

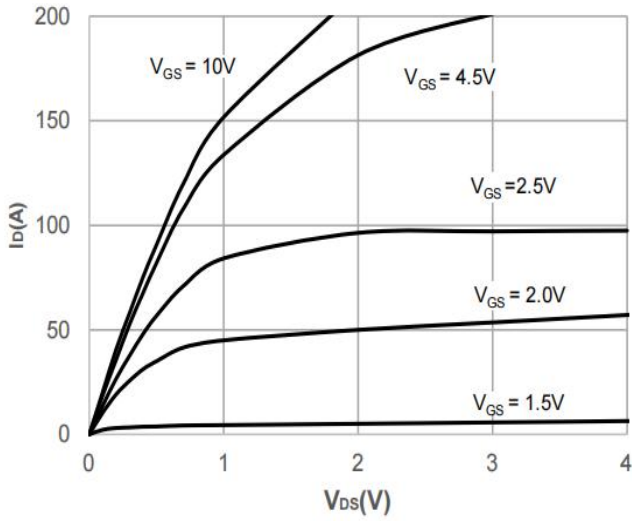
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
IS	Continuous Source Current	--	--	60	A	Integral pn- diode in MOSFET
ISM	Maximum Pulsed Current	--	--	240	A	
VSD	Diode Forward Voltage	--	--	1.2	V	IS=30A,VGS=0V
trr	Reverse Recovery Time	--	12	--	nS	VGS=0V IS=20A di/dt=100A/μs
Qrr	Reverse Recovery Charge	--	2.5	--	nC	

**Notes:**

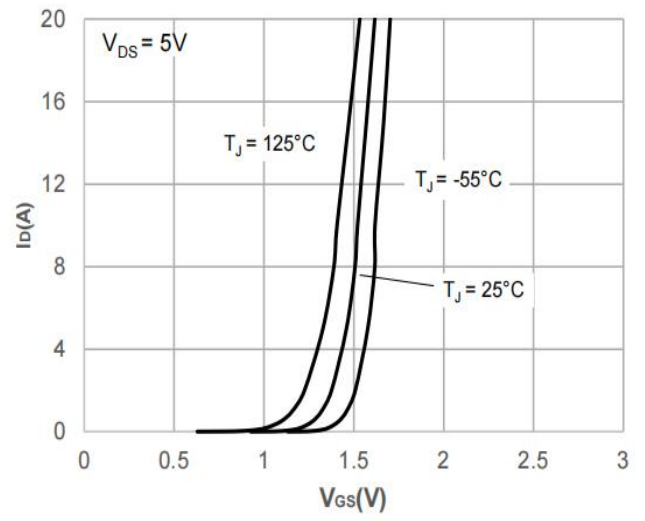
- 
- \* 1. Repetitive rating, pulse width limited by maximum junction temperature.
  - \* 2. Pulse Test: Pulse width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 0.5\%$

**Typical Feature Curve**

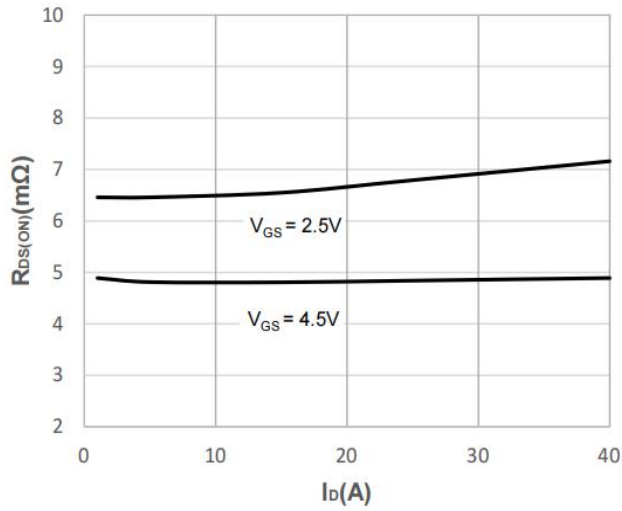
**Figure 1: Output Characteristics**



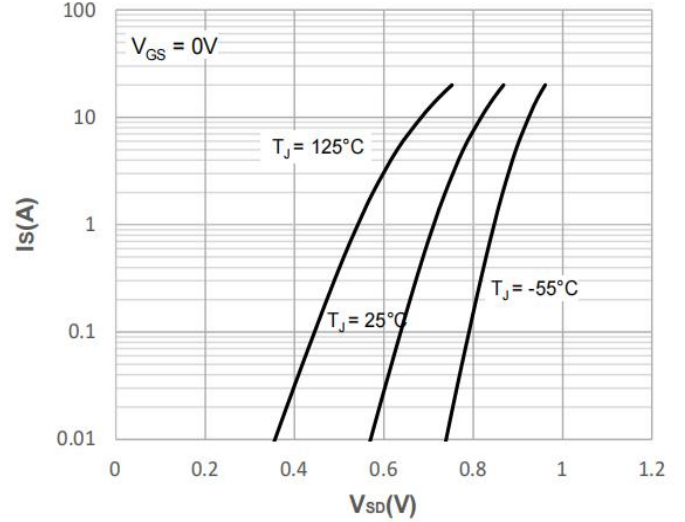
**Figure 2: Typical Transfer Characteristics**



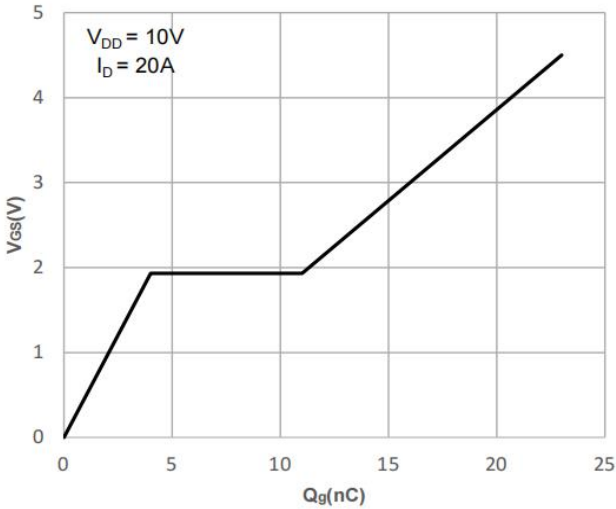
**Figure 3: On-resistance vs. Drain Current**



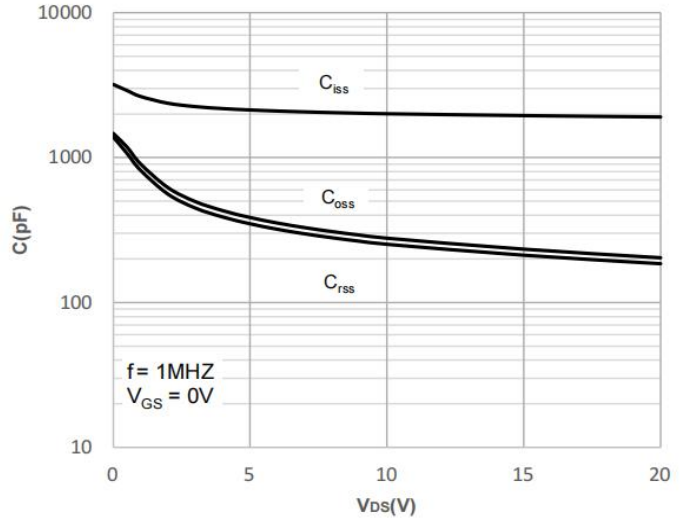
**Figure 4: Body Diode Characteristics**



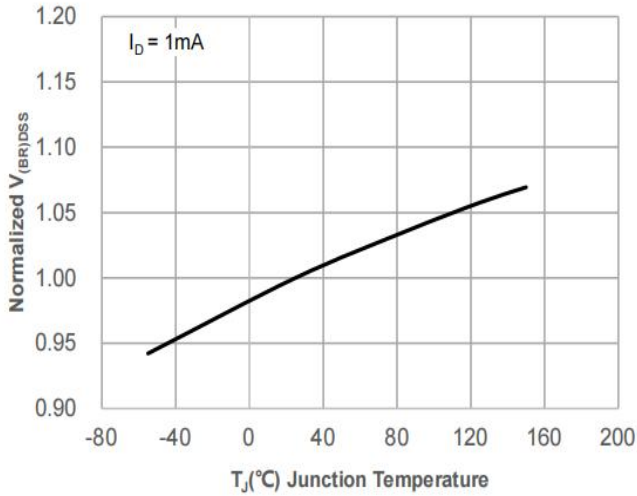
**Figure 5: Gate Charge Characteristics**



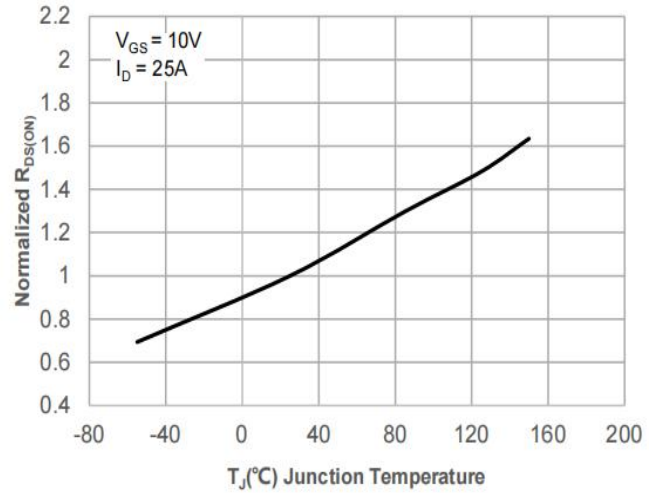
**Figure 6: Capacitance Characteristics**



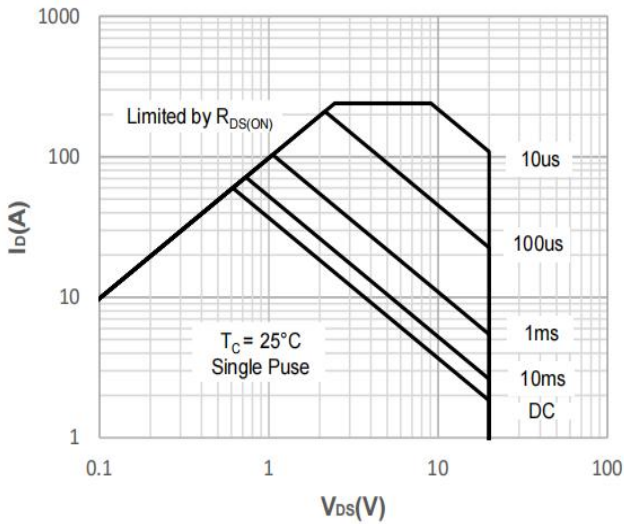
**Figure 7: Normalized Breakdown voltage vs. Junction Temperature**



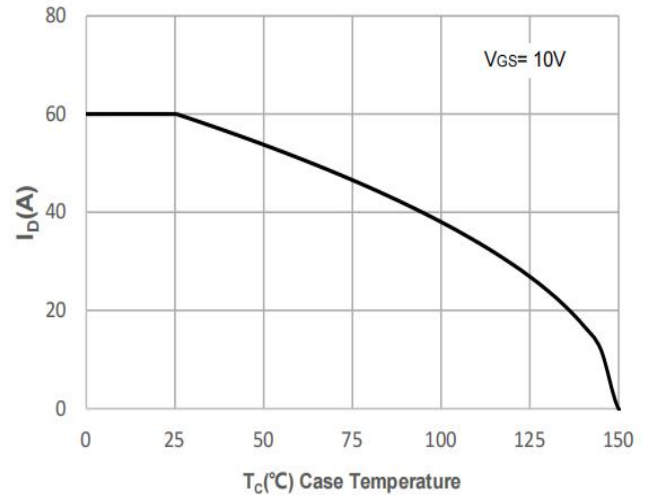
**Figure 8: Normalized on Resistance vs. Junction Temperature**



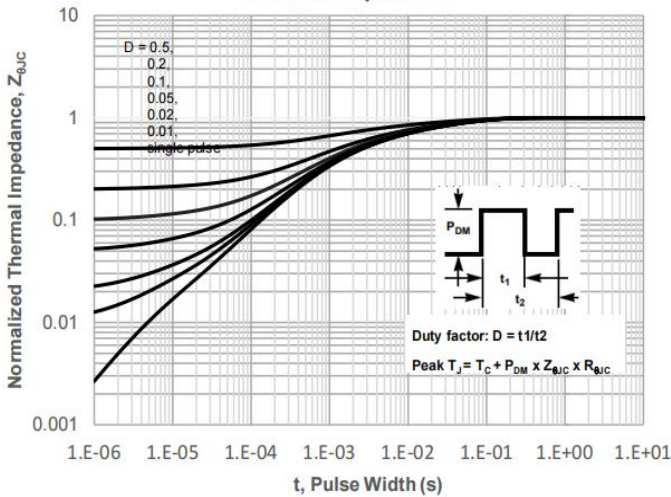
**Figure 9: Maximum Safe Operating Area**



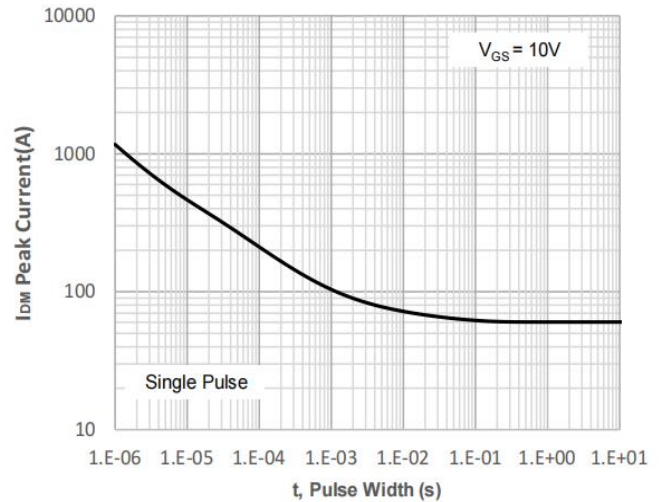
**Figure 10: Maximum Continuous Drain Current vs. Case Temperature**



**Figure 11: Normalized Maximum Transient Thermal Impedance**



**Figure 12: Peak Current Capacity**



Test Circuits and Waveforms

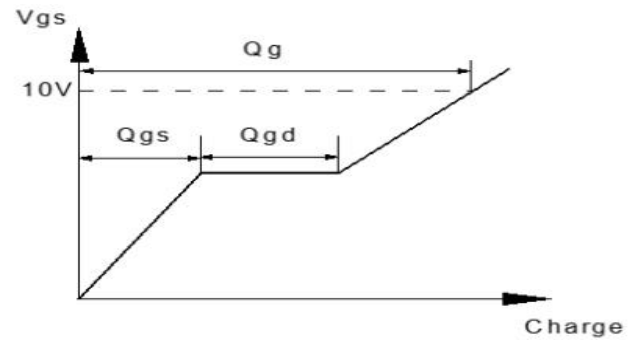
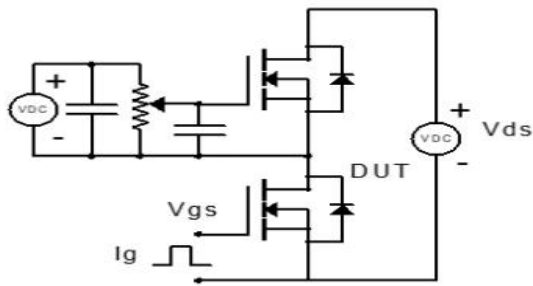


Figure 1: Gate Charge Test Circuit & Waveform

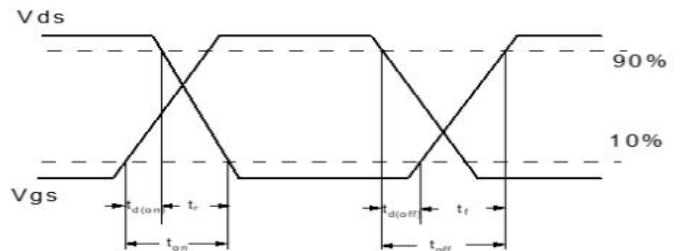
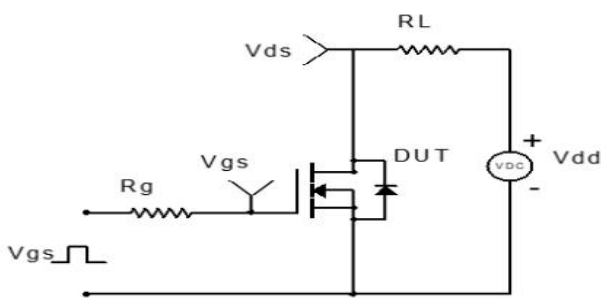


Figure 2: Resistive Switching Test Circuit & Waveform

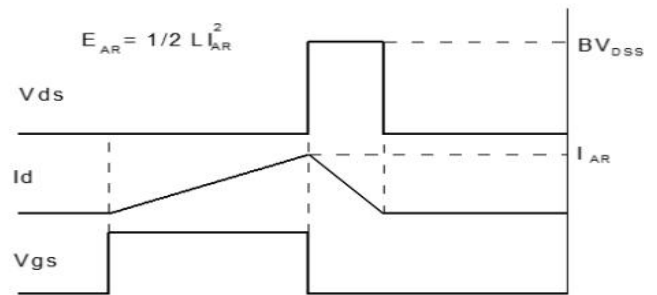
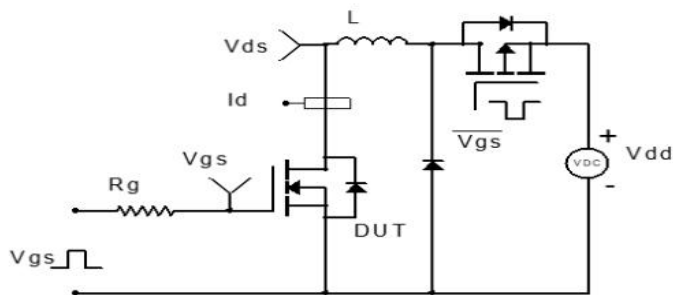


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

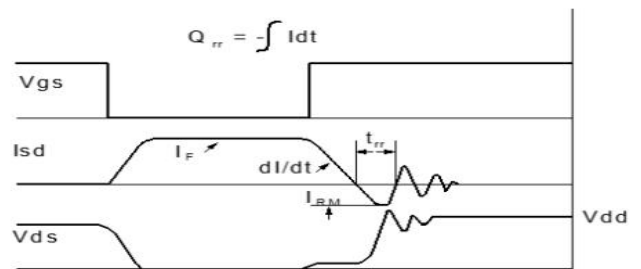
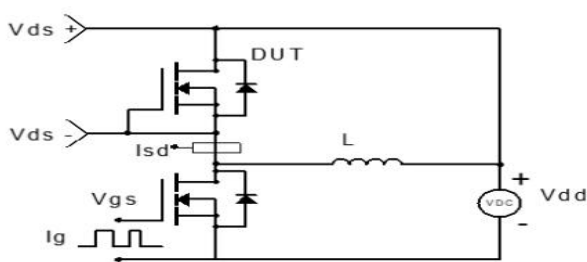
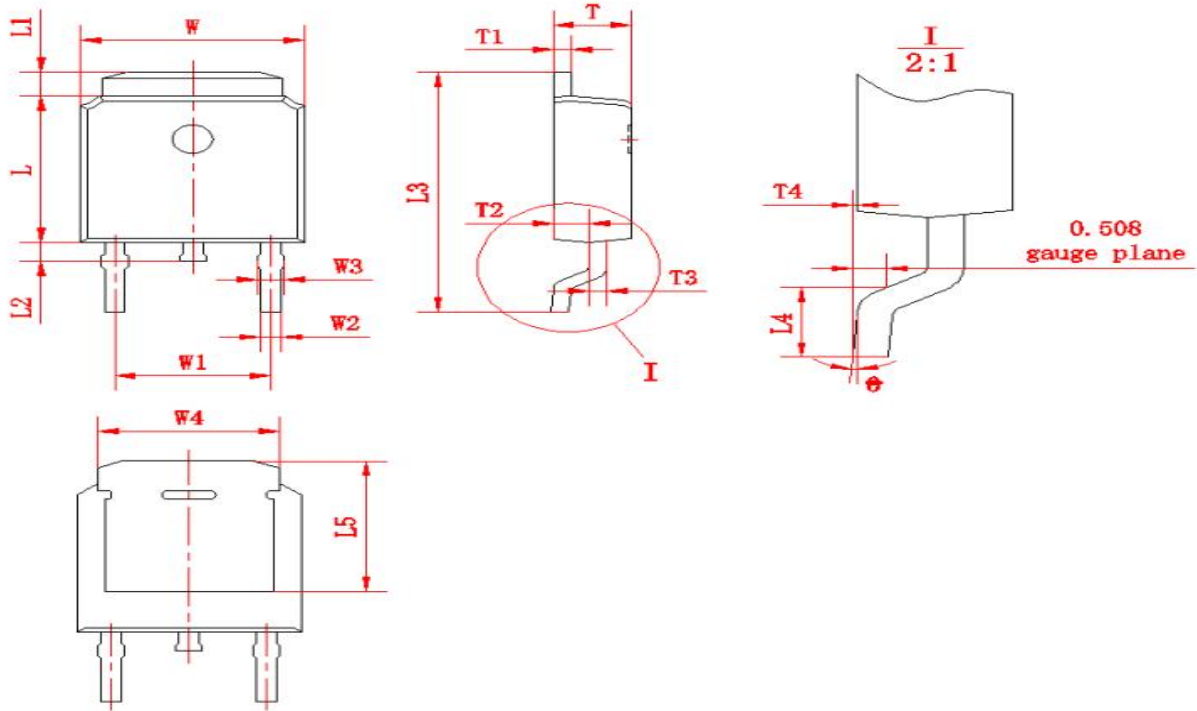


Figure 4: Diode Recovery Test Circuit & Waveform

Package outline drawing(TO-252 Unit: mm)



符号	尺寸		符号	尺寸		符号	尺寸	
	Min	Max		Min	Max		Min	Max
W	6.50	6.70	L1	0.80	1.20	T1	0.48	0.58
W1	(4.572)		L2	0.60	1.00	T2	0.95	1.15
W2	0.6	0.8	L3	9.70	10.30	T3	0.48	0.58
W3	0.68	0.88	L4	1.30	1.70	T4	0.00	0.12
W4	(5.3)		L5	(5.20)		0	0	8
L	6.00	6.20	T	2.20	2.40			

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