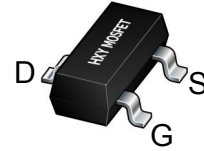




### Description

The DMG3401LSN uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.



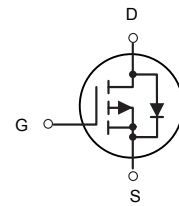
SOT-23

### General Features

$V_{DS} = -30V, I_D = -6A$   
 $R_{DS(ON)} < 35m\Omega @ V_{GS}=10V$

### Application

- High power and current handing capability
- Lead free product is acquired
- Surface mount package
- PWM applications
- Load switch
- Power management



P-Channel MOSFET

### Package Marking and Ordering Information

Product ID	Pack	Brand	Qty(PCS)
DMG3401LSN	SOT-23	HXY MOSFET	3000

### Absolute Maximum Ratings ( $T_A=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Limit	Unit
$V_{DS}$	Drain-Source Voltage	-30	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Drain Current-Continuous	-6	A
$I_{DM}$	Drain Current-Pulsed <sup>(Note 1)</sup>	-24	A
$P_D$	Maximum Power Dissipation	1.32	W
$T_J, T_{STG}$	Operating Junction and Storage Temperature Range	-55 To 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient <sup>(Note 2)</sup>	125	$^\circ C/W$



**Electrical Characteristics ( $T_J=25\text{ }^\circ\text{C}$ , unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-30	---	---	V
$\Delta BV_{DSS}/\Delta T$	$BV_{DSS}$ Temperature Coefficient	Reference to $25^\circ\text{C}$ , $I_D=-1\text{mA}$	---	-0.022	---	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=-10V, I_D=-4A$	---	28	35	$m\Omega$
		$V_{GS}=-4.5V, I_D=-2A$	---	40	55	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=-250\mu A$	-1.0	---	-2.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	4.6	---	$mV/^\circ\text{C}$
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS}=-24V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	1	$\mu A$
		$V_{DS}=-24V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	5	
$I_{GSS}$	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	$\pm 100$	nA
$g_{fs}$	Forward Transconductance	$V_{DS}=-5V, I_D=-4A$	---	15	---	S
$R_g$	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$	---	13	---	$\Omega$
$Q_g$	Total Gate Charge (-4.5V)	$V_{DS}=-15V, V_{GS}=-4.5V, I_D=-4A$	---	9.7	---	nC
$Q_{gs}$	Gate-Source Charge		---	2.5	---	
$Q_{gd}$	Gate-Drain Charge		---	3	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=-15V, V_{GS}=-10V, R_G=3.3\Omega, I_D=-4A$	---	16.4	---	ns
$T_r$	Rise Time		---	20.2	---	
$T_{d(off)}$	Turn-Off Delay Time		---	55	---	
$T_f$	Fall Time		---	10	---	
$C_{iss}$	Input Capacitance	$V_{DS}=-15V, V_{GS}=0V, f=1\text{MHz}$	---	750	---	pF
$C_{oss}$	Output Capacitance		---	150	---	
$C_{riss}$	Reverse Transfer Capacitance		---	127	---	
$I_S$	Continuous Source Current <sup>1,4</sup>	$V_G=V_D=0V, \text{Force Current}$	---	---	-6.0	A
$I_{SM}$	Pulsed Source Current <sup>2,4</sup>		---	---	-24	A
$V_{SD}$	Diode Forward Voltage <sup>2</sup>	$V_{GS}=0V, I_S=-1A, T_J=25^\circ\text{C}$	---	---	-1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F=-4A, dI/dt=100A/\mu s, T_J=25^\circ\text{C}$	---	18.3	---	nS
$Q_{rr}$	Reverse Recovery Charge		---	7.2	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch<sup>2</sup>FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$
- 3.The power dissipation is limited by  $150^\circ\text{C}$  junction temperature
- 4.The data is theoretically the same as  $I_D$  and  $I_{DM}$  , in real applications , should be limited by total power dissipation.



### Typical Characteristics

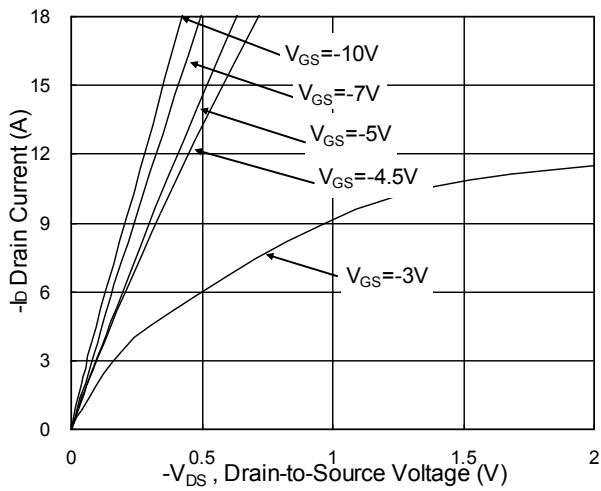


Fig.1 Typical Output Characteristics

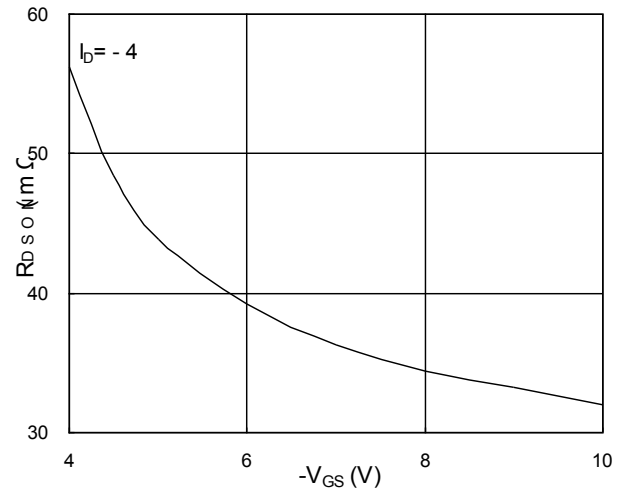


Fig.2 On-Resistance v.s Gate-Source

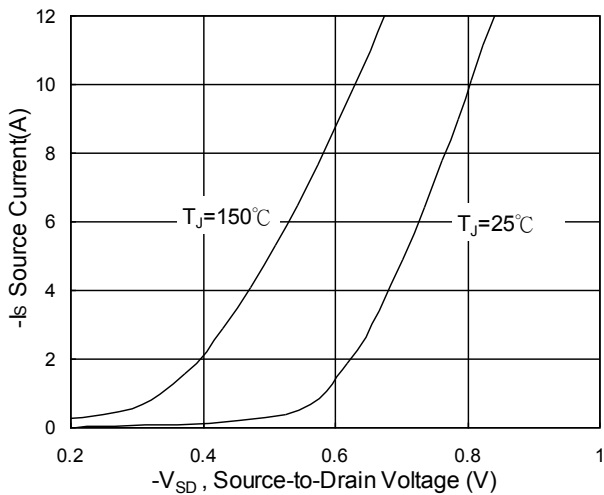


Fig.3 Forward Characteristics of Reverse

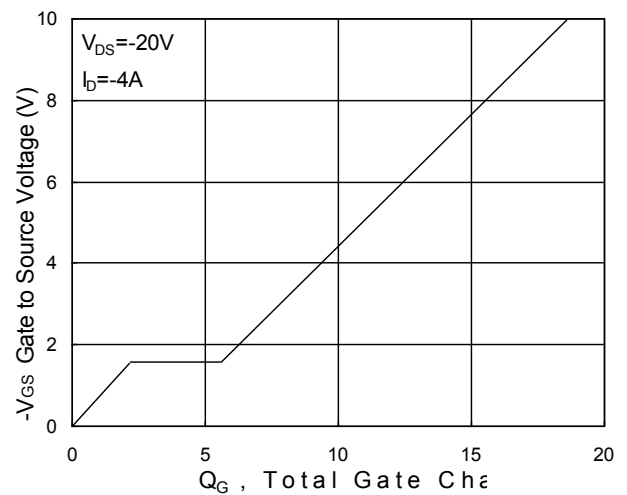


Fig.4 Gate-Charge Characteristics

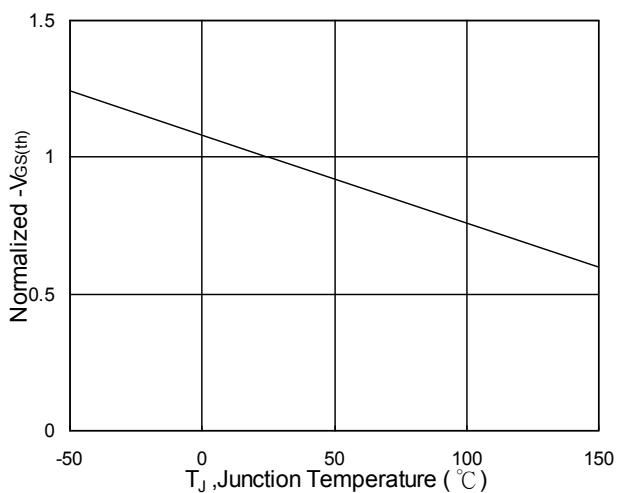


Fig.5 Normalized  $V_{GS(th)}$  v.s  $T_J$

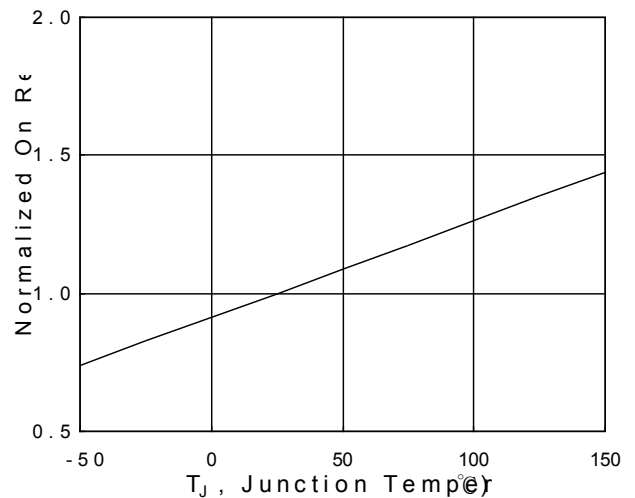


Fig.6 Normalized  $R_{DS(on)}$  v.s  $T_J$

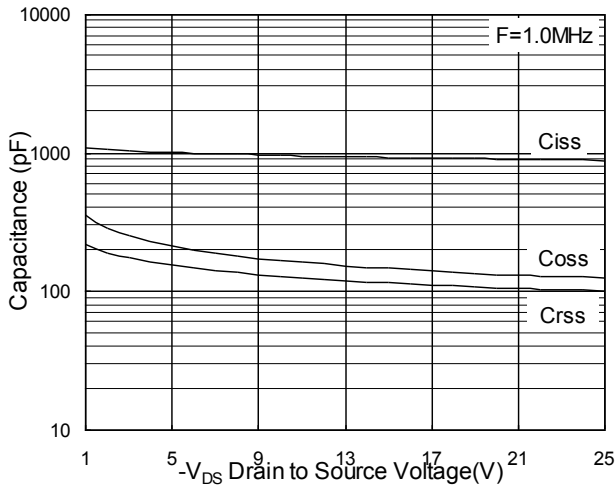


Fig.7 Capacitance

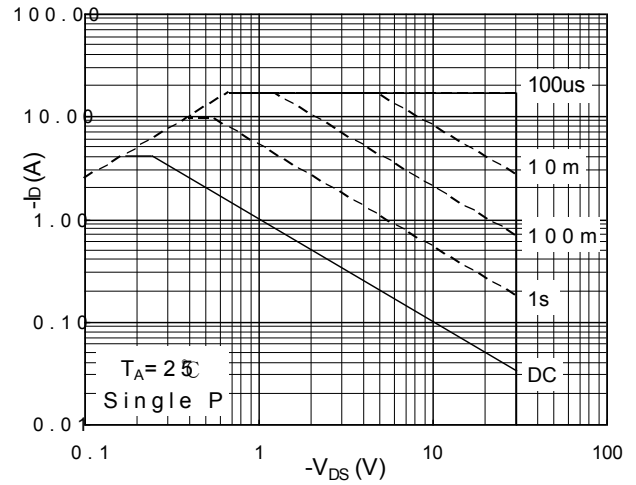


Fig.8 Safe Operating Area

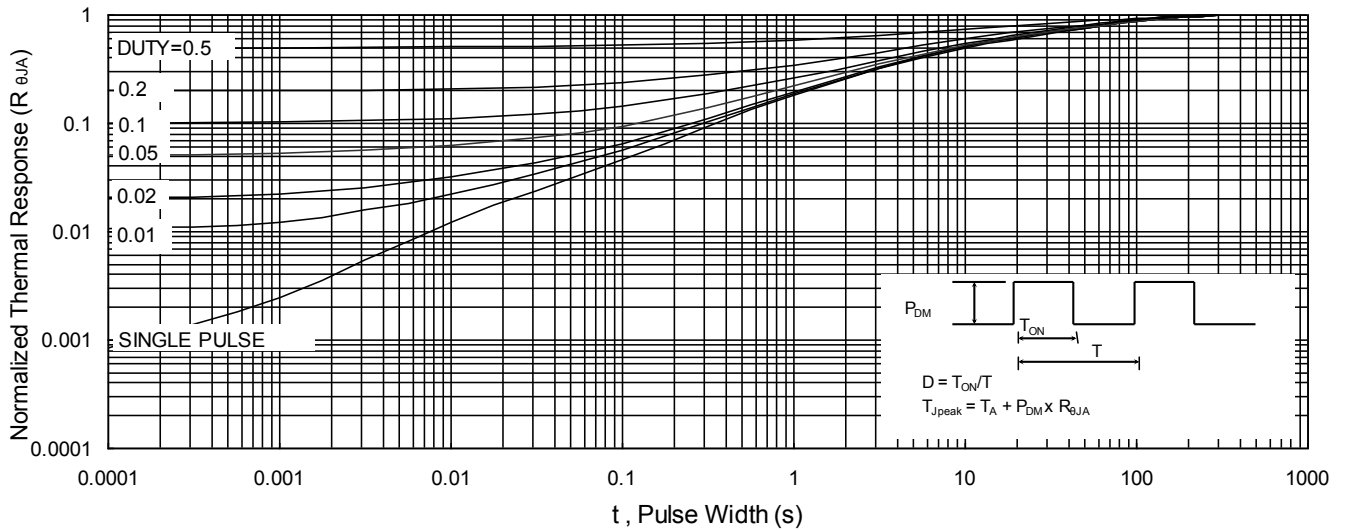


Fig.9 Normalized Maximum Transient Thermal Impedance



Fig.10 Switching Time Waveform

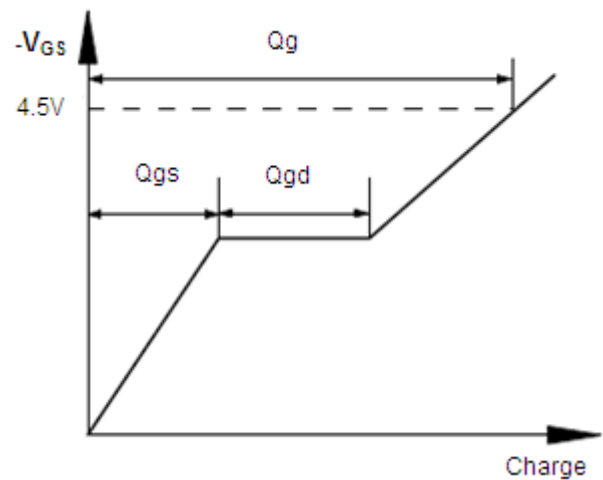
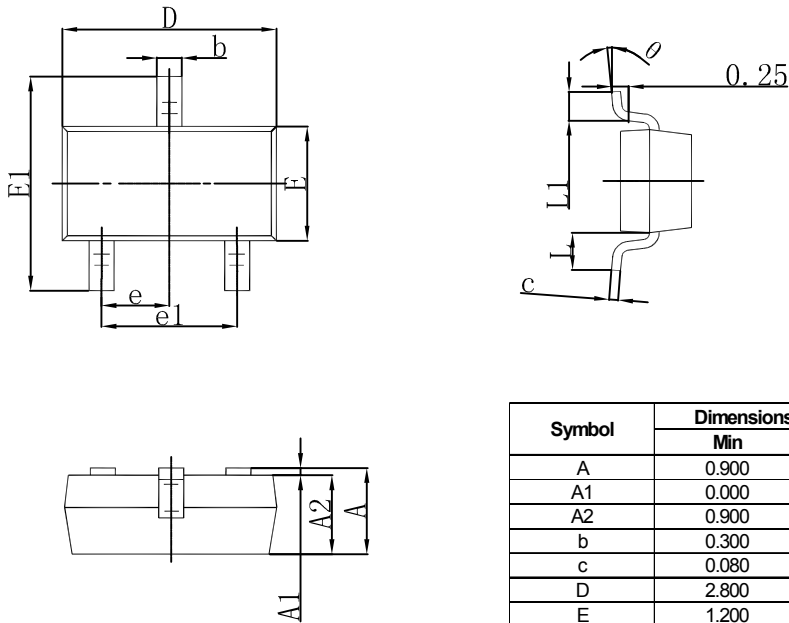


Fig.11 Gate Charge Waveform

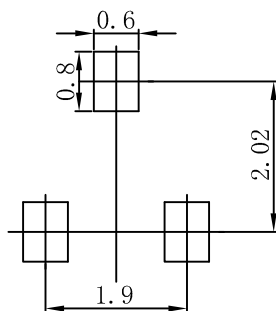


### SOT-23 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP		0.037 TYP	
e1	1.800	2.000	0.071	0.079
L	0.550 REF		0.022 REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°

### SOT-23 Suggested Pad Layout



- Note:
1. Controlling dimension: in millimeters.
  2. General tolerance:  $\pm 0.05\text{mm}$ .
  3. The pad layout is for reference purposes only.



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