

## N-Channel 60-V (D-S) MOSFET

### PRODUCT SUMMARY

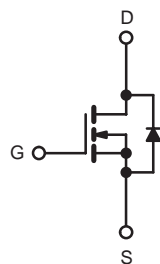
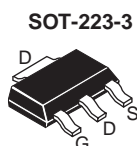
$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A) <sup>a</sup>	$Q_g$ (Typ.)
60	0.076 at $V_{GS} = 10$ V	4.5	10 nC
	0.085 at $V_{GS} = 4.5$ V	3.5	

### FEATURES

- Halogen-free
- TrenchFET<sup>®</sup> Power MOSFET

### APPLICATIONS

- Load Switches for Portable Devices


**RoHS**  
 COMPLIANT


N-Channel MOSFET

### ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 150$ °C)	$I_D$	4.5	A
		3.2 <sup>a</sup>	
		2.7	
		2.3	
Pulsed Drain Current	$I_{DM}$	20	W
Continuous Source-Drain Diode Current	$I_S$	3.2	
		2.1 <sup>b, c</sup>	
Maximum Power Dissipation	$P_D$	4.0	
		3.0	
		2.5 <sup>b, c</sup>	
		1.6 <sup>b, c</sup>	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) <sup>e, f</sup>		260	

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>a, c, d</sup>	$R_{thJA}$	40	50	°C/W
Maximum Junction-to-Foot (Drain)	$R_{thJF}$	15	20	

Notes:

 a. Package limited,  $T_C = 25$  °C.

b. Surface Mounted on 1" x 1" FR4 board.

 c.  $t = 10$  s.

d. Maximum under Steady State conditions is 95 °C/W.

e. See Reliability Manual for profile. The ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

f. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

SPECIFICATIONS T <sub>J</sub> = 25 °C, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	60			V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA		25		mV/°C
V <sub>GS(th)</sub> Temperature Coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>			- 4.0		
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1.0		2.5	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 12 V			± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V			1	μA
		V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			10	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 5 V, V <sub>GS</sub> = 4.5 V	30			A
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 4.0 A		0.076		Ω
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 3.0 A		0.085		
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 4.0 A		45		S
Dynamic <sup>b</sup>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 30V, V <sub>GS</sub> = 0 V, f = 1 MHz		810		pF
Output Capacitance	C <sub>oss</sub>			120		
Reverse Transfer Capacitance	C <sub>rss</sub>			100		
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 4.0 A		22	33	nC
		V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 3.0 A		10	15	
Gate-Source Charge	Q <sub>gs</sub>			2.5		
Gate-Drain Charge	Q <sub>gd</sub>			1.7		
Gate Resistance	R <sub>g</sub>	f = 1 MHz		2.4		Ω
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =30V, , R <sub>L</sub> = 1.5 Ω I <sub>D</sub> ≅ 4.0 A, V <sub>GEN</sub> = 4.5 V, R <sub>g</sub> = 1 Ω		15	25	ns
Rise Time	t <sub>r</sub>			10	15	
Turn-Off Delay Time	t <sub>d(off)</sub>			35	55	
Fall Time	t <sub>f</sub>			12	20	
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 30V, R <sub>L</sub> = 1.5 Ω I <sub>D</sub> ≅ 4.0 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω		10	15	
Rise Time	t <sub>r</sub>			12	20	
Turn-Off Delay Time	t <sub>d(off)</sub>			25	40	
Fall Time	t <sub>f</sub>			10	15	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			7.2	A
Pulse Diode Forward Current	I <sub>SM</sub>				30	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = 4.0 A, V <sub>GS</sub> = 0 V		0.8	1.2	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 4.0 A, dI/dt = 100 A/μs, T <sub>J</sub> = 25 °C		20	40	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			10	20	nC
Reverse Recovery Fall Time	t <sub>a</sub>			10		ns
Reverse Recovery Rise Time	t <sub>b</sub>			10		

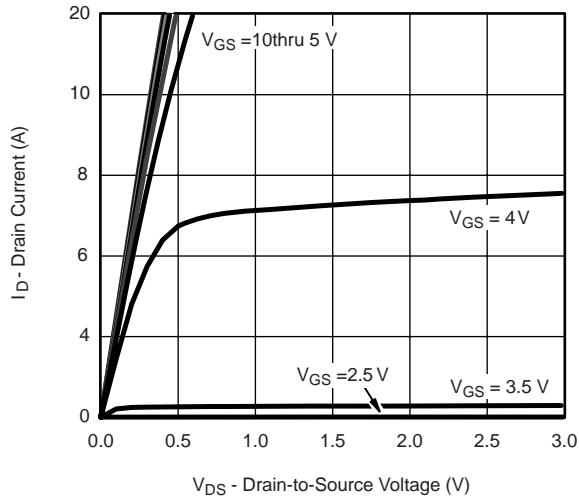
Notes:

a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ 

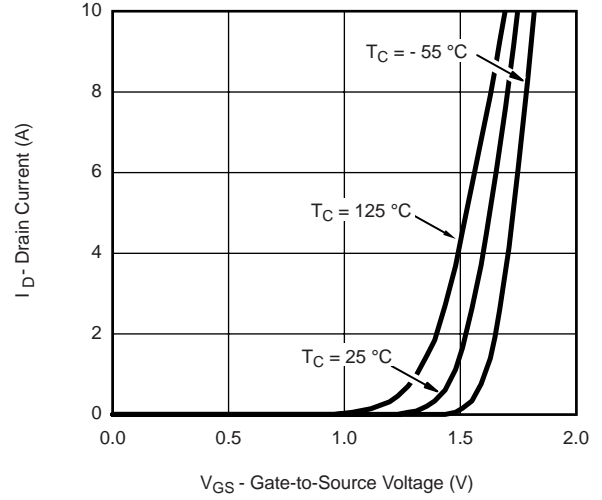
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

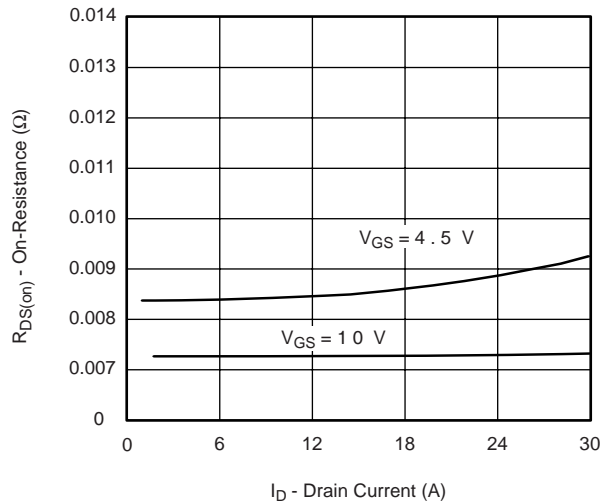
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



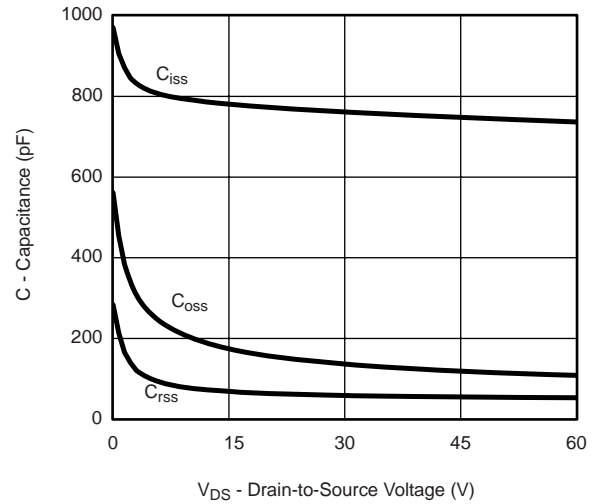
**Output Characteristics**



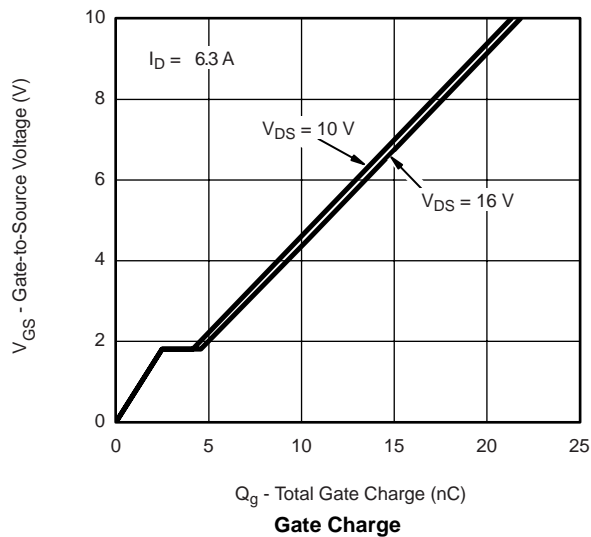
**Transfer Characteristics**



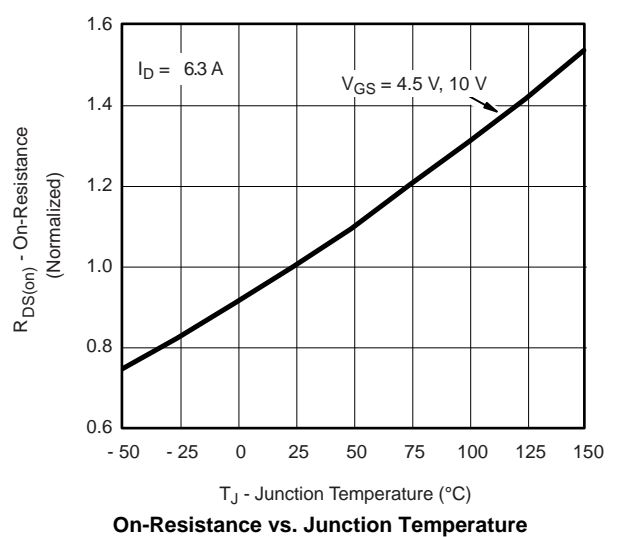
**On-Resistance vs. Drain Current**



**Capacitance**

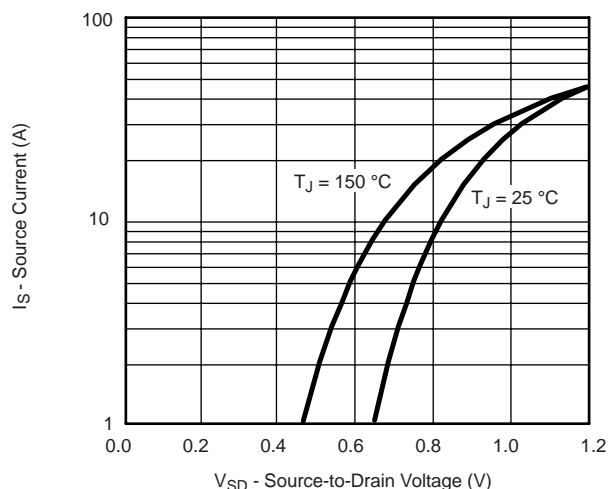


**Gate Charge**

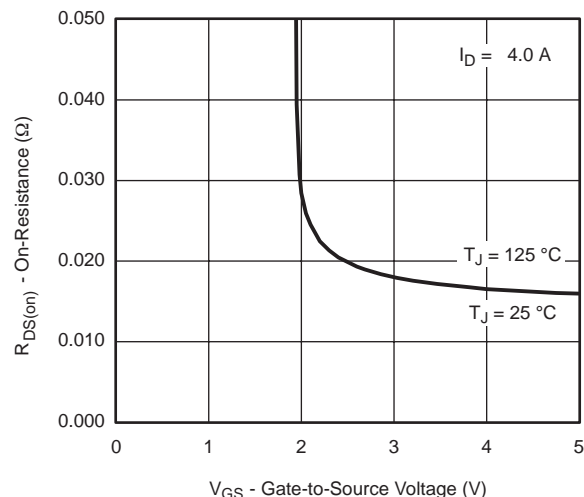


**On-Resistance vs. Junction Temperature**

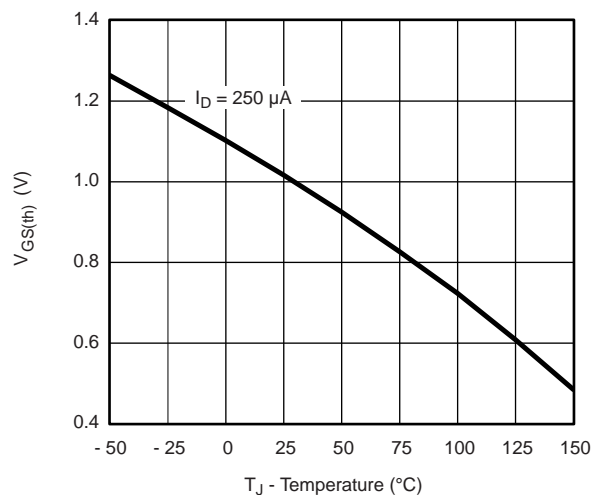
## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



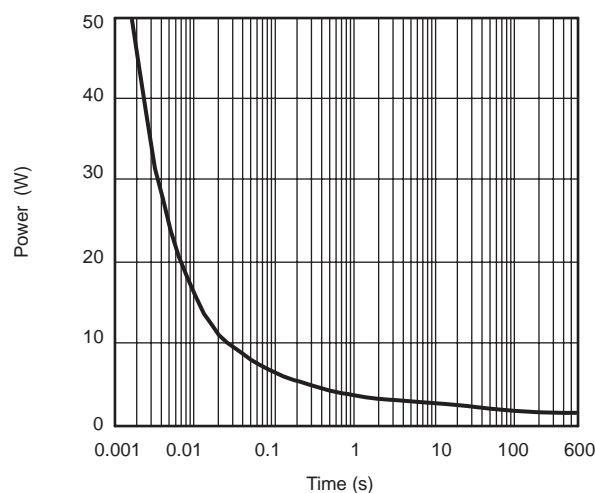
Source-Drain Diode Forward Voltage



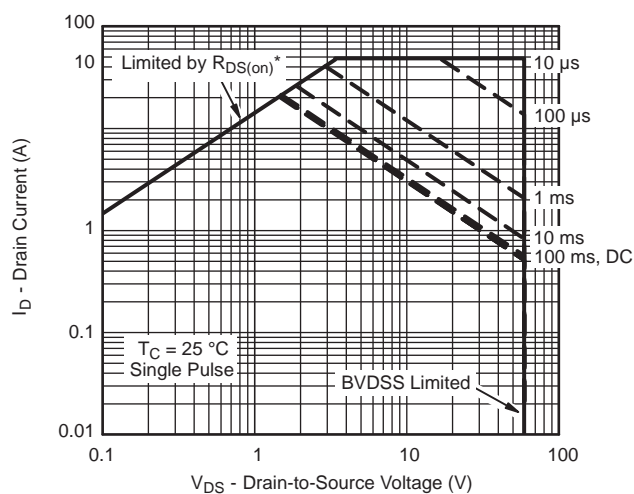
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



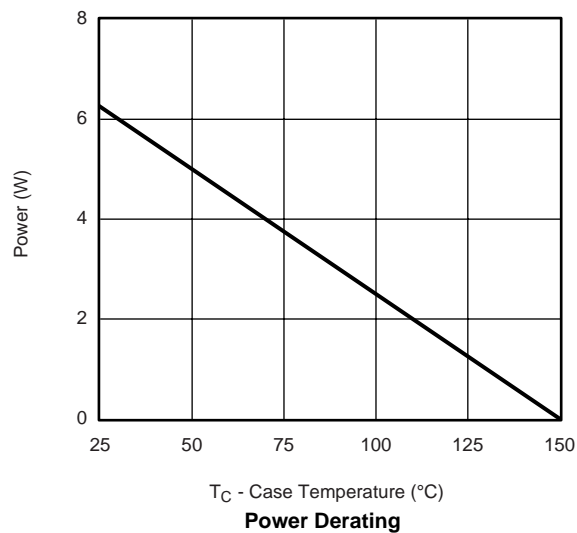
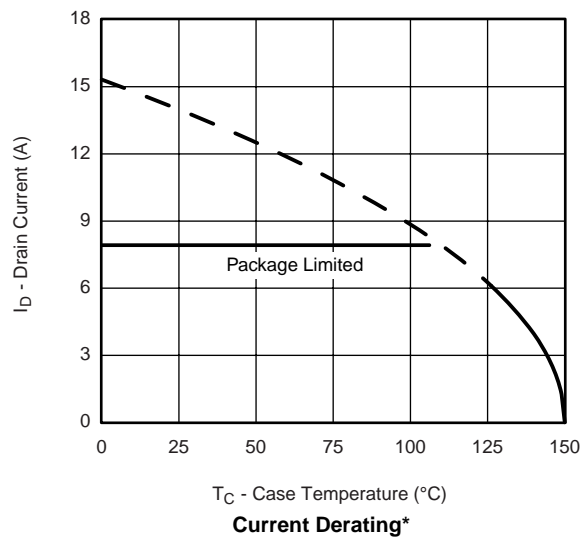
Single Pulse Power



\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

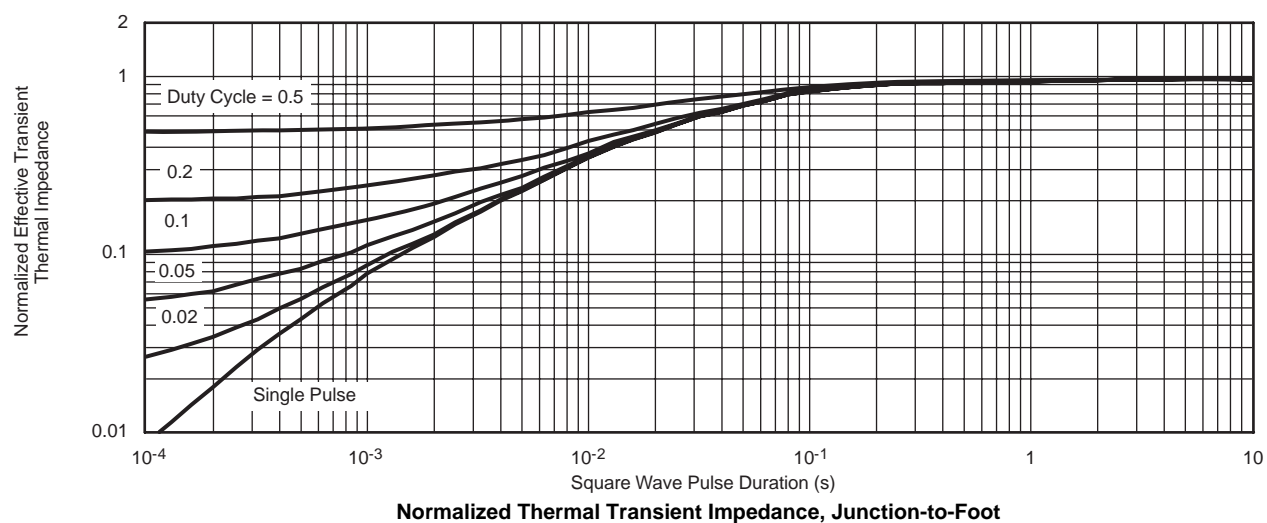
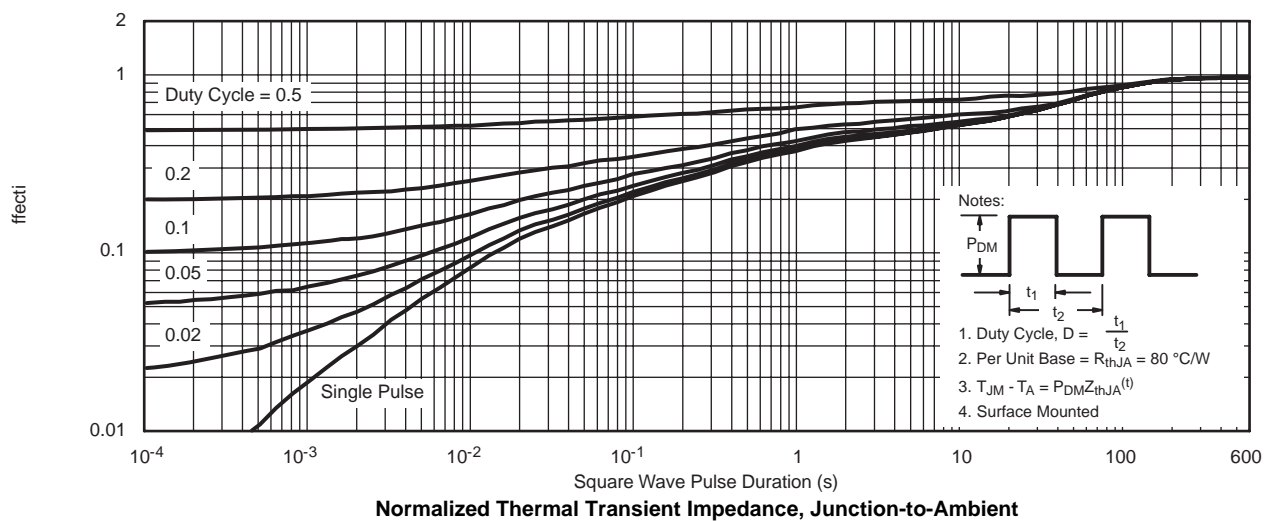
Single Pulse Power, Junction-to-Case

## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

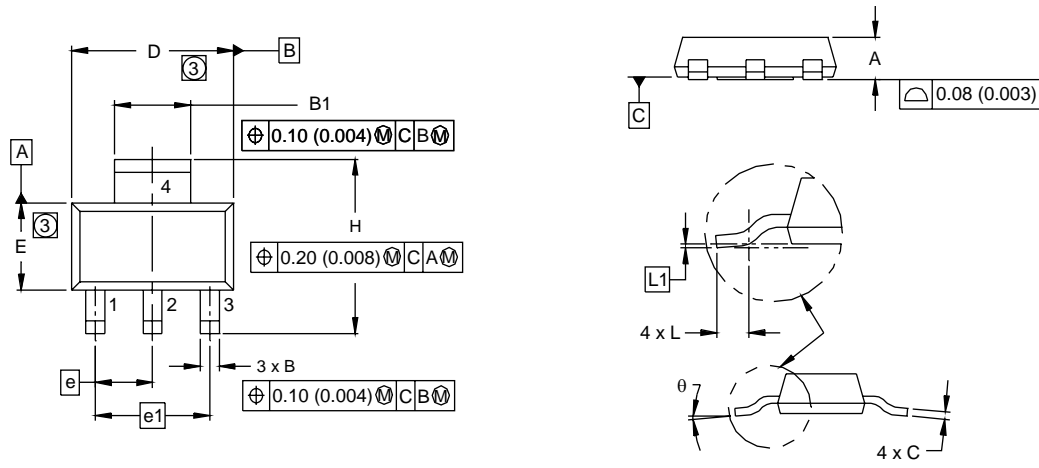


\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



**SOT-223 (HIGH VOLTAGE)**



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	1.55	1.80	0.061	0.071
B	0.65	0.85	0.026	0.033
B1	2.95	3.15	0.116	0.124
C	0.25	0.35	0.010	0.014
D	6.30	6.70	0.248	0.264
E	3.30	3.70	0.130	0.146
e	2.30 BSC		0.0905 BSC	
e1	4.60 BSC		0.181 BSC	
H	6.71	7.29	0.264	0.287
L	0.91	-	0.036	-
L1	0.061 BSC		0.0024 BSC	
θ	-	10°	-	10°
ECN: S-82109-Rev. A, 15-Sep-08 DWG: 5969				

**Notes**

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension do not include mold flash.
4. Outline conforms to JEDEC outline TO-261AA.

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