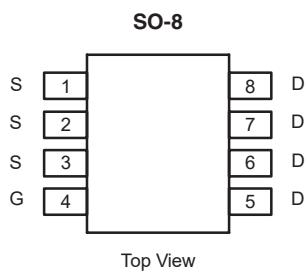


N-Channel 40-V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^d	Q_g (Typ.)
40	0.014 at $V_{GS} = 10$ V	10	15 nC
	0.016 at $V_{GS} = 4.5$ V	9	

FEATURES

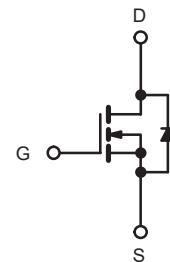
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- 100 % R_g Tested
- 100 % UIS Tested
- Compliant to RoHS directive 2002/95/EC



Top View

APPLICATIONS

- Synchronous Rectification
- POL, IBC
 - Secondary Side



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V_{DS}	40	V	
Gate-Source Voltage	V_{GS}	± 20		
Continuous Drain Current ($T_J = 150$ °C)	I_D	10	A	
		8		
		10.4 ^{a, b}		
		8.8 ^{a, b}		
Pulsed Drain Current	I_{DM}	50		
Avalanche Current	I_{AS}	15		
Avalanche Energy	E_{AS}	11	mJ	
Continuous Source-Drain Diode Current	I_S	5	A	
		2.1 ^{a, b}		
Maximum Power Dissipation	P_D	6	W	
		3.8		
		2.5 ^{a, b}		
		1.6 ^{a, b}		
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, c}	R_{thJA}	37	50	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	17	21

Notes:

- Surface Mounted on 1" x 1" FR4 board.
- $t = 10$ s.
- Maximum under Steady State conditions is 85 °C/W.
- Based on $T_C = 25$ °C.

SPECIFICATIONS $T_J = 25^\circ\text{C}$, unless otherwise noted

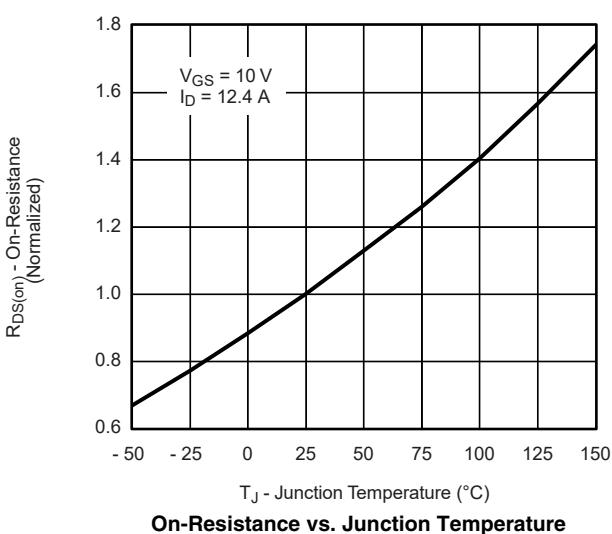
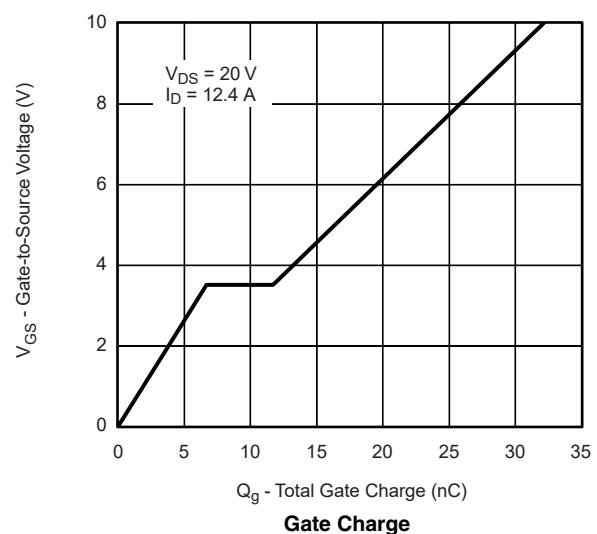
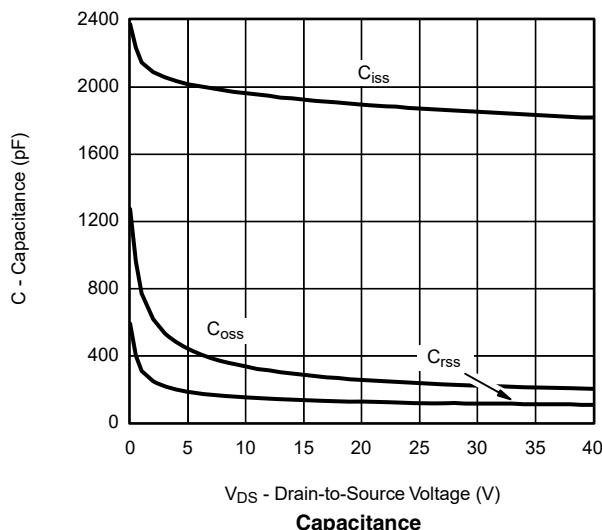
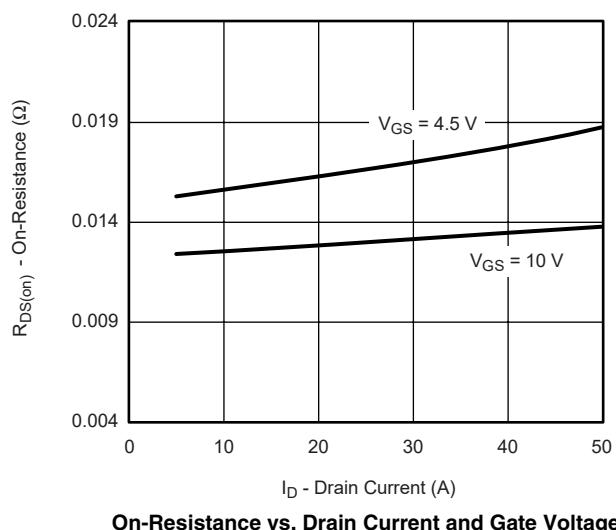
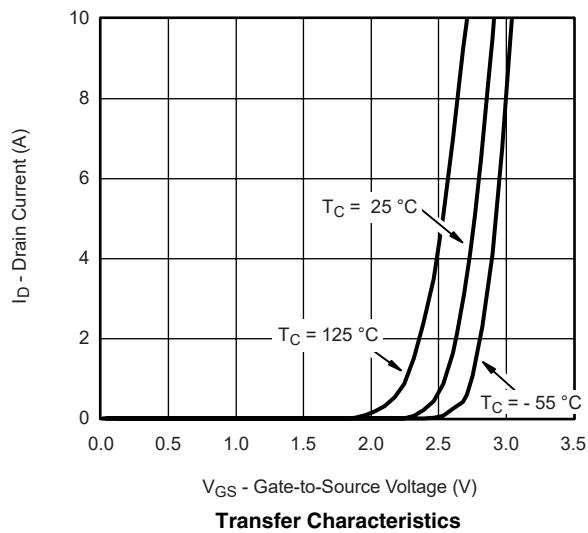
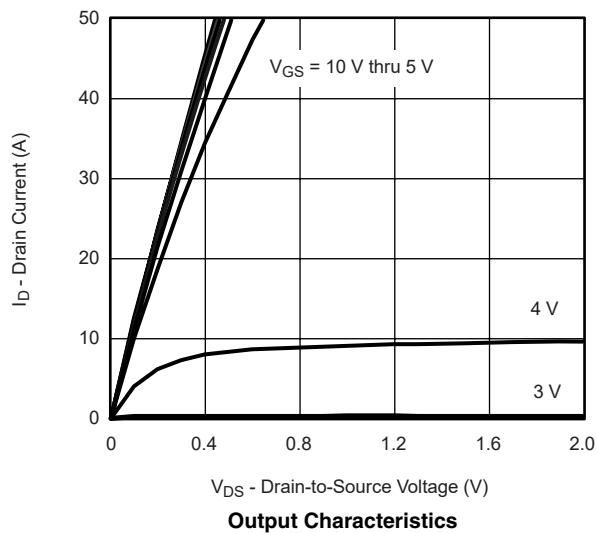
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}$, $I_D = 250 \mu\text{A}$	40			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250 \mu\text{A}$		40		$\text{mV}/^\circ\text{C}$
$V_{GS(\text{th})}$ Temperature Coefficient	$\Delta V_{GS(\text{th})}/T_J$			- 6		
Gate-Source Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$	1		3	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}$, $V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 40 \text{ V}$, $V_{GS} = 0 \text{ V}$			1	μA
		$V_{DS} = 40 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 55^\circ\text{C}$			5	
On-State Drain Current ^a	$I_{D(\text{on})}$	$V_{DS} \geq 5 \text{ V}$, $V_{GS} = 10 \text{ V}$	50			A
Drain-Source On-State Resistance ^a	$R_{DS(\text{on})}$	$V_{GS} = 10 \text{ V}$, $I_D = 12.4 \text{ A}$		0.014		Ω
		$V_{GS} = 4.5 \text{ V}$, $I_D = 10.8 \text{ A}$		0.016		
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15 \text{ V}$, $I_D = 12.4 \text{ A}$		56		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 20 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$		2000		pF
Output Capacitance	C_{oss}			260		
Reverse Transfer Capacitance	C_{rss}			150		
Total Gate Charge	Q_g	$V_{DS} = 10 \text{ V}$, $V_{GS} = 10 \text{ V}$, $I_D = 12.4 \text{ A}$		33	50	nC
Gate-Source Charge	Q_{gs}			15	23	
Gate-Drain Charge	Q_{gd}			6.7		
Gate Resistance	R_g		$f = 1 \text{ MHz}$	5.1		
Turn-On Delay Time	$t_{d(\text{on})}$	$V_{DD} = 20 \text{ V}$, $R_L = 2 \Omega$ $I_D \cong 10 \text{ A}$, $V_{GEN} = 4.5 \text{ V}$, $R_g = 1 \Omega$		1.4	2.1	Ω
Rise Time	t_r			25	40	
Turn-Off Delay Time	$t_{d(\text{off})}$			12	20	
Fall Time	t_f			25	40	
Turn-On Delay Time	$t_{d(\text{on})}$			10	15	
Rise Time	t_r			10	15	
Turn-Off Delay Time	$t_{d(\text{off})}$			15	25	
Fall Time	t_f			30	45	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25^\circ\text{C}$			30	A
Pulse Diode Forward Current	I_{SM}				50	
Body Diode Voltage	V_{SD}	$I_S = 10 \text{ A}$, $V_{GS} = 0 \text{ V}$		0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 10 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $T_J = 25^\circ\text{C}$		30	60	ns
Body Diode Reverse Recovery Charge	Q_{rr}			26	52	
Reverse Recovery Fall Time	t_a			17.5		ns
Reverse Recovery Rise Time	t_b			12.5		

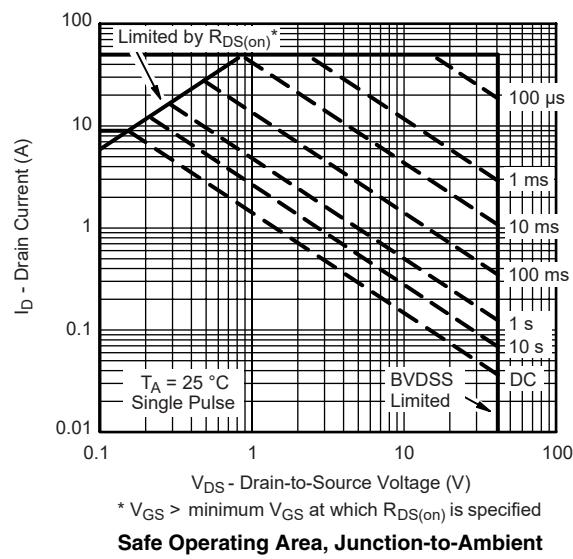
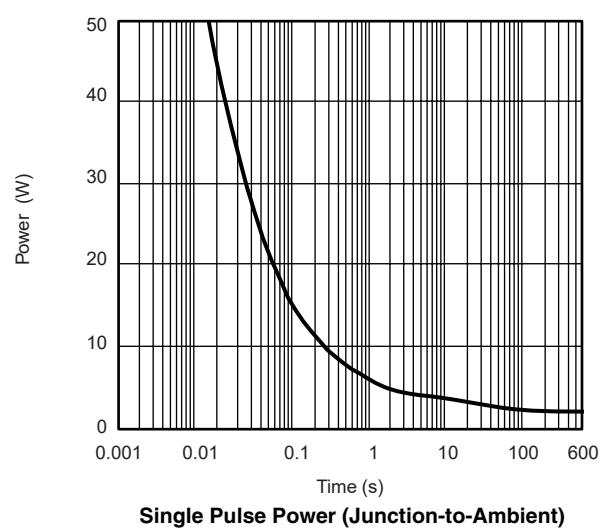
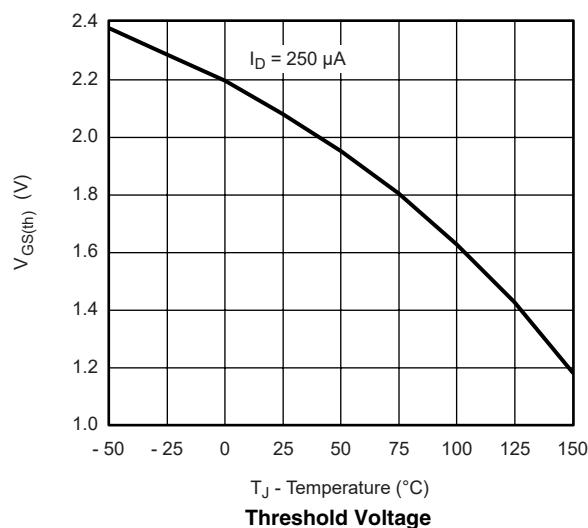
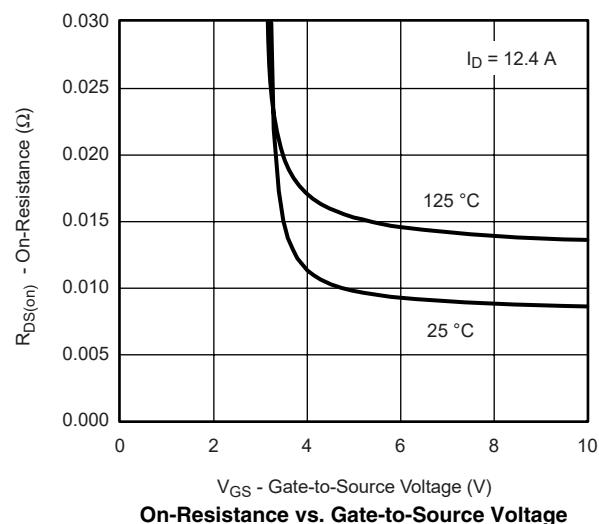
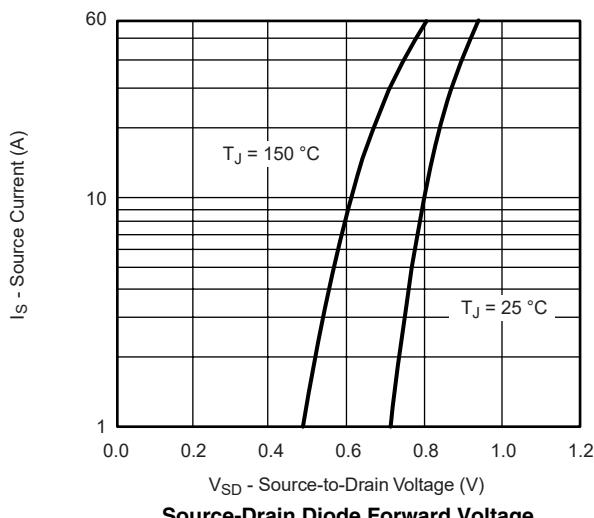
Notes:

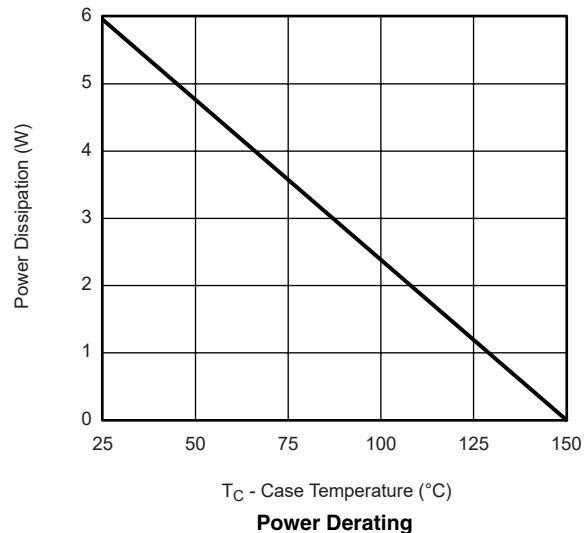
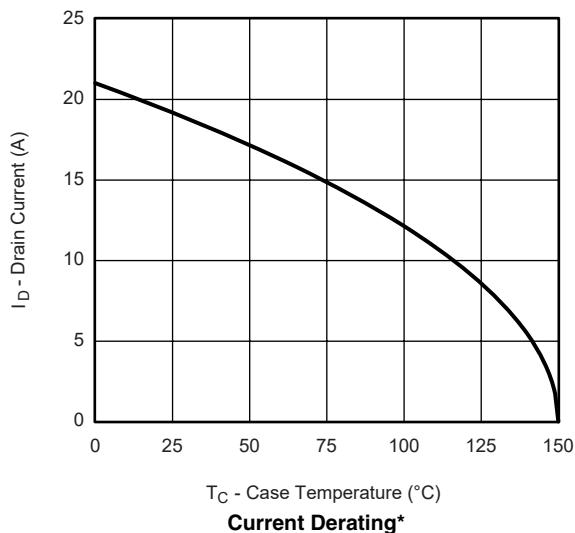
a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$

b. Guaranteed by design, not subject to production testing.

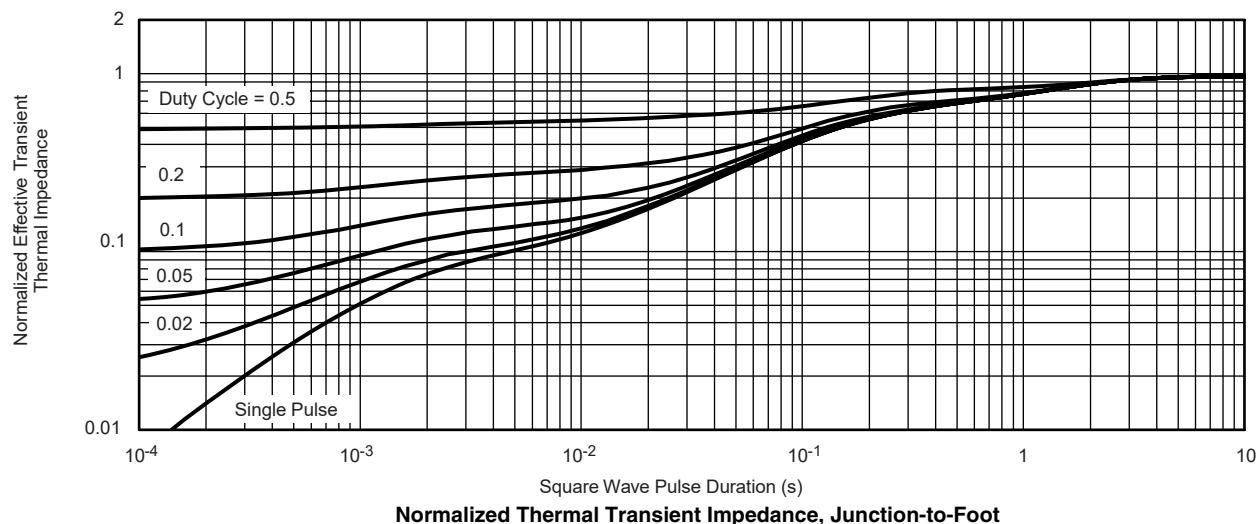
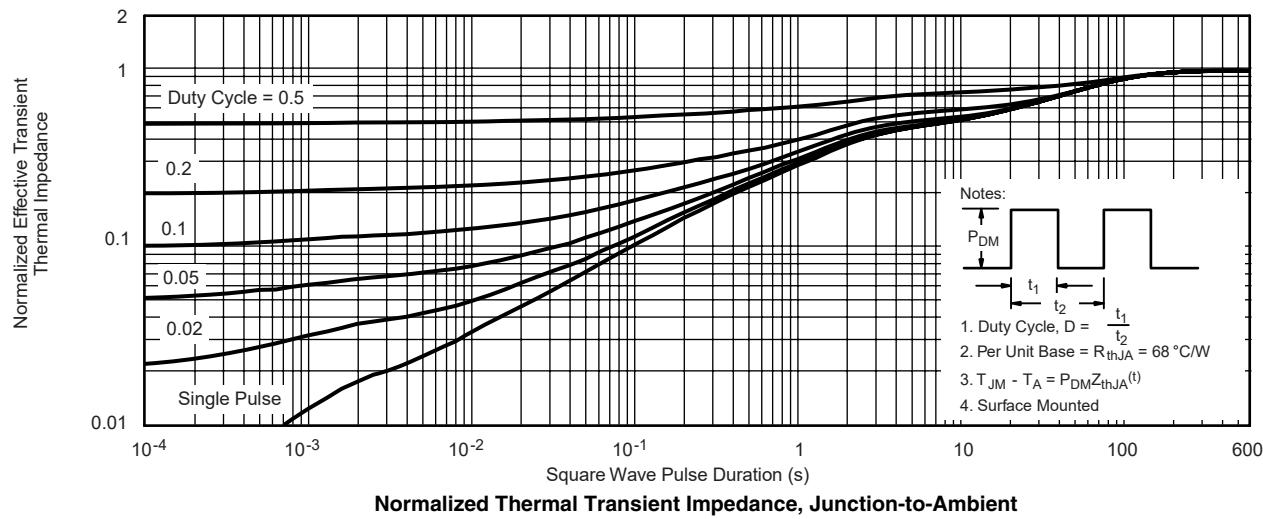
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted


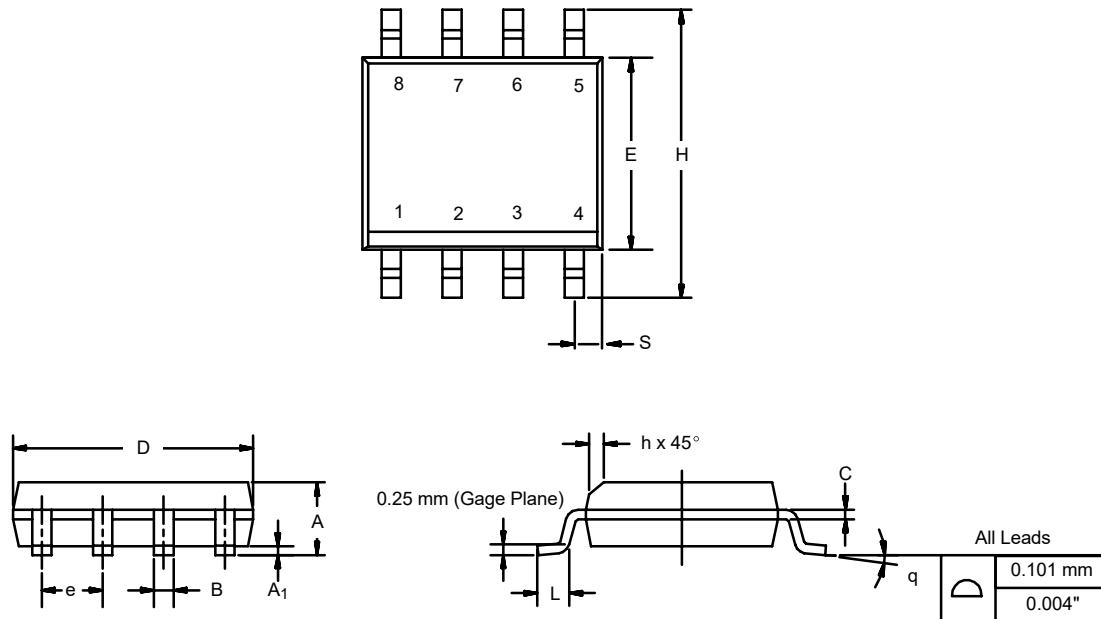
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

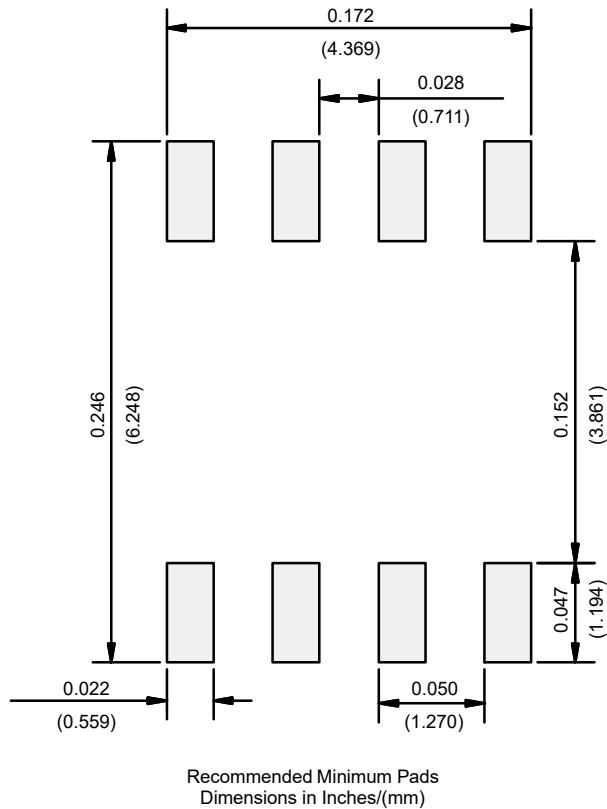
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted


SOIC (NARROW): 8-LEAD
 JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				

RECOMMENDED MINIMUM PADS FOR SO-8



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