■ ABSOLUTE MAXIMUM RATINGS[1]

(Unless otherwise specified, T_A=25°C)

PARAMETER	SYMBOL	RATINGS	UNITS
Input Voltage[2]	V_{IN}	-0.3~65	V
Output Voltage[2]	V_{OUT}	-0.3~15	V
CE Pin Voltage[2]	V_{CE}	-0.3~V_{IN}+0.3	V
Output Current	I_{OUT}	400	mA
Power Dissipation		600	mW
Operating Junction Temperature Range	T_j	-40~125	°C
Storage Temperature	T_{stg}	-40~125	°C
Lead Temperature(Soldering, 10 sec)	T_{solder}	260	°C
ESD rating[3]	Human Body Model-(HBM)	2	kV
	Machine Model- (MM)	200	V

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.

(2)All voltages are with respect to network ground terminal.

(3)ESD testing is performed according to the respective JESD22 JEDEC standard.The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin. The machine model is a 200pFcapacitor discharged directly into each pin.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN.	NOM.	MAX.	UNITS
Supply voltage at V_{IN}	2.5		60	V
Operating junction temperature range, T_j	-40		125	°C
Operating free air temperature range, T_A	-40		85	°C

■ MODEL DEFINITION INFORMATION

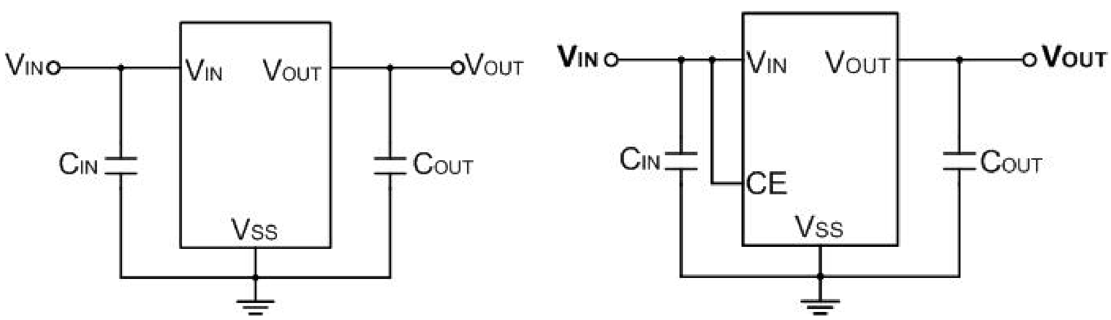
Model	Output Voltage
CJ8833	3.3V
CJ8850	5.0V
CJ88120	12V

Electrical Characteristics

(V_{CE}=V_{IN}=V_{OUT}+2V, C_{IN}=C_{OUT}=1μF, T_A=25℃,unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Voltage	V_{IN}		2.5	—	60	V
Output Voltage Range	V_{OUT}		1.2	—	12	V
DC Output Accuracy		I_{OUT}=1mA	-2	—	2	%
			-1	—	1	%
Dropout Voltage	V_{dif}	I_{OUT} =50mA,V_{OUT}=3.3V	—	500	—	mV
Supply Current	I_{SS}	I_{OUT}=0A, V_{OUT}≤5.0V	—	3	6	μA
		I_{OUT}=0A, V_{OUT}>5.0V		5	10	μA
Standby Current	I_{STBY}	CE = V_{SS}		0.1	0.5	μA
Line Regulation	$\frac{\Delta V_{OUT}}{V_{OUT} \times \Delta V_{IN}}$	I_{OUT} =10mA V_{OUT} +1V≤V_{IN}≤18V	—	0.01	0.3	%/V
Load Regulation	ΔV_{OUT}	V_{IN}= V_{OUT} +1V, 1mA≤I_{OUT}≤100mA	—	10	—	mV
Temperature Coefficient	$\frac{\Delta V_{OUT}}{V_{OUT} \times \Delta T_A}$	I_{OUT}=10mA, -40°C<T_A<125°C		50		ppm
Output Current Limit	I_{LIM}	V_{OUT}= 0.5 x $V_{OUT(Normal)}$, V_{IN} = 5V	150	250		mA
Short Current	I_{SHORT}	V_{OUT} =V_{SS}	—	20	—	mA
Power Supply Rejection Ratio	PSRR	I_{OUT}=50mA, 100Hz		75		dB
		I_{OUT}=50mA, 1kHz	—	80	—	dB
		I_{OUT}=50mA, 10kHz	—	60	—	dB
		I_{OUT}=50mA, 100kHz	—	45	—	dB
Output Noise Voltage	V_{ON}	BW=10Hz to 100kHz	—	27 x V_{OUT}	—	μV_{RMS}
Thermal Shutdown Temperature	T_{SD}	——	—	170	—	°C
Thermal Shutdown Hysteresis	ΔT_{SD}	——	—	20	—	°C
CE "High" Voltage	V_{CE}“H”		1.5		V_{IN}	V
CE "Low" Voltage	V_{CE}“L”				0.3	V

■ TYPICAL APPLICATION CIRCUIT



C_{IN} :1.0μF or more

C_{OUT} :1.0μF or more，10μF is recommended

APPLICATION INFORMATION

Selection of Input/ Output Capacitors

Phase compensation is provided to secure operation even when the load current is varied. For this purpose, use a 1.0μF or more output capacitor (C_{OUT}) with good frequency characteristics and proper ESR (Equivalent Series Resistance). Connect a 1.0μF or more input capacitor (C_{IN}) between the V_{IN} pin and the V_{SS} pin as close as possible to the pins.
The value of the output overshoot or undershoot transient response varies depending on the value of the output capacitor.
When selecting the output capacitor, perform sufficient evaluation, including evaluation of temperature characteristics, on the actual device.

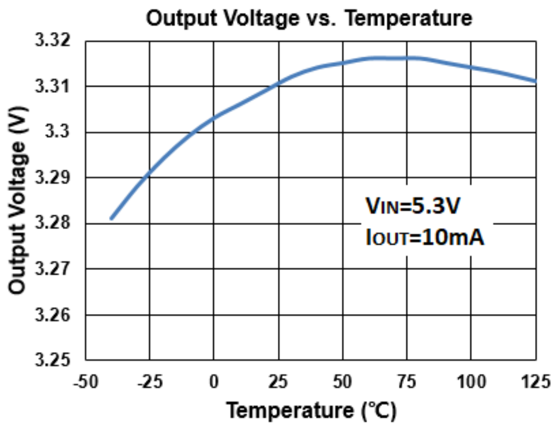
In the design of portable devices the ceramic capacitors are often chosen because of their small size, low equivalent series resistance (ESR) and high RMS current capability. Also, designers have been looking to ceramic capacitors due to shortages of tantalum capacitors.

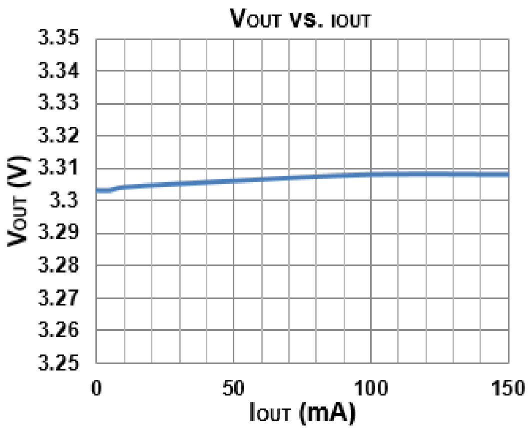
Unfortunately, using ceramic capacitors for input filtering can cause problems. Applying a voltage step to a ceramic capacitor causes a large current surge that stores energyin the inductances of the power leads. A large voltage spike is created when the stored energy is transferred from these inductances into the ceramic capacitor. These voltagespikes can easily be twice the amplitude of the input voltage step.

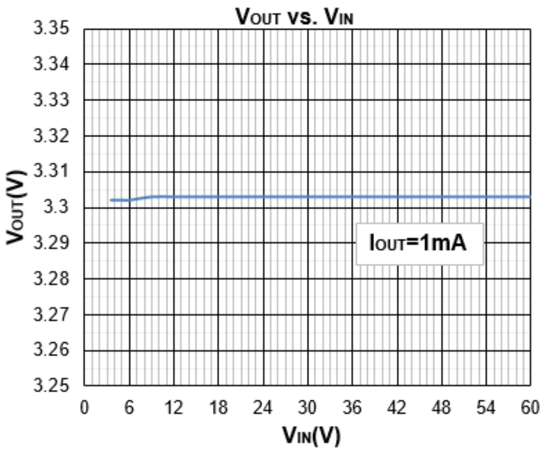
Many types of capacitors can be used for input bypassing, however, caution must be exercised when using multilayer ceramic capacitors (MLCC). Because of the self-resonant and high Q characteristics of some types of ceramic capacitors, high voltage transients can be generated under some start-up conditions, such as connecting the LDO input to a live power source. Adding a 3Ω resistor in series with an X5R ceramic capacitor will minimize start-up voltage transients.

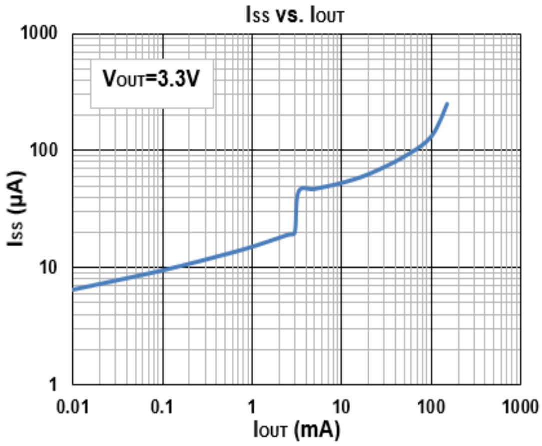
Typical Characteristics

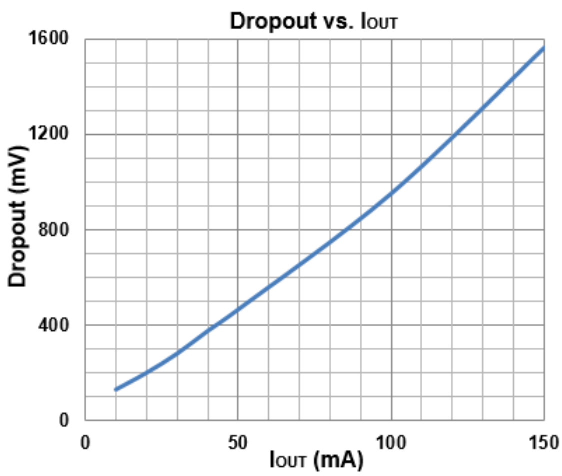
(V_{CE}=V_{IN}=V_{OUT}+2V, C_{IN}=1μF, C_{OUT}=10μF , T_A=25℃,unless otherwise specified)

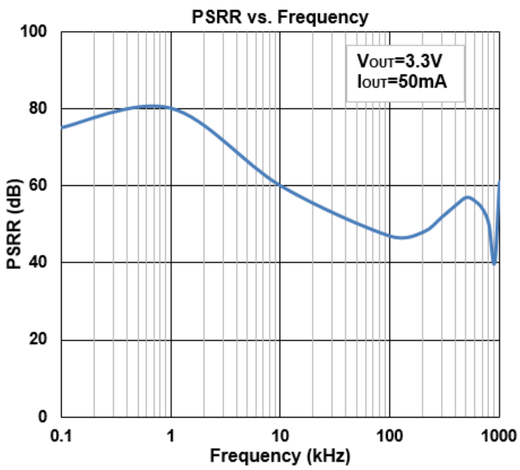






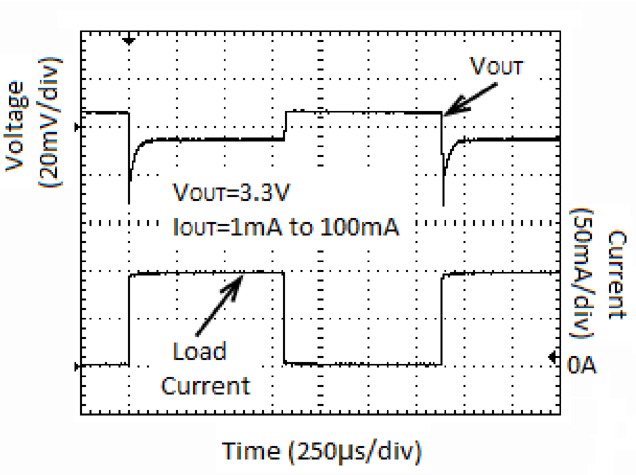


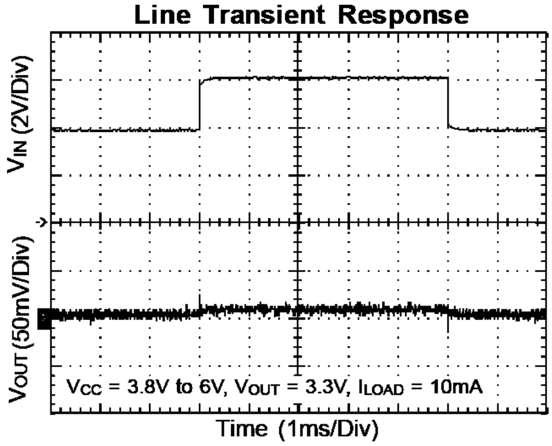


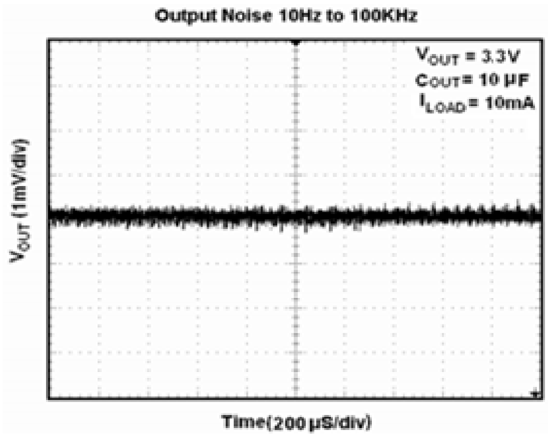


Typical Characteristics

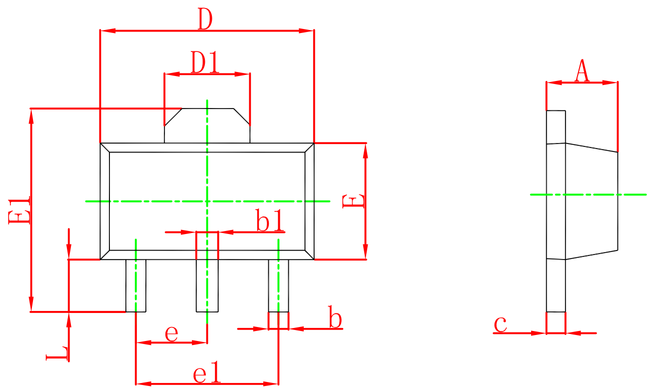
(V_{CE}=V_{IN}=V_{OUT}+2V, C_{IN}=1μF, C_{OUT}=10μF , T_A=25℃,unless otherwise specified)





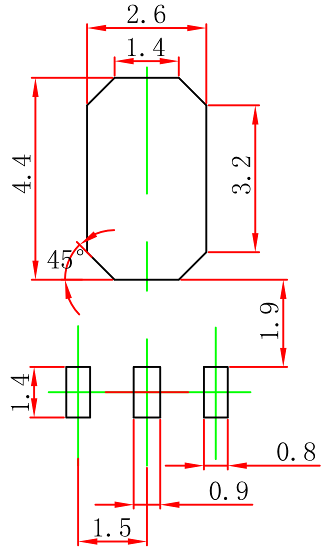


SOT-89-3L Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.400	1.600	0.055	0.063
b	0.320	0.520	0.013	0.197
b1	0.400	0.580	0.016	0.023
c	0.350	0.440	0.014	0.017
D	4.400	4.600	0.173	0.181
D1	1.550 REF		0.061 REF	
E	2.300	2.600	0.091	0.102
E1	3.940	4.250	0.155	0.167
e	1.500 TYP		0.060 TYP	
e1	3.000 TYP		0.118 TYP	
L	0.900	1.200	0.035	0.047

SOT-89-3L Suggested Pad Layout



Note:
1.Controlling dimemsion"in"milimeters.
2.General tolerance: ±0.05mm.
3.The pad layout is for reference purpose only.

DISCLAIMER

IMPORTANT NOTICE, PLEASE READ CAREFULLY

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