

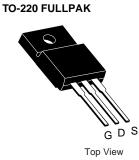
P-Channel 200V (D-S) MOSFET

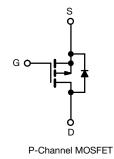
PRODUCT SUMMARY				
V _{DS} (V)	-200			
R _{DS(on)} (Ω)	V _{GS} = -10 V 2.0			
Q _g max. (nC)	29			
Q _{gs} (nC)	5.4			
Q _{gd} (nC)	15			
Configuration	Sing	le		

FEATURES

- Surface mount
- Available in tape and reel
- Dynamic dV/dt rating
- Repetitive avalanche rated
- P-channel
- · Fast switching
- Ease of paralleling







ABSOLUTE MAXIMUM RATINGS (T _C	= 25 °C, unl	ess otherwis	se noted)			
PARAMETER		SYMBOL	LIMIT	UNIT		
Drain-Source Voltage			V _{DS}	-200	V	
Gate-Source Voltage			V _{GS}	± 20	v	
Continuous Drain Current	Vac et 10 V	T _C = 25 °C T _C = 100 °C	- I _D	-3.6		
Continuous Drain Current	VGS at - TO V	T _C = 100 °C		-2.5	A	
Pulsed Drain Current ^a		I _{DM}	-12			
Linear Derating Factor			0.59	14//80		
Linear Derating Factor (PCB mount) ^e			0.025	W/°C		
Single Pulse Avalanche Energy ^b		E _{AS}	500	mJ		
Avalanche Current ^a		I _{AR}	-6.4	А		
Repetitive Avalanche Energy ^a		E _{AR}	7.4	mJ		
Maximum Power Dissipation	$T_{\rm C} = 25 ^{\circ}{\rm C}$ 74		10/			
Maximum Power Dissipation (PCB mount) ^e	$T_A = 2$	25 °C	PD	3.0	vv	
Peak Diode Recovery dV/dt ^c		dV/dt	-5.0	V/ns		
Operating Junction and Storage Temperature Range		T _J , T _{stg} -55 to +150		*0		
Soldering Recommendations (Peak temperature) ^d for 10 s		10 s		300	°C	

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11). b. V_{DD} = -50 V, starting T_J = 25 °C, L = 17 mH, R_g = 25 Ω , I_{AS} = -6.5 A (see fig. 12). c. I_{SD} \leq -6.5 A, dI/dt \leq 120 A/µs, V_{DD} \leq V_{DS}, T_J \leq 150 °C. d. 1.6 mm from case. e. When mounted on 1" square PCB (FR-4 or G-10 material).



THERMAL RESISTANCE RAT	INGS			
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R _{thJA}	-	62	
Maximum Junction-to-Ambient (PCB mount) ^a	R _{thJA}	-	40	°C/W
Maximum Junction-to-Case (Drain)	R _{thJC}	-	1.7	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

PARAMETER	SYMBOL	TES	ST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static		•			•	•	•
Drain-Source Breakdown Voltage	V _{DS}	V _{GS}	= 0, I _D = -250 μA	-200	-	-	V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Referenc	e to 25 °C, I _D = -1 mA	-	-0.24	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} =	: V _{GS} , I _D = -250 μA	-1.5	-	-4.0	V
Gate-Source Leakage	I _{GSS}		$V_{GS} = \pm 20 V$	-	-	± 10	μA
Zava Cata Vialtaga Dirain Current		V _{DS} =	$V_{DS} = -200 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$		-	- 100	μA
Zero Gate Voltage Drain Current	the Voltage Drain Current I_{DSS} $V_{DS} = -160 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ T}_{J} = 125 \text{ °C}$		V, V _{GS} = 0 V, T _J = 125 °C	-	-	-500	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = -10 V	I _D = -1.0 A ^b	-	2.00	-	Ω
Forward Transconductance	9 _{fs}	V _{DS} =	-50 V, I _D = -1.0 A ^b	2.8	-	-	S
Dynamic		-					
Input Capacitance	C _{iss}		V _{GS} = 0 V, V _{DS} = -25 V,		700	-	pF
Output Capacitance	C _{oss}				200	-	
Reverse Transfer Capacitance	C _{rss}	f = 1.0 MHz, see fig. 5		-	40	-	
Total Gate Charge	Qg			-	-	29	
Gate-Source Charge	Q _{gs}	V _{GS} = -10 V	I _D = -3.5A, V _{DS} = -160 V, see fig. 6 and 13 ^b	-	-	5.4	nC
Gate-Drain Charge	Q _{gd}		see lig. o and to	-	-	15	
Turn-On Delay Time	t _{d(on)}		•	-	12	-	
Rise Time	t _r	V_{DD} = -100 V, I_D = -3.5A, R_g = 12 Ω,R_D = 15 $\Omega,$ see fig. 10 $^{\rm b}$		-	27	-	- ns
Turn-Off Delay Time	t _{d(off)}			-	28	-	
Fall Time	t _f			-	24	-	
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from		-	4.5	-	- nH
Internal Source Inductance	L _S	package and die contact	package and center of die contact		7.5	-	
Gate Input Resistance	Rg	f = 1 MHz, open drain		0.6	-	3.7	Ω
Drain-Source Body Diode Characteristic	S						
Continuous Source-Drain Diode Current	I _S	MOSFET sym showing the	MOSFET symbol showing the		-	-3.5	
Pulsed Diode Forward Current ^a	I _{SM}	integral reverse p - n junction diode		-	-	-6	A
Body Diode Voltage	V _{SD}	T _J = 25 °C	, I _S = -3.5A, V _{GS} = 0 V ^b	-	-	-6.5	V
Body Diode Reverse Recovery Time	t _{rr}	T 05 %0 1		-	200	300	ns
Body Diode Reverse Recovery Charge	Q _{rr}	$T_J = 25 \text{ °C}, I_F = -3.5A, dI/dt = 100 \text{ A/}\mu\text{s}^{-b}$		-	1.9	2.9	μC
Forward Turn-On Time	t _{on}	Intrinsic tu	-on is dor	ninated b	y Ls and	L _D)	

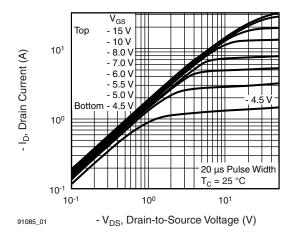
Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width \leq 300 $\mu s;$ duty cycle \leq 2 %.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)





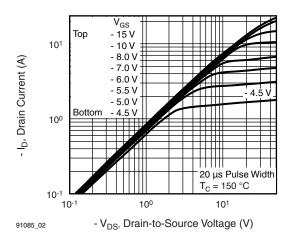


Fig. 2 - Typical Output Characteristics, $T_C = 150 \ ^\circ C$

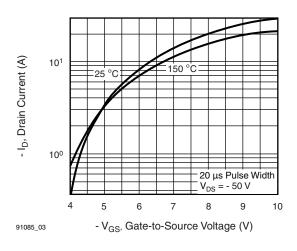


Fig. 3 - Typical Transfer Characteristics

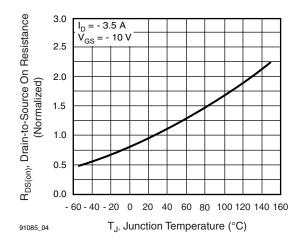


Fig. 4 - Normalized On-Resistance vs. Temperature

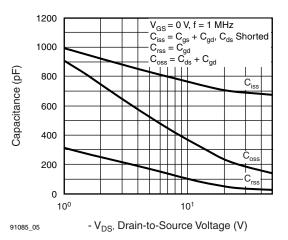


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

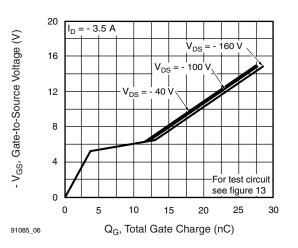


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

VBMB2202K



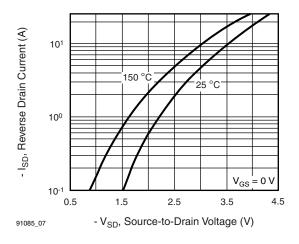


Fig. 7 - Typical Source-Drain Diode Forward Voltage

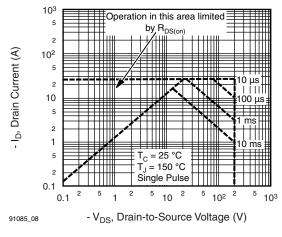


Fig. 8 - Maximum Safe Operating Area

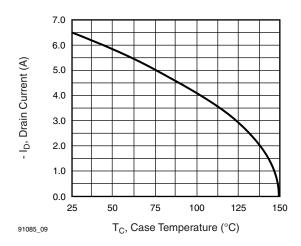


Fig. 9 - Maximum Drain Current vs. Case Temperature

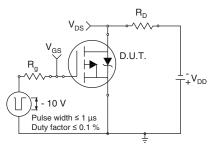


Fig. 10a - Switching Time Test Circuit

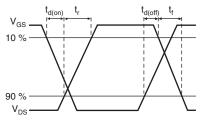
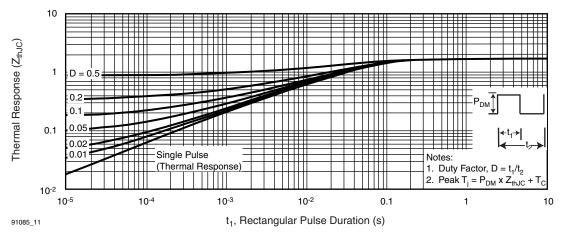


Fig. 10b - Switching Time Waveforms







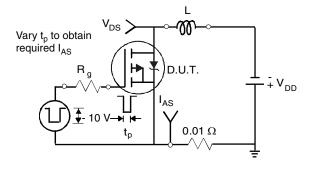


Fig. 12a - Unclamped Inductive Test Circuit

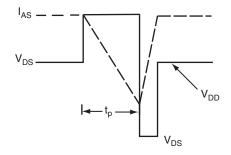


Fig. 12b - Unclamped Inductive Waveforms

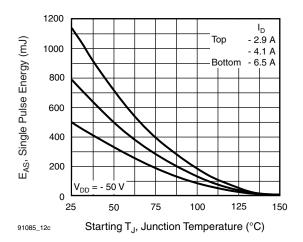


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

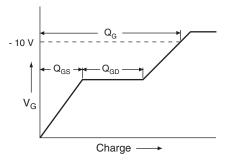


Fig. 13a - Basic Gate Charge Waveform

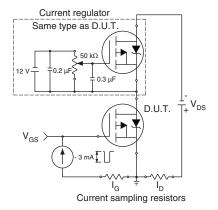
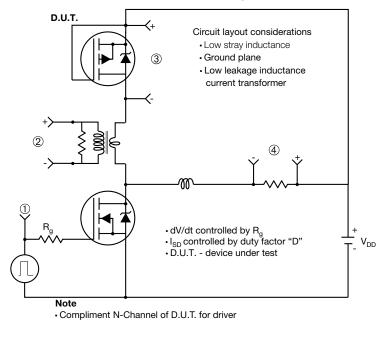
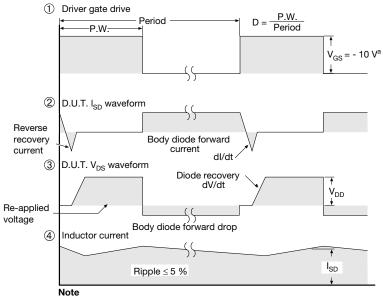


Fig. 13b - Gate Charge Test Circuit



Peak Diode Recovery dV/dt Test Circuit



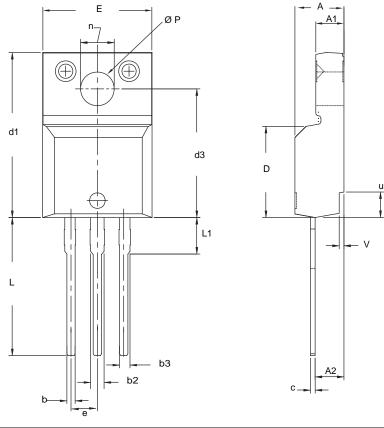


a. V_{GS} = - 5 V for logic level and - 3 V drive devices

Fig. 14 - For P-Channel



TO-220 FULLPAK



	MILLI	METERS	INCHES		
DIM.	MIN.	MAX.	MIN.	MAX.	
А	4.570	4.830	0.180	0.190	
A1	2.570	2.830	0.101	0.111	
A2	2.510	2.850	0.099	0.112	
b	0.622	0.890	0.024	0.035	
b2	1.229	1.400	0.048	0.055	
b3	1.229	1.400	0.048	0.055	
С	0.440	0.629	0.017	0.025	
D	8.650	9.800	0.341	0.386	
d1	15.88	16.120	0.622	0.635	
d3	12.300	12.920	0.484	0.509	
E	10.360	10.630	0.408	0.419	
е	2.54	BSC	0.100	BSC	
L	13.200	13.730	0.520	0.541	
L1	3.100	3.500	0.122	0.138	
n	6.050	6.150	0.238	0.242	
ØP	3.050	3.450	0.120	0.136	
u	2.400	2.500	0.094	0.098	
V	0.400	0.500	0.016	0.020	
N: X09-0126-Rev. B, 2 G: 5972	26-Oct-09				

Notes

1. To be used only for process drawing. 2. These dimensions apply to all TO-220, FULLPAK leadframe versions 3 leads. 3. All critical dimensions should C meet $C_{pk} > 1.33$. 4. All dimensions include burrs and plating thickness. 5. No chipping or package damage.



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