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YT9215S Datasheet

LAYER 2 MANAGED 5+2 PORT 10/100/1000M SWITCH CONTROLLER

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General Description

The YT9215S is a LQFP-128, high-performance 5+2-port 10/100/1000M Ethernet switch featuring a low-power integrated 5-Port Giga-PHY that supports 1000Base-T, 100Base-TX, and 10Base-T.

The integrated Giga-PHY complies with 10BASE-Te, 100BASE-TX, and 1000BASE-T IEEE standard 802.3 and also support Motorcomm proprietary LRE100-4 feature, which makes the device can auto-negotiate and link up with LRE100-4 compliant link partners. LRE100-4 in extended cable length applications up to 400 meter at 100Mbps over CAT5E cable.

For specific applications, the YT9215S supports one extra interface that could be configured as RGMII/MII interfaces. The YT9215S also supports one Ser-Des interface that could be configured as SGMII/HSGMII interfaces. The YT9215S integrates all the functions of a high-speed switch system; including SRAM for packet buffering, non-blocking switch fabric, and internal register management into a single CMOS device. Only a 25MHz crystal is required; an optional EEPROM is offered for internal register configuration.

YT9215S integrates a 4K look-up table with an efficient hashing algorithm for address searching and learning, each of the entries can be configured as a static entry.

The YT9215S supports IEEE 802.1Q VLAN and has a 4K-entry VLAN table. It provides VLAN classification according to port-based, protocol-and-port-based, VLAN translation ,Flow-based capability, and MAC-based, IP-subnet-based VLAN can be supported by configuration It also supports IVL, SVL, and IVL/SVL for flexible network topology architecture.

The Extension GMAC1 of the YT9215S implements a SGMII/HSGMII interfaces and Extension GMAC2 of the YT9215S implements a RGMII/MII interfaces. These interfaces could be connected to an external PHY, MAC, CPU, or RISC for specific applications. In router applications, the YT9215S supports Port VID (PVID) for each port to insert a PVID in the VLAN tag on egress. When using this function, VID information carried in the VLAN tag will be changed to PVID.

Note: The YT9215S Extra Interface (Extension GMAC2) supports:

Media Independent Interface (MII)

Reduced Gigabit Media Independent Interface (RGMII)

The YT9215S supports standard 802.3x flow control frames for full duplex, and optional backpressure for half duplex. It determines when to invoke the flow control mechanism by checking the availability of system resources. The YT9215S supports storm control.

In order to support flexible traffic classification, the YT9215S supports 384-hardware entry ACL rule check and multiple actions options. The 384 entries are composed of 48 rows, each row has 8 entries. To support long rule, rule extension is supported by any combinations of the 8 entries for each row. Each port can optionally enable or disable the ACL rule check function. The ACL rule key can be based on packet physical port, Layer2, Layer3, and Layer4 information. When an ACL rule matches, the action taken is configurable to Drop/Permit/Redirect/Mirror, change priority/DSCP value in 802.1q/Q tag, and rate policing.

Key Features

- High performance, nonblocking, 7 port Ethernet Switch integrating:
  - Five 10/100/1000Mbps PHYs with Advanced Virtual Cable Tester (VCT) diagnostic features,
  - Each PHY supports 10/100/1000M full duplex connectivity (half duplex only supported in 10/100M mode)
  - Full duplex and half duplex operation with IEEE 802.3x flow control and backpressure
- Interface
  - Embedded 5-port 1000/100Base-T/ 10Base-Te PHY
  - Embedded one 2.5Gbps/1Gbps SerDes for 2500Base-X/SGMII/1000Base-X/ 100Base-FX
  - Embedded one RGMII/MII/RMII interface
- Advanced Features
  - Supports parallel LED or serial LED outputs
  - Supports MDIO/IIC Slave interface
  - Supports MDIO/IIC Master interface
  - Supports 1 interrupt output to external CPU for notification
  - Supports 16K-byte EEPROM space for configuration
  - Link On Cable Length Power Saving
  - Supports 9K byte jumbo frames
- Supports 2 IEEE 802.3ad Link aggregation port groups
- Security Filtering
  - Disable learning for each port
  - Disable learning-table aging for each port
  - Unknown DA filter mask
  - Supports Port Isolation
  - Supports Broadcast/Multicast/Unknown DA storm control protects system from attack by hackers
- Control, Management and Statistics
  - Supports RFC MIB Counters
    - MIB-II (RFC 1213)
    - Ethernet-Like MIB (RFC 3635)
    - RMON (RFC 2819)
    - Bridge MIB (RFC 1493)
    - Bridge MIB Extension (RFC 2674)

- Supports OAM and EEE LLDP (Energy Efficient Ethernet Link Layer Discovery Protocol)
- Supports Loop Detection

- Packet Process Engine
  - Supports 802.1Q VLANs
  - Supports 4K VLANs
  - Supports untag definition in each VLAN
  - Supports VLAN policing and VLAN forwarding decision
  - Supports Port based, Tag based, and Protocol based VLAN
  - Supports per port egress VLAN tagging and untagging
  - Supports IEEE 802.1D/s/w Spanning Tree Protocols
  - Support Multicast VLAN (MVR)
  - Supports IVL, SVL, and IVL/SVL
  - Supports IEEE 802.1ad Stacking VLAN
  - Support VLAN translation (1:1/2:1/2:2/ N:1/1:N)
  - Supports IEEE 802.1x Access Control Protocol
    - Port-Based Access Control
    - MAC-Based Access Control
    - Guest VLAN
  - Supports ACL Rules
  - Supports Hardware/Software IGMP/ MLD Snooping
    - Supports Fast Leave
    - Support IGMPV1/V2/V3
    - Static/Dynamic Router port
  - Mirror
    - Port based mirror
    - Flow based mirror
  - Support reserved multicast control
  - Support WOL
- Quality of Service (QoS)
  - Supports Queue based DWRR/SP, packet/byte modes are both supported for DWRR
  - Support min-max queue based shaping, packet/byte modes are both supported
  - Support single token bucket for port based shaping, packet/byte modes are both supported
  - trTCM color aware/blind packet/byte modes
  - Traffic classification based on multiple source type

- Support 8 unicast queues and 4 multicast queues for each port
- Tail drop is supported for UQ/MQ, WRED is supported for UQ

- Microprocessor
  - Integrated RISC-V microprocessor
  - Supports Flash Interface (Dual mode/Single mode)
- 25MHz crystal or 3.3V OSC input
- LQFP 128-pin E-PAD package

Block Diagram

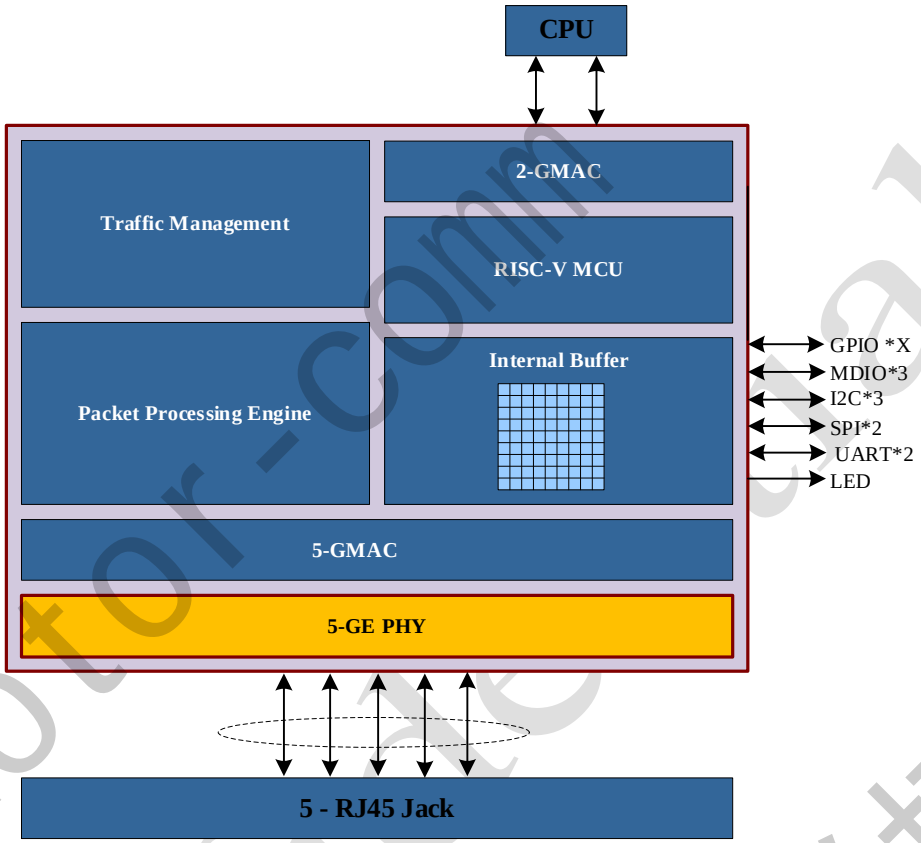

Figure 1. Block Diagram

System Applications

- 5-Port 1000Base-T+1-Port RGMII + 1-Port 2500Base-X Switch
- 5-Port 1000Base-T Router with Single MII/RGMII
- 5-Port 1000Base-T Router with Single SGMII
- 5-Port 1000Base-T NVR
- 5-Port 1000Base-T ONU

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Revision History

Revision	Release Date	Summary
Draft_01	2022/10/31	First version.
Draft_02	2022/11/08	Change Key Features format&add some pin descriptions
Draft_03	2022/11/12	Change DVDDIO&EN_PWRLIGHT description，Optimize pin color distribution
Draft_05	2023/02/10	Chang power pin color&MII pin name

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1.1. Pin Assignment

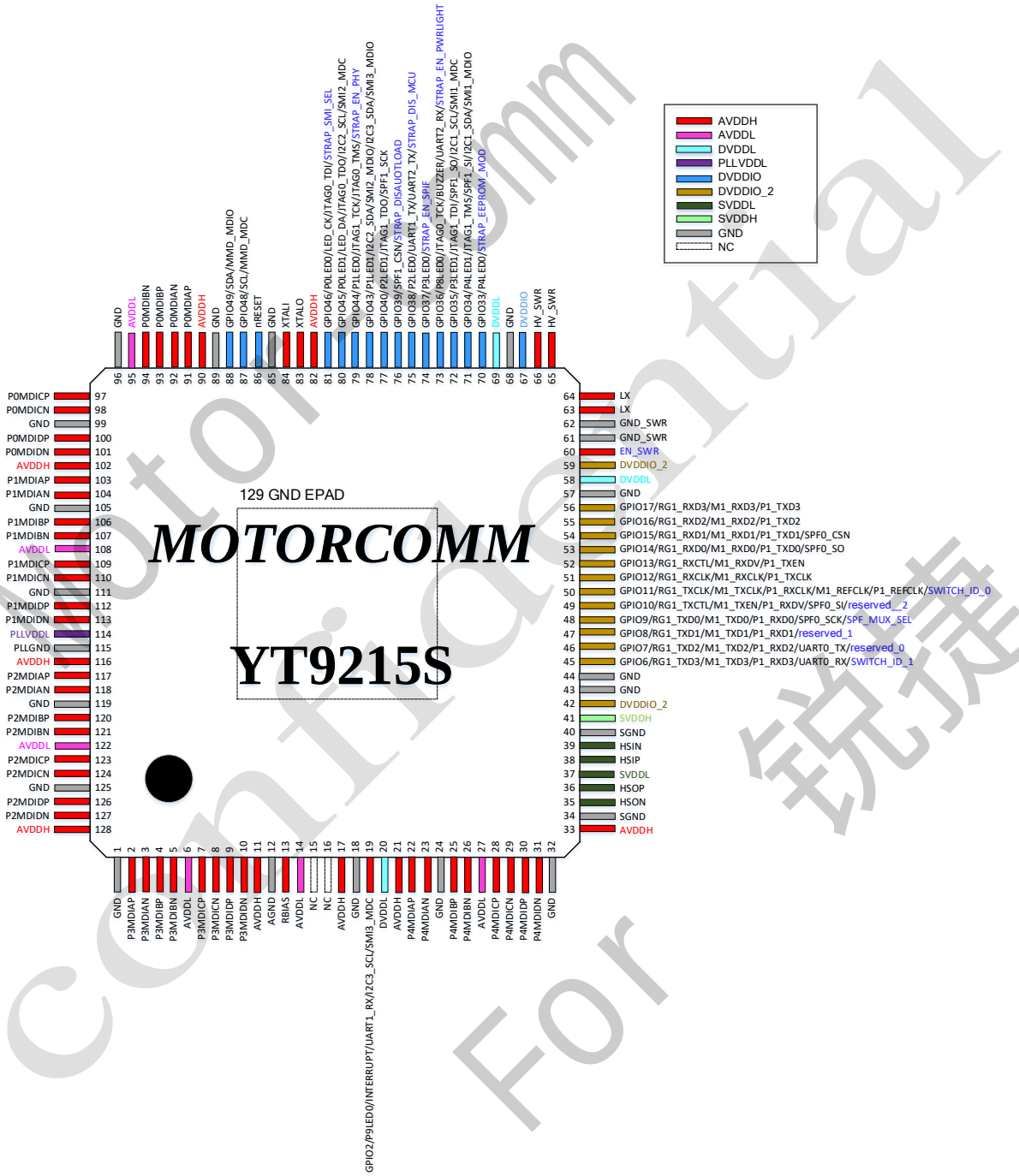


Figure 2. Pin Assignment

1.2. Pin Assignment Table

Some pins have multiple functions.

Refer to the Pin Assignment figures for a graphical representation.

- I: Input
- O: Output
- IO: Bidirectional Input and Output
- P: Digital Power Pin
- G: Digital Ground pin
- PU: Internal pull up
- LI: Latched Input During Power UP
- OD: Open Drain
- AI: Analog Input
- AO: Analog Output
- AIO: Analog Bidirectional Input and Output
- AP: Analog Power pin
- AG: Analog Ground pin
- PD: Internal pull down
- XT: Crystal Related

Table 1. Pin Assignment

No.	Pin Name	Type
1	GND	G
2	P3MDIAP	AIO
3	P3MDIAN	AIO
4	P3MDIBP	AIO
5	P3MDIBN	AIO
6	AVDDL	AP
7	P3MDICP	AIO
8	P3MDICN	AIO
9	P3MDIDP	AIO
10	P3MDIDN	AIO
11	AVDDH	AP
12	AGND	AG
13	MDIREF	AO
14	AVDDL	AP

No.	Pin Name	Type
15	NC	-
16	NC	-
17	AVDDH	AP
18	GND	G
19	GPIO2/P9LED0/INTERRUPT/UART1_RX/I2C3_SCL/SMI3_MDC	IO/PU/OD
20	DVDDL	P
21	AVDDH	AP
22	P4MDIAP	AIO
23	P4MDIAN	AIO
24	GND	G
25	P4MDIBP	AIO
26	P4MDIBN	AIO
27	AVDDL	AP

No.	Pin Name	Type
28	P4MDICP	AIO
29	P4MDICN	AIO
30	P4MDIDP	AIO
31	P4MDIDN	AIO
32	GND	G
33	AVDDH	AP
34	SGND	AG
35	HSON	AO
36	HSOP	AO
37	SVDDL	AP
38	HSIP	AI
39	HSIN	AI
40	SGND	AG
41	SVDDH	AP
42	DVDDIO_2	P
43	GND	G
44	GND	G
45	GPIO6/RG1_TXD3/M1_TXD3/P1_RXD3/UART0_RX/SWITCH_ID_1	IO/LI/PD/OD
46	GPIO7/RG1_TXD2/M1_TXD2/P1_RXD2/UART0_TX/reserved_0	IO/LI/PU/OD
47	GPIO8/RG1_TXD1/M1_TXD1/P1_RXD1/reserved_1	IO/LI/PU/OD
48	GPIO9/RG1_TXD0/M1_TXD0/P1_RXD0/SPF0_SCK/SPF_MUX_SEL	IO/LI/PD/OD
49	GPIO10/RG1_TXCTL/M1_TXEN/P1_RXDV/SPF0_SI/reserved_2	IO/PD/OD
50	GPIO11/RG1_TXCLK/M1_TXCLK/P1_RXCLK/M1_REFCLK/P1_REFCLK/SWITCH_ID_0	IO/LI/PD/OD
51	GPIO12/RG1_RXCLK/M1_RXCLK/P1_TXCLK	IO/PU
52	GPIO13/RG1_RXCTL/M1_RXDV/P1__TXEN	IO/PU
53	GPIO14/RG1_RXD0/M1_RXD0/P1_TXD0/SPF0_SO	IO/PU
54	GPIO15/RG1_RXD1/M1_RXD1/P1_TXD1/SPF0_CSN	IO/PU
55	GPIO16/RG1_RXD2/M1_RXD2/P1_TXD2	IO/PU
56	GPIO17/RG1_RXD3/M1_RXD3/P1_TXD3	IO/PU
57	GND	G
58	DVDDL	P
59	DVDDIO_2	P
60	EN_SWR	AI
61	GND_SWR	AG
62	GND_SWR	AG
63	LX	AO
64	LX	AO
65	HV_SWR	AP
66	HV_SWR	AP
67	DVDDIO	P
68	GND	G
69	DVDDL	P
70	GPIO33/P4LED0/STRAP_EEPROM_MOD	IO/LI/PU

No.	Pin Name	Type
71	GPIO34/P4LED1/JTAG1_TMS/SPF1_SI/I2C1_SDA/SMI1_MDIO	IO/PU/OD
72	GPIO35/P3LED1/JTAG1_TDI/SPF1_SO/I2C1_SCL/SMI1_MDC	IO/PU/OD
73	GPIO36/P8LED0/JTAG0_TCK/BUZZER/UART2_RX/STRAP_EN_PWRLIGHT	IO/LI/PU
74	GPIO37/P3LED0/STRAP_EN_SPIF	IO/LI/PU
75	GPIO38/P2LED0/UART1_TX/UART2_TX/STRAP_DIS_MCU	IO/LI/PU
76	GPIO39/SPF1_CSN/STRAP_DISAUOTLOAD	IO/LI/PU
77	GPIO40/P2LED1/JTAG1_TDO/SPF1_SCK	IO/PU
78	GPIO43/P1LED1/I2C2_SDA/SMI2_MDIO/I2C3_SDA/SMI3_MDIO	IO/PU/OD
79	GPIO44/P1LED0/JTAG1_TCK/JTAG0_TMS/STRAP_EN_PHY	IO/LI/PU
80	GPIO45/P0LED1/LED_DA/JTAG0_TDO/I2C2_SCL/SMI2_MDC	IO/LI/PU/OD
81	GPIO46/P0LED0/LED_CK/JTAG0_TDI/STRAP_SMI_SEL	IO/LI/PU
82	AVDDH	AP
83	XTALO	XT
84	XTALI	XT
85	GND	G
86	nRESET	AI/PU

No.	Pin Name	Type
87	GPIO48/SCL/MMD_MDC	IO/PU/OD
88	GPIO49/SDA/MMD_MDIO	IO/PU/OD
89	GND	G
90	AVDDH	AP
91	P0MDIAP	AIO
92	P0MDIAN	AIO
93	P0MDIBP	AIO
94	P0MDIBN	AIO
95	AVDDL	AP
96	GND	G
97	P0MDICP	AIO
98	P0MDICN	AIO
99	GND	G
100	P0MDIDP	AIO
101	P0MDIDN	AIO
102	AVDDH	AP
103	P1MDIAP	AIO
104	P1MDIAN	AIO
105	GND	G
106	P1MDIBP	AIO
107	P1MDIBN	AIO
108	AVDDL	AP
109	P1MDICP	AIO
110	P1MDICN	AIO
111	GND	G
112	P1MDIDP	AIO
113	P1MDIDN	AIO
114	PLLVDDL	AP
115	PLLGND	AG
116	AVDDH	AP

No.	Pin Name	Type
117	P2MDIAP	AIO
118	P2MDIAN	AIO
119	GND	G
120	P2MDIBP	AIO
121	P2MDIBN	AIO
122	AVDDL	AP

No.	Pin Name	Type
123	P2MDICP	AIO
124	P2MDICN	AIO
125	GND	G
126	P2MDIDP	AIO
127	P2MDIDN	AIO
128	AVDDH	AP

2. Pin Description

2.1. MDI Interface Pins

Table 2. Transceiver Interface

No.	Pin Name	Type	Description
91	P0MDIAP	AIO	Port 0 Media-dependent interface, differential pairs A, with 100Ω termination resistor.
92	P0MDIAN	AIO	
93	P0MDIBP	AIO	Port 0 Media-dependent interface, differential pairs B, with 100Ω termination resistor.
94	P0MDIBN	AIO	
97	P0MDICP	AIO	Port 0 Media-dependent interface, differential pairs C, with 100Ω termination resistor.
98	P0MDICN	AIO	
100	P0MDIDP	AIO	Port 0 Media-dependent interface, differential pairs D, with 100Ω termination resistor.
101	P0MDIDN	AIO	
103	P1MDIAP	AIO	Port 1 Media-dependent interface, differential pairs A, with 100Ω termination resistor.
104	P1MDIAN	AIO	
106	P1MDIBP	AIO	Port 1 Media-dependent interface, differential pairs B, with 100Ω termination resistor.
107	P1MDIBN	AIO	
109	P1MDICP	AIO	Port 1 Media-dependent interface, differential pairs C, with 100Ω termination resistor.
110	P1MDICN	AIO	
112	P1MDIDP	AIO	Port 1 Media-dependent interface, differential pairs D, with 100Ω termination resistor.
113	P1MDIDN	AIO	
117	P2MDIAP	AIO	Port 2 Media-dependent interface, differential pairs A, with 100Ω termination resistor.
118	P2MDIAN	AIO	
120	P2MDIBP	AIO	Port 2 Media-dependent interface, differential pairs B, with 100Ω termination resistor.
121	P2MDIBN	AIO	
123	P2MDICP	AIO	Port 2 Media-dependent interface, differential pairs C, with 100Ω termination resistor.
124	P2MDICN	AIO	
126	P2MDIDP	AIO	Port 2 Media-dependent interface, differential pairs D, with 100Ω termination resistor.
127	P2MDIDN	AIO	
2	P3MDIAP	AIO	Port 3 Media-dependent interface, differential pairs A, with 100Ω termination resistor.
3	P3MDIAN	AIO	
4	P3MDIBP	AIO	

5	P3MDIBN	AIO	Port 3 Media-dependent interface, differential pairs B, with 100Ω termination resistor.
7	P3MDICP	AIO	Port 3 Media-dependent interface, differential pairs C, with 100Ω termination resistor.
8	P3MDICN	AIO	
9	P3MDIDP	AIO	Port 3 Media-dependent interface, differential pairs D, with 100Ω termination resistor.
10	P3MDIDN	AIO	
22	P4MDIAP	AIO	Port 4 Media-dependent interface, differential pairs A, with 100Ω termination resistor.
23	P4MDIAN	AIO	
25	P4MDIBP	AIO	Port 4 Media-dependent interface, differential pairs B, with 100Ω termination resistor.
26	P4MDIBN	AIO	
28	P4MDICP	AIO	Port 4 Media-dependent interface, differential pairs C, with 100Ω termination resistor.
29	P4MDICN	AIO	
30	P4MDIDP	AIO	Port 4 Media-dependent interface, differential pairs D, with 100Ω termination resistor.
31	P4MDIDN	AIO	

2.2. RGMII Interface Pins

Table 3. RGMII

No.	Pin Name	Type	Description
50	RG1_TXCLK	IO/LI/PD/OD	RGMII 2 transmit reference clock will be 125Mhz, 25MHz, or 2.5MHz depending on speed.
49	RG1_TXCTL	IO/LI/PD/OD	RGMII 2 Transmit Control Signal from the MAC.
45	RG1_TXD3	IO/LI/PD/OD	RGMII 2 transmit Data. Data is transmitted from MAC to PHY via TXD[3:0].
46	RG1_TXD2	IO/LI/PU/OD	
47	RG1_TXD1	IO/LI/PU/OD	
48	RG1_TXD0	IO/PD/OD	
51	RG1_RXCLK	IO/PU	RGMII 2 receive Control Signal to the MAC.

52	RG1_RXCTL	IO/PU	RGMII 2 continuous receive reference clock will be 125MHz, 25MHz, or 2.5MHz, and is derived from the received data stream.
56	RG1_RXD3	IO/PU	RGMII 2 receive Data. Data is transmitted from PHY to MAC via RXD[3:0].
55	RG1_RXD2	IO/PU	
54	RG1_RXD1	IO/PU	
53	RG1_RXD0	IO/PU	

2.3. MII Interface Pins

Table 4. MII Interface Pins

No.	Pin Name	Type	Description
50	M1_TXCLK/ P1_RXCLK	IO/LI/PD/OD	1. M_TXC Pin in MII MAC Mode. MII Transmit Clock (input). Used to synchronize M_TXD[3:0], and M_TXEN. 2. P_RXC Pin in MII PHY Mode. MII Receive Clock (output). Used to synchronize P_RXD[3:0], and P_RXDV. The frequency depends on the link speed, that is 25MHz at 100Base-TX , and 2.5MHz at 10Base-Te.
49	M1_TXEN/ P1_RXDV	IO/LI/PD/OD	1. M_TXEN Pin in MII MAC Mode. MII Transmit Enable. The synchronous output indicates that valid data is being driven on the M_TXD bus. M_TXEN is synchronous to M_TXC. 2. P_RXDV Pin in MII PHY Mode. MII Receive Data Valid. This synchronous output is asserted when valid data is driven on the P_RXD bus. P_RXDV is synchronous to P_RXC.
45	M1_TXD3/ P1_RXD3	IO/LI/PD/OD	1. M_TXD[3:0] Pin in MII MAC Mode. MII Transmit Data Bus. M_TXD[3:0] is synchronous to M_TXC. 2. P_RXD[3:0] Pin in MII PHY Mode. MII Receive Data Bus. P_RXD[3:0] is synchronous to P_RXC.
46	M1_TXD2/ P1_RXD2	IO/LI/PU/OD	
47	M1_TXD1/ P1_RXD1	IO/LI/PU/OD	

48	M1_TXD0/ P1_RXD0	IO/LI/PD/OD	
51	M1_RXCLK/ P1_TXCLK	IO/PU	1. M_RXC Pin in MII 1 MAC Mode. MII Receive Clock(input). Used to synchronize M_RXD[3:0], and M_RXDV. 2. P_TXC Pin in MII PHY Mode. MII Transmit Clock (output). Used to synchronize P_TXD[3:0], and P_TXEN. The frequency depends on the link speed, that is 25MHz at 100Base-TX , and 2.5MHz at 10Base-Te.
52	M1_RXDV/ P2_TXEN	IO/PU	1. M_RXDV Pin in MII MAC Mode. MII Receive Data Valid. This synchronous input is asserted when valid data is driven on M_RXD bus. M_RXDV is synchronous to M_RXC. 2. P_TXEN Pin in MII PHY Mode. MII Transmit Enable. The synchronous input indicates that valid data is being driven on the P_TXD bus. P_TXEN is synchronous to P_TXC.
56	M1_RXD3/ P1_TXD3	IO/PU	1. M_RXD[3:0] Pin in MII MAC Mode. MII Receive Data Bus. M_RXD[3:0] is synchronous to M_RXC. 2. P_TXD[3:0] Pin in MII 1 PHY Mode. MII Transmit Data Bus. P_TXD[3:0] is synchronous to P_TXC .
55	M1_RXD2/ P1_TXD2	IO/PU	
54	M1_RXD1/ P1_TXD1	IO/PU	
53	M1_RXD0/ P1_TXD0	IO/PU	

2.4. RMII Interface Pins

Table 5. RMII Interface Pins

No.	Pin Name	Type	Description
50	M1_REFCLK/ P1_REFCLK	IO/LI/PD/OD	REFCLK pin in RMII Mode. 1. In RMII MAC Mode, REFCLK is an input pin. 2. In RMII PHY Mode, REFCLK is a output pin.

			REF_CLK is a 50Mhz clock that provides the timing reference for CRSDV, RXD[1:0], TXEN, TXD[1:0].
49	M1_TXEN/ P1_RXDV	IO/LI/PD/ OD	1. TXEN Pin in RMII MAC Mode. The synchronous output indicates that valid data is being driven on the TXD bus. TXEN is synchronous to REFCLK. 2. CRSDV Pin in RMII PHY Mode. Carrier Sense/Receive Data Valid. This shall be asserted by the PHY when the receive medium is non-idle synchronized with REFCLK.
47	M1_TXD1/ P1_RXD1	IO/LI/PU/ OD	1. TXD[1:0] Pin in RMII MAC Mode, synchronous to REFCLK. 2. RXD[1:0] Pin in RMII PHY Mode, synchronous to REFCLK.
48	M1_TXD0/ P1_RXD0	IO/PD/OD	
52	M1_RXDV/ P1_TXEN	IO/PU	1. TXEN Pin in RMII MAC Mode. The synchronous output indicates that valid data is being driven on the TXD bus. TXEN is synchronous to REFCLK. 2. CRSDV Pin in RMII PHY Mode. Carrier Sense/Receive Data Valid. This shall be asserted by the PHY when the receive medium is non-idle synchronized with REFCLK.
54	M1_RXD1/ P1_TXD1	IO/PU	1. RXD[1:0] Pin in RMII MAC Mode, is synchronous to REFCLK. 2. TXD[1:0] Pin in RMII PHY Mode, is synchronous to REFCLK .
53	M1_RXD0/ P1_TXD0	IO/PU	

2.5. High-Speed Serial Interface Pins

Table 6. High-Speed Serial Interface Pins

No.	Pin Name	Type	Description
35	HSON	AO	High-Speed Serial Interface Pins: support 3.125GHz or 1.25GHz. Differential serial output interface.
36	HSOP	AO	
38	HSIP	AI	High-Speed Serial Interface Pins: support 3.125GHz or 1.25GHz. Differential serial input interface.
39	HSIN	AI	

2.6. Parallel LED Pins

Table 7. Parallel LED Pins

No.	Pin Name	Type	Description
19	P9LED0	IO/PU/OD	Default port 9 Parallel LED LED0 Output Signal. The LED indicates information is defined by register or EEPROM
73	P8LED0	IO/LI/PU	Default port 8 Parallel LED LED0 Output Signal. The LED indicates information is defined by register or EEPROM
71	P4LED1	IO/PU/OD	Default port 4 Parallel LED LED1 Output Signal. The LED indicates information is defined by register or EEPROM
70	P4LED0	IO/LI/PU	Default port 4 Parallel LED LED0 Output Signal. The LED indicates information is defined by register or EEPROM
72	P3LED1	IO/PU/OD	Default port 3 Parallel LED LED1 Output Signal. The LED indicates information is defined by register or EEPROM
74	P3LED0	IO/LI/PU	Default port 3 Parallel LED LED0 Output Signal. The LED indicates information is defined by register or EEPROM
77	P2LED1	IO/PU	Default port 2 Parallel LED LED1 Output Signal. The LED indicates information is defined by register or EEPROM
75	P2LED0	IO/LI/PU	Default port 2 Parallel LED LED0 Output Signal. The LED indicates information is defined by register or EEPROM
78	P1LED1	IO/PU/OD	Default port 1 Parallel LED LED1 Output Signal. The LED indicates information is defined by register or EEPROM
79	P1LED0	IO/LI/PU	Default port 1 Parallel LED LED0 Output Signal. The LED indicates information is defined by register or EEPROM

80	P0LED1	IO/PU/OD	Default port 0 Parallel LED LED1 Output Signal. The LED indicates information is defined by register or EEPROM
81	P0LED0	IO/LI/PU	Default port 0 Parallel LED LED0 Output Signal. The LED indicates information is defined by register or EEPROM

2.7. Serial LED Pins

Table 8. Serial LED Pins

No.	Pin Name	Type	Description
81	LED_CK	IO/LI/PU	Serial Mode LED Clock Signal.
80	LED_DA	IO/PU/OD	Serial Mode LED Data Signal.

2.8. SPI FLASH Pins

Table 9. SPI FLASH Interface Pins

No.	Pin Name	Type	Description
54	SPF0_CSN	IO/PU	SPI FLASH chip select signal.
76	SPF1_CSN	IO/LI/PU	
49	SPF0_SI	IO/PD/OD	In Serial I/O Mode SPI Serial FLASH Serial Data Input (YT9215S output pin) In Dual I/O Mode SPI FLASH bi-directional pin (this is LSB)
71	SPF1_SI	IO/LI/PD/OD	
53	SPF0_SO	IO/PU	In Serial I/O Mode, SPI Serial FLASH Serial Data Output (YT9215S input pin) In Dual I/O Mode, SPI FLASH bi-directional pin (this is MSB)
72	SPF1_SO	IO/PU/OD	
48	SPF0_SCK	IO/LI/PD/OD	SPI FLASH Clock.
77	SPF1_SCK	IO/PU	

2.9. JTAG Interface Pins

Table 10. JTAG Interface Pins

No.	Pin Name	Type	Description
77	JTAG1_TDO	IO/PU	Test Data Out.
72	JTAG1_TDI	IO/PU/OD	Test Data In.
71	JTAG1_TMS	IO/PU/OD	Test Mode Select.
79	JTAG1_TCK	IO/LI/PU	Test Clock.
80	JTAG0_TDO	IO/PU/OD	Test Data Out.
81	JTAG0_TDI	IO/LI/PU	Test Data In.
79	JTAG0_TMS	IO/PU/OD	Test Mode Select.
73	JTAG0_TCK	IO/LI/PU/OD	Test Clock.

2.10. UART Interface Pins

Table 11. UART Interface Pins

No.	Pin Name	Type	Description
45	UART0_RX	IO/LI/PU/OD	UART RX pin.
46	UART0_TX	IO/LI/PU/OD	UART TX pin.
19	UART1_RX	IO/PU/OD	UART RX pin.
75	UART1_TX	IO/LI/PU	UART TX pin.
73	UART2_RX	IO/LI/PU	UART RX pin.
75	UART2_TX	IO/LI/PU	UART TX pin.

2.11. Master I2C and MDIO Interface Pins

Table 12. Master I2C and MDIO Interface Pins

No.	Pin Name	Type	Description
72	I2C1_SCL/ SMI1_MDC	IO/PU/OD	SCL pin in Group1 Master I2C. MDC pin in Group1 Master SMI.

71	I2C1_SDA/ SMI1_MDIO	IO/PU/OD	SDA pin in Group1 Master I2C. MDIO pin in Group1 Master SMI.
80	I2C2_SCL/ SMI2_MDC	IO/PU/OD	SCL pin in Group2 Master I2C. MDC pin in Group2 Master SMI.
19	I2C3_SCL/ SMI3_MDC	IO/PU/OD	SCL pin in Group3 Master I2C. MDC pin in Group3 Master SMI.
78	I2C2_SDA/ I2C3_SDA/ SMI2_MDIO/ SMI3_MDIO	IO/PU/OD	SDA pin in Group2/3 Master I2C. MDIO pin in Group2/3 Master SMI.

2.12. Management Interface Pins

Table 13. Management Interface Pins

No.	Pin Name	Type	Description
87	SCL/ MMD_MDC	IO/PU/OD	EEPROM auto load mode serial clock output I2C slave mode serial clock input MDC/MDIO slave mode serial clock input
88	SDA/ MMD_MDIO	IO/PU/OD	EEPROM auto load mode serial data input I2C slave mode serial data MDC/MDIO slave mode serial data

2.13. GPIO Pins

Table 14. GPIO Pins

No.	Pin Name	Type	Description
19	GPIO2	IO/PD/OD	General Purpose Input/Output Interfaces IO2.
45	GPIO6	IO/LI/PD/OD	General Purpose Input/Output Interfaces IO6.
46	GPIO7	IO/LI/PU/OD	General Purpose Input/Output Interfaces IO7.
47	GPIO8	IO/LI/PU/OD	General Purpose Input/Output Interfaces IO8.

48	GPIO9	IO/LI/PD/OD	General Purpose Input/Output Interfaces IO9.
49	GPIO10	IO/LI/PD/OD	General Purpose Input/Output Interfaces IO10.
50	GPIO11	IO/LI/PD/OD	General Purpose Input/Output Interfaces IO11.
51	GPIO12	IO/PU	General Purpose Input/Output Interfaces IO12.
52	GPIO13	IO/PU	General Purpose Input/Output Interfaces IO13
53	GPIO14	IO/PU	General Purpose Input/Output Interfaces IO14.
54	GPIO15	IO/PU	General Purpose Input/Output Interfaces IO15.
55	GPIO16	IO/PU	General Purpose Input/Output Interfaces IO16.
56	GPIO17	IO/PU	General Purpose Input/Output Interfaces IO17.
70	GPIO33	IO/PU	General Purpose Input/Output Interfaces IO33.
71	GPIO34	IO/PU/OD	General Purpose Input/Output Interfaces IO34.
72	GPIO35	IO/PU/OD	General Purpose Input/Output Interfaces IO35.
73	GPIO36	IO/LI/PU	General Purpose Input/Output Interfaces IO36.
74	GPIO37	IO/LI/PU	General Purpose Input/Output Interfaces IO37.
75	GPIO38	IO/LI/PU	General Purpose Input/Output Interfaces IO38.
76	GPIO39	IO/LI/PU	General Purpose Input/Output Interfaces IO39.
77	GPIO40	IO/LI/PU	General Purpose Input/Output Interfaces IO40.
78	GPIO43	IO/PU/OD	General Purpose Input/Output Interfaces IO43.
79	GPIO44	IO/LI/PU	General Purpose Input/Output Interfaces IO44.
80	GPIO45	IO/PU/OD	General Purpose Input/Output Interfaces IO45.
81	GPIO46	IO/LI/PU	General Purpose Input/Output Interfaces IO46.
87	GPIO48	IO/PU/OD	General Purpose Input/Output Interfaces IO48.
88	GPIO49	IO/PU/OD	General Purpose Input/Output Interfaces IO49.

2.14. Configuration Pins

Table 15. Configuration Pins

No.	Pin Name	Type	Description
45	SWITCH_ID_1	IO/LI/PD/OD	Switch_ID[1:0] for slave MDC/MDIO format.

50	SWITCH_ID_0	IO/LI/PD/OD	
48	SPF_MUX_SEL	IO/PD/OD	SPI FLASH Interface Position Select. Pull Up: Select Spi-Flash-0 pin 54\53\49\48. Pull Down: Select Spi-Flash-1 pin 77\76\72\71.
60	EN_SWR	AI	Enable Internal Switching Regulator. Pull Up: Enable Internal Switching Regulator Pull Down: Disable Internal Switching Regulator Note: This pin must be pulled high or low via an external 1k ohm resistor when normal operation.
70	STRAP_EEPROM_MOD	IO/LI/PU	EEPROM Mode Selection. Pull Up: EEPROM 24Cxx Size greater than 16Kbits (24C32~) Pull Down: EEPROM 24Cxx Size less than or equal to 16Kbit (24C02~24C16).
73	STRAP_EN_PWRLIGHT	IO/LI/PU	Disable/Enable LED function When Powered On. Pull Up: Enable LED Pull Down: Disable LED.
74	STRAP_EN_SPIF	IO/LI/PU	Enable SPI FLASH Interface. Pull Up: Enable FLASH interface Pull Down: Disable FLASH interface
75	STRAP_DIS_MCU	IO/LI/PU	Disable Embedded MCU. Pull Up: Disable embedded MCU upon power on or reset Pull Down: Enable embedded MCU upon power on or reset
76	STRAP_DISAUTOLOAD	IO/LI/PU	Disable EEPROM Autoload. Pull Up: Disable EEPROM autoload upon power on or reset Pull Down: Enable EEPROM autoload upon power on or reset
79	STRAP_EN_PHY	IO/LI/PU	Enable Embedded PHY. Pull Up: Enable embedded PHY Pull Down: Disable embedded PHY
81	STRAP_SMI_SEL	IO/LI/PU	EEPROM SMI/MII Management Interface Selection. Pull Up: EEPROM SMI interface when DIS_SPIS = 1

			Pull Down: MII Management interface when DIS_SPIS = 1

2.15. Power Related Pins

Table 16. Power Related Pins

No.	Pin Name	Type	Description
67	DVDDIO	P	Digital power 2.5V/3.3V Note: When DVDDIO uses 2.5V, its external interface must also support the corresponding voltage.
42, 59	DVDDIO_2	P	Digital power 1.8V/2.5V/3.3V for Extension Port 1 Note: When DVDDIO_2 uses 1.8V/2.5V,its external interface must also support the corresponding voltage.
20, 58, 69	DVDDL	P	Digital power 1.1V
11, 17, 21, 33, 82, 90, 102, 116, 128	AVDDH	AP	Analog power 3.3V
65,66	HV_SWR	AP	Internal Switching Regulator Power, Connect to a bulk capacitor 10uF to GND.
6, 14, 27, 95, 108, 122	AVDDL	AP	Analog power 1.1V
41	SVDDH	AP	SerDes power 3.3V
37	SVDDL	AP	SerDes power 1.1V
114	PLLVDDL	AP	PLL Power 1.1V
63,64	LX	AO	Analog power output 1.1V
13	RBIAS	AO	Bias Resistor. An external 2.49 kΩ±1% resistor must be connected between the RBIAS pin and GND
12	AGND	AG	Analog GND
34, 40	SGND	AG	SerDes GND
115	PLLGND	AG	PLL GND

2.16. Clock Pins

Table 17. Clock Pins

No.	Pin Name	Type	Description
84	XTAL_I	XT	25MHz Crystal Input pin. If use external oscillator or clock from another device. 1. When connect an external 25Hhz oscillator or clock from another device to XTAL_O pin, XTAL_I must be shorted to GND. 2. When connect an external 25Hhz oscillator or clock from another device to XTAL_I pin, keep the XTAL_O floating.
83	XTAL_O	XT	25Mhz Crystal Output pin. If use external oscillator or clock from another device. 1. When connect an external 25Hhz oscillator or clock from another device to XTAL_O pin, XTAL_I must be shorted to GND. 2. When connect an external 25Hhz oscillator or clock from another device to XTAL_I pin, keep the XTAL_O floating.

2.17. Reset Pins

Table 18. Reset Pins

No.	Pin Name	Type	Description
86	nRESET	AI/PU	Hardware reset, active low. Requires an external pull-up resistor

2.18. Miscellaneous Pins

Table 19. Miscellaneous Pin

No.	Pin Name	Type	Description

15, 16	NC	-	Not connect. Must be left floating in normal operation.
46	reserved_0	-	Reserved. This pin must be pulled high via an external 4.7kohm resistor to DVDDIO upon power on.
47	reserved_1	-	Reserved. This pin must be pulled high via an external 4.7kohm resistor to DVDDIO upon power on.
49	reserved_2	-	Reserved. This pin must be pulled high via an external 4.7kohm resistor to DVDDIO upon power on.

3. Power Requirements

3.1. Absolute Maximum Ratings

Table 20. Absolute Maximum Ratings

Parameter	Min	Max	Units
Junction Temperature (T_j)	-	+125	℃
Storage Temperature	-45	+125	℃
DVDDIO, DVDDIO_2,AVDDH, SVDDH, Supply Referenced to GND and AGND	GND-0.3	+3.70	V
DVDDL, AVDDL, PLLVDDL, SVDDL , Supply Referenced to GND, AGND and PLLGND	GND-0.3	+1.40	V
Digital Input Voltage	GND-0.3	VDDIO+0.3	V

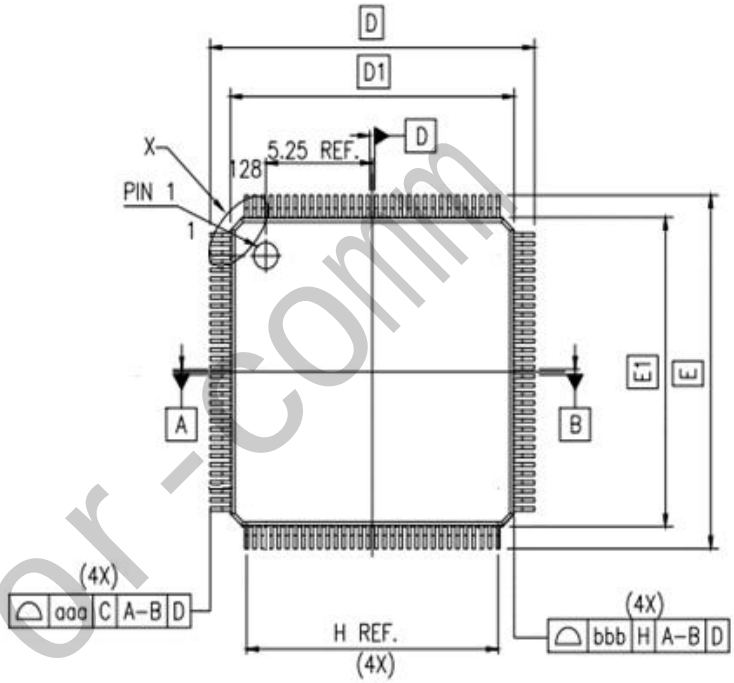
3.2. Recommended Operating Range

Table 21. Recommended Operating Range

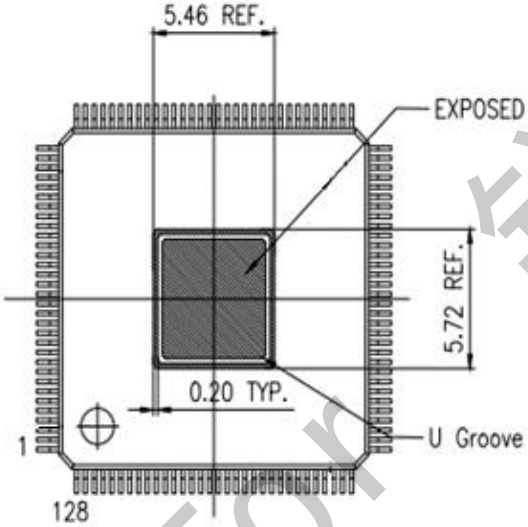
Parameter		Min	TYP	Max	Units
Ambient Operating Temperature (T_a)		0	-	70	℃
DVDDIO, AVDDH, SVDDH Supply Voltage Range		3.135	3.3	3.63	V
DVDDIO_2 Supply Voltage Range (DVDDIO_2: Extension Port 2 Supports 1.8V, 2.5V, 3.3V)	3.3V	3.135	3.3	3.63	V
	2.5V	2.25	2.5	2.75	V
	1.8V	1.620	1.8	1.98	V
DVDDL, AVDDL, PLLVDDL, SVDDL, Supply Voltage Range		1.045	1.1	1.32	V

4. Mechanical Information

Top View



Bottom View



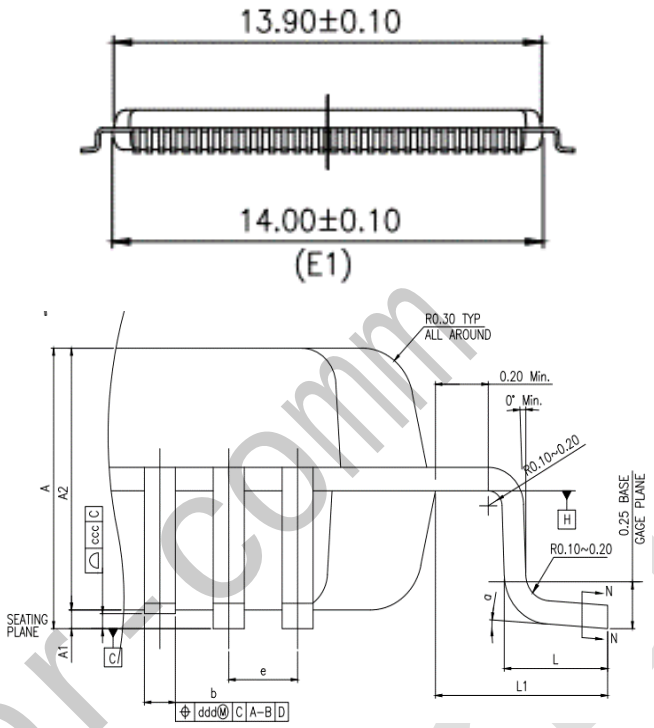


Table 22. Mechanical Dimensions in mm

	SYMBOL	MIN	NOM	MAX
OVERALL HEIGHT	A	-	-	1.6
STANDOFF	A1	-	-	0.127
PKG THICKNESS	A2	1.35	1.4	1.45
LEAD WIDTH	b	0.13	0.18	0.23
LEAD TIP TO TIP	D	15.85	16	16.15
LEAD TIP TO TIP	E	15.85	16	16.15
PKG LENGTH	D1	13.9	14	14.1
PKG WIDTH	E1	13.9	14	14.1
	E-PAD	5.72 REF x5.46 REF.		
LEAD PITCH	e	0.4BSC		
FOOT LENGTH	L	0.45	0.6	0.75
LEAD LENGTH	L1	1.0 REF.		

5. Ordering Information

Motorcomm offers a RoHS package that is compliant with RoHS.

Table 23. Pin Assignment

Part Number	Grade	Package	Pack	Status	Operation Temp
YT9215S	Consumer	LQFP128-pin	Tray 900e.a	Engineering Sample	0 ~70 °C