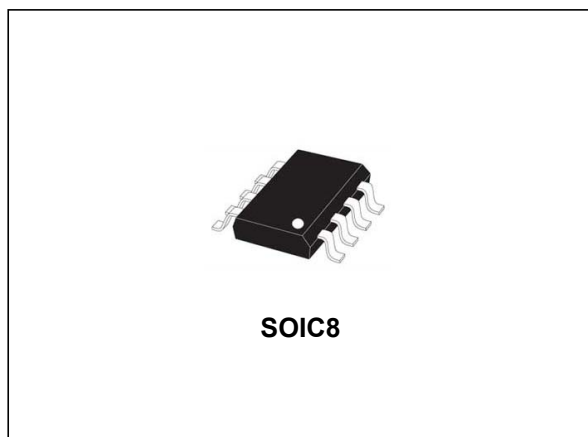


## MEMS automotive acceleration sensor: single/dual-axis with SPI interface

Datasheet - production data



### Description

The AIS1120SX / AIS2120SX is a central acceleration sensor with a single or dual axis sensing element and an IC interface able to provide acceleration information to a master control unit via an SPI protocol.

The sensing element, capable of detecting the acceleration, is manufactured using a dedicated process developed by ST to produce inertial sensors and actuators in silicon.

The IC interface is manufactured using a BCD process that allows a high level of integration. The device is factory trimmed to better tune the characteristics of the sensing element with the acceleration information to be supplied.

The AIS1120SX / AIS2120SX has a full scale of  $\pm 120\text{ g}$ . The acquisition chain consists of a C/V converter, a full-differential charge amplifier, a 2<sup>nd</sup> order  $\Sigma\Delta$  analog-to-digital converter and a digital core, which includes filtering, compensation and interpolation, control logic and SPI protocol generation.

The differential capacitance of the sensor is proportional to the proof mass displacement; thus, by sensing the differential capacitance, the position of the sensor is determined. Then, since the mass position is known, and the position is related to the input acceleration, the input acceleration can be easily deduced.

The device is available in a plastic SOIC8 package and is guaranteed to operate over a temperature range extending from  $-40\text{ }^{\circ}\text{C}$  to  $+105\text{ }^{\circ}\text{C}$ .

### Features

- AEC-Q100 qualified
- 3.3 V single supply operation
- 14-bit data output
- $\pm 120\text{ g}$  full scale
- Slow and fast offset cancellation
- Embedded self-test
- Selectable low-pass filter
- SPI interface
- ECOPACK<sup>®</sup> compliant
- Extended temperature range  $-40\text{ }^{\circ}\text{C}$  to  $+105\text{ }^{\circ}\text{C}$



### Applications

- Airbag systems
- Vibrations, impact monitoring

Table 1. Device summary

Order code	g-range	Sensitivity axes	Operating temperature range [ $^{\circ}\text{C}$ ]	Package	Packing
AIS1120SXTR	120 g	x	$-40$ to $+105$	SOIC8N	Tape and reel
AIS2120SXTR	120 g	xy	$-40$ to $+105$	SOIC8N	Tape and reel

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# 1 Block diagrams and pin description

## 1.1 Block diagrams

Figure 1. AIS1120SX block diagram

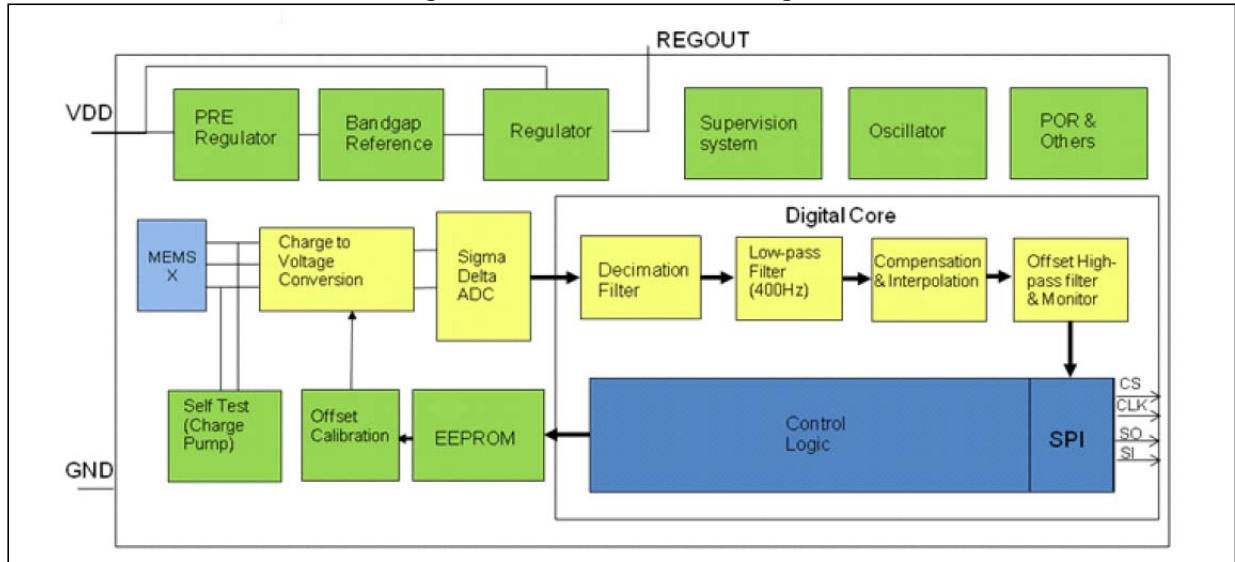
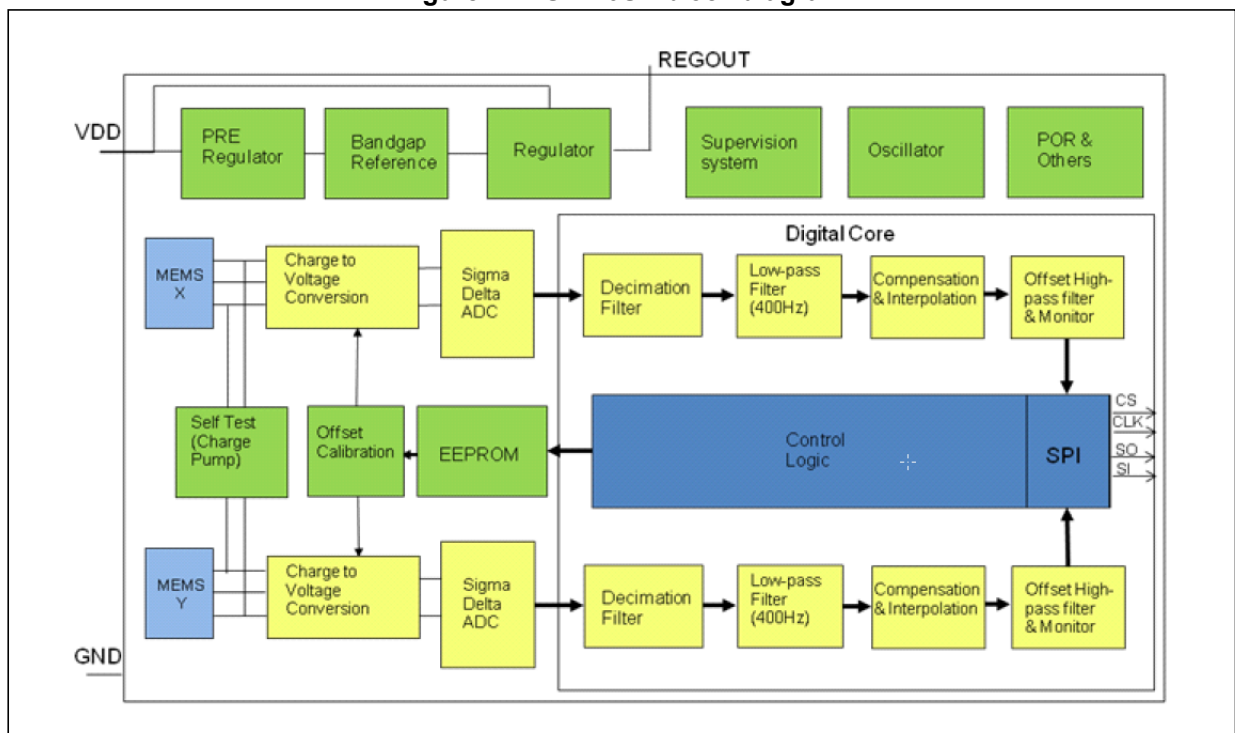


Figure 2. AIS2120SX block diagram



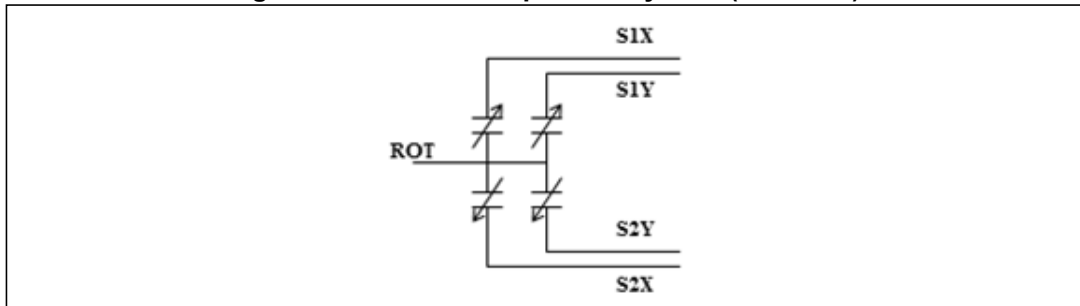


### 1.1.1 Mechanical element

A proprietary process is used to create a surface micromachined accelerometer. This technology allows processing suspended silicon structures which are attached to the substrate in few points called anchors and are free to move in the direction of the sensed acceleration thanks to flexible springs. In order to be compatible with standard packaging techniques, a cap is placed at wafer level on the top of the sensing element.

From an electrical point of view, the sensor can be represented as a differential capacitive system (see below for a dual-axis element). When the acceleration is applied to the sensor, the proof mass displaces from its nominal position, causing an unbalance in the capacitive half-bridge. This unbalance is measured using charge integration in response to a voltage pulse applied to the sense capacitor:

**Figure 3. Differential capacitive system (dual axis)**



The differential capacitive change towards acceleration can be expressed, in small displacements approximation, as:

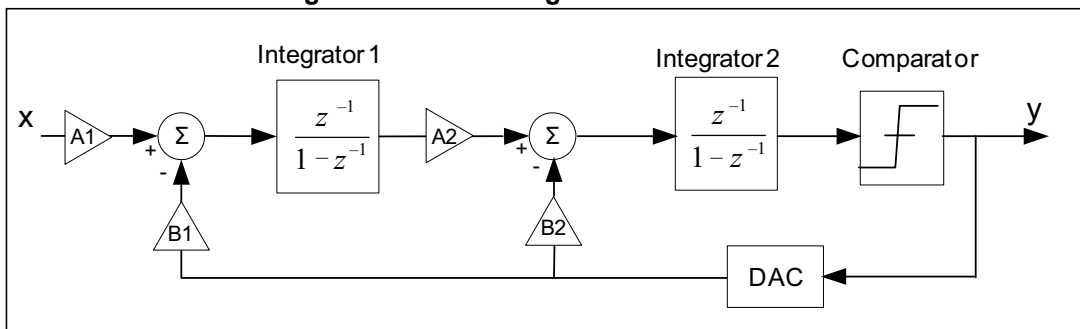
$$\Delta C = \frac{2C_0 m a}{gk}$$

Where  $C_0$  is the at-rest capacitance,  $m$  is the inertial mass,  $a$  the acceleration,  $k$  stiffness of the springs and  $g$  the distance between capacitor electrodes.

### 1.1.2 Sigma-Delta converter

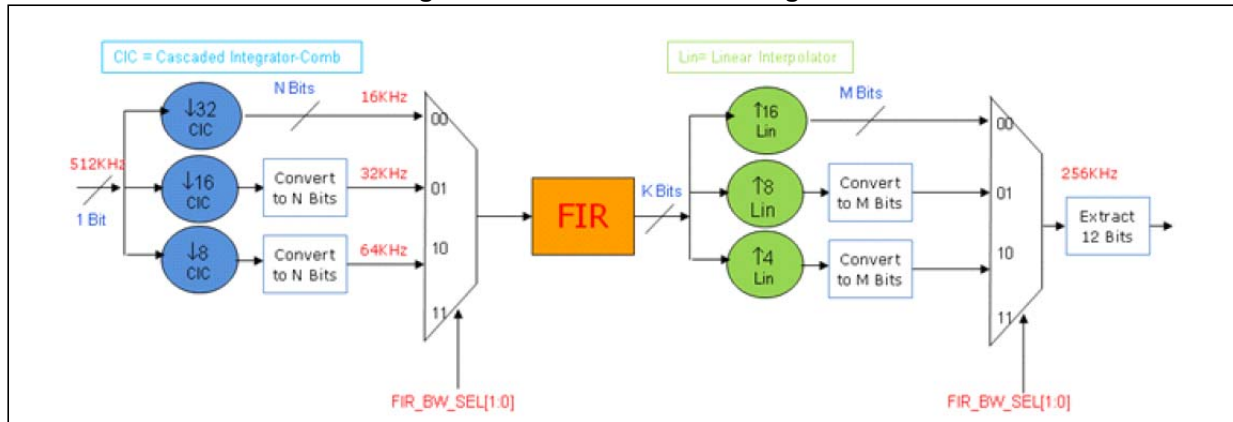
A 2<sup>nd</sup> order sigma-delta modulator is used to convert the differential voltage that comes from the charge-to-voltage converter to a pulse-density modulated (PDM) data stream. The data stream will be further processed through on-chip digital filters.

**Figure 4. 2<sup>nd</sup> order sigma-delta modulator**



### 1.1.3 Filter architecture

Figure 5. Filter architecture diagram



The architecture of the digital filters allows selecting 3 different cut-off frequencies based on 2 bits in the register map: FIR\_BW\_SEL[1:0].

The cut-off frequencies are 400 Hz, 800 Hz, and 1600 Hz. For the 1600 Hz filter, the noise level is higher and the ENOB is 10/11 bits, and not 12 bits.

The cut-off frequency has to be selected for each axis during the initialization phase. Once the initialization phase is finished and the end of the initialization bit is set, the cut-off frequency is locked and any attempt to change it during normal mode will generate an SPI error.

The cut-off frequencies can be selected as described below:

FIR\_BW\_SEL[1:0]:

- = "00" FIR with F3DB = 400 Hz is selected (default);
- = "01" FIR with F3DB = 800 Hz is selected;
- = "10" FIR with F3DB = 1600 Hz is selected (ENOB is 10/11bits in this mode);
- = "11" FIR with F3DB = 400 Hz is selected.

### 1.1.4 Decimation filter

$$H_D(z) = \left[ \frac{1 - z^{-D \times M}}{1 - z^{-1}} \right]^N$$

Differential delay: D=1

Number of sections: N=3

Decimation factor:

- M = 32 if FIR\_BW\_SEL[1:0] = "00" (400 Hz)
- M = 16 if FIR\_BW\_SEL[1:0] = "01" (800 Hz)
- M = 8 if FIR\_BW\_SEL[1:0] = "10" (1600 Hz)

### 1.1.5 Low-pass filter

H<sub>LPF</sub>(Z) is a FIR digital filter with 26 coefficients (K = 25):

$$H_{LPF}(Z) = \sum_{i=0}^K a_i Z^{-i}$$

Figure 6 and Figure 7 shows the comparison between the FIR filter and an analog Bessel filter when the cut-off frequency is 400 Hz.

Figure 6. FIR vs. 4<sup>th</sup> and 6<sup>th</sup> order Bessel filter for amplitude frequency response

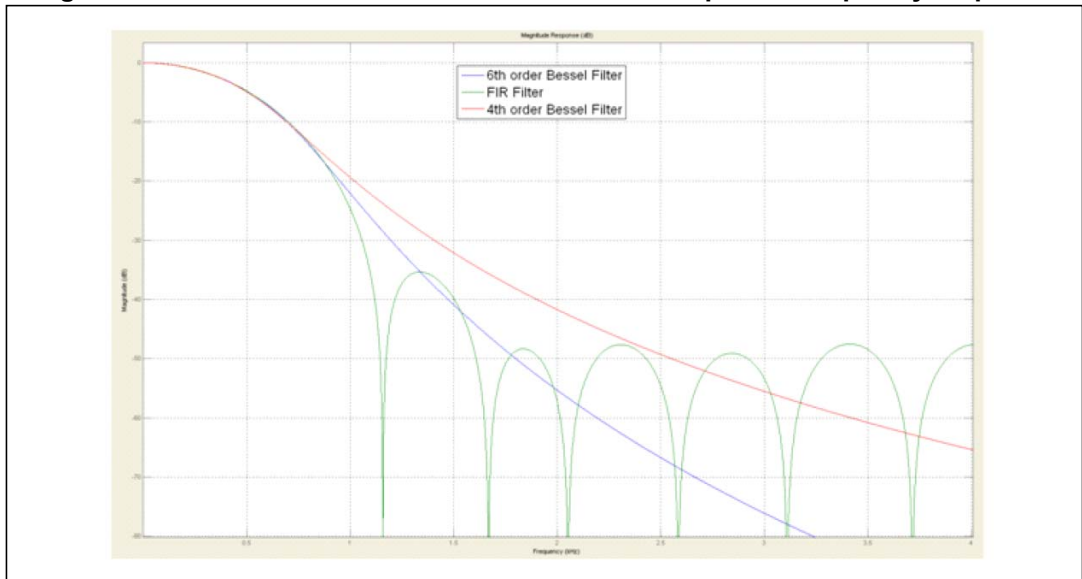
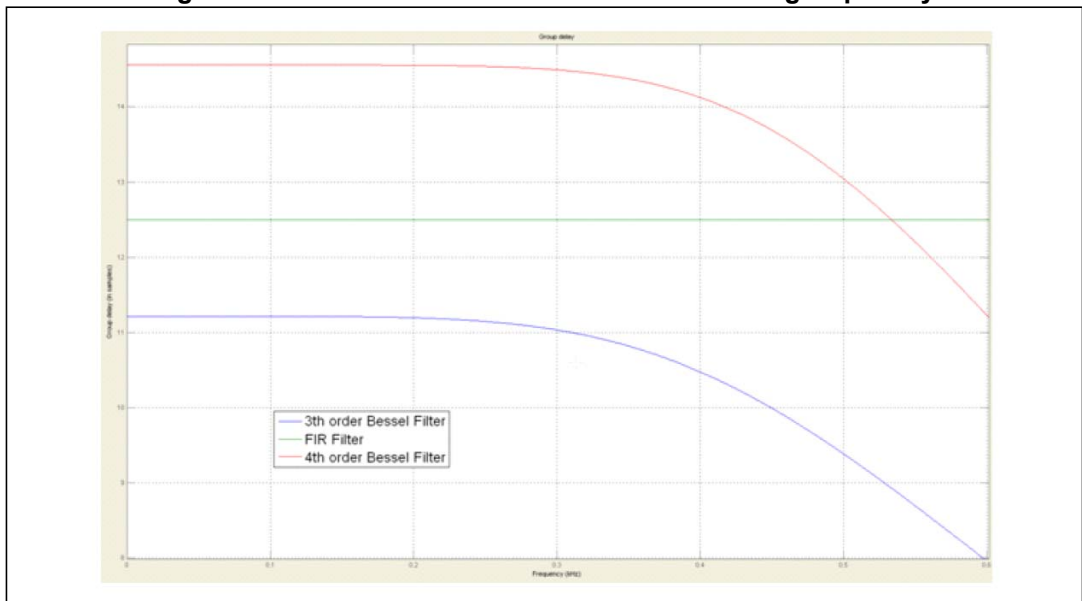


Figure 7. FIR vs. 3<sup>rd</sup> and 4<sup>th</sup> order Bessel filter for group delay



### 1.1.6 Signal compensation

On-chip EEPROM bits are used to compensate sensitivity error and offset error.

### 1.1.7 Linear interpolation

The device features an L-to-1 linear data interpolation computed from the present and the previous samples. L depends on the cut-off frequency selected:

Interpolation factor:

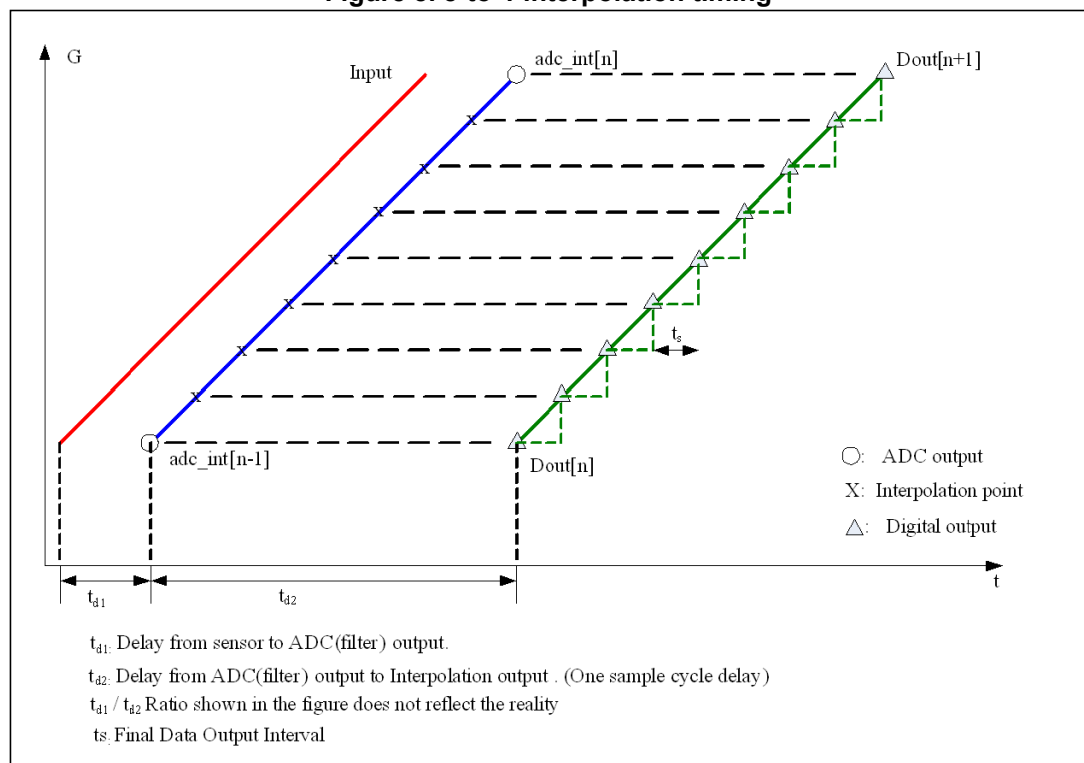
- L = 16 if FIR\_BW\_SEL[1:0] = "00" or "11"
- L = 8 if FIR\_BW\_SEL[1:0] = "01"
- L = 4 if FIR\_BW\_SEL[1:0] = "10"

The data interpolation helps reduce sample jitter. The digital result will have a latency of one sample time before being sent to the SPI bus.

The maximum jitter will be  $62.5 \mu\text{s}/16 = 3.9 \mu\text{s}$ .

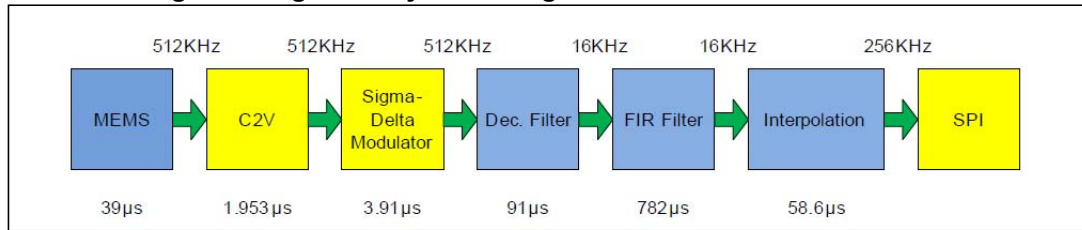
Figure 8 shows an interpolation example.

Figure 8. 8-to-1 interpolation timing

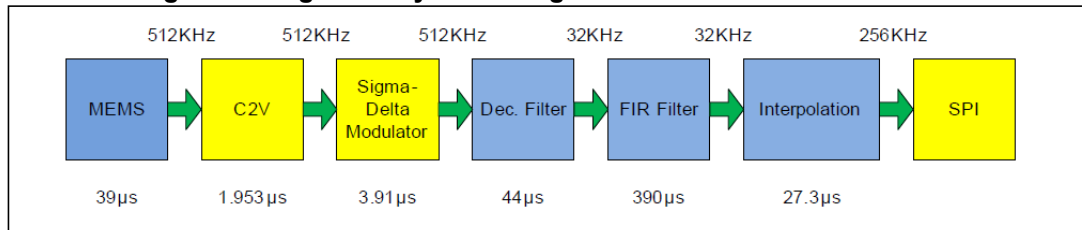


### 1.1.8 Signal delays

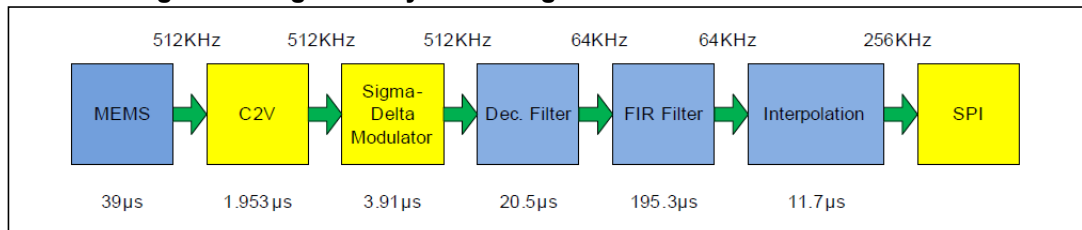
**Figure 9. Signal delay of reading-chain blocks with 400 Hz filter**



**Figure 10. Signal delay of reading-chain blocks with 800 Hz filter**



**Figure 11. Signal delay of reading-chain blocks with 1600 Hz filter**



### 1.1.9 Offset cancellation

The offset cancellation is performed in the last step of the digital signal processing and includes two modes:

1. Slow offset cancellation
2. Fast offset cancellation

The digital low-pass filter with selectable bandwidth (fast, slow cancellation) is controlled by a state machine. Fast offset cancellation is used after power-on. Slow offset cancellation, for continuously running offset cancellation, operates in normal mode.

Offset cancellation uses a moving average filter with a fixed update limit. Fast offset cancellation occurs after power up while EOI = 0. Slow offset cancellation occurs after EOI is set to 1.

The Offset Cancellation Error Flag is set when the offset is outside the offset correction range ( $\pm 1020$  LSB) during slow offset cancellation. A hardware error is indicated based on this flag being set for the affected axis. The flow chart for the offset cancellation block is shown in the following figure.

Figure 12. Offset cancellation block diagram

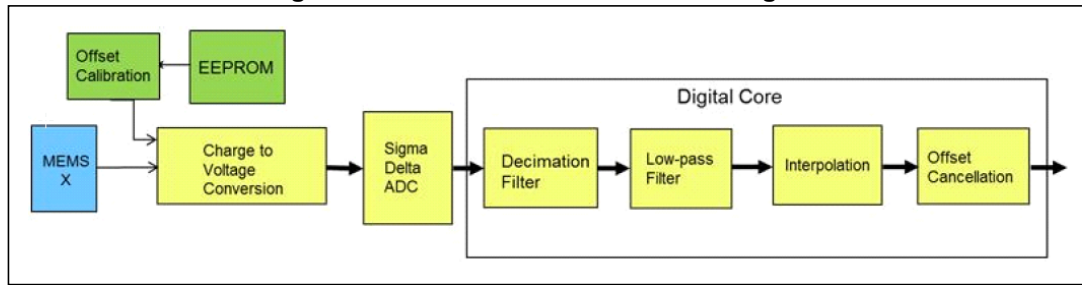
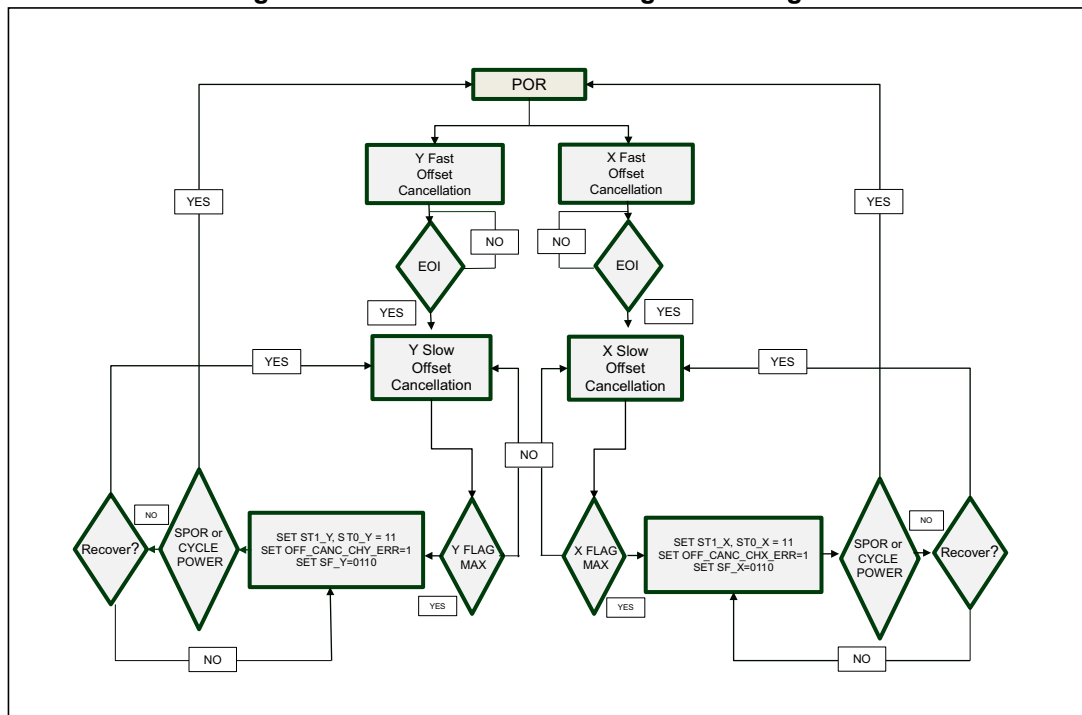


Figure 13. Offset cancellation flag monitoring flow



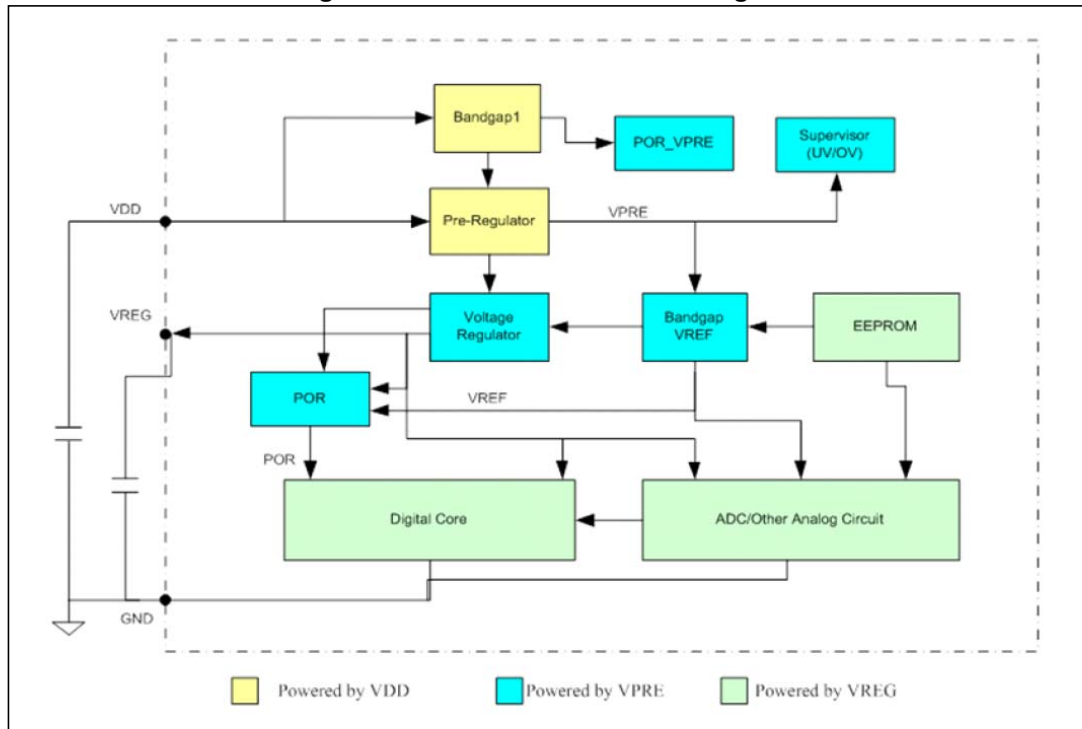
**1.1.10 State machine and on-chip-oscillator**

There is an on-chip oscillator implemented. The clock frequency is trimmed to 16.384 MHz at room temp. This clock is used for the digital core. One 1024 KHz clock divided from this main clock is used for the sigma-delta convertor and digital signal processing module (DSP).

**1.1.11 Power domain block diagram**

Figure 14 shows the power domain of the device. A pre-regulator is implemented to improve power supply sensitivity and PSRR of the device. The pre-regulator provides power to an on-chip bandgap reference and the EEPROM.

Figure 14. Power domain block diagram

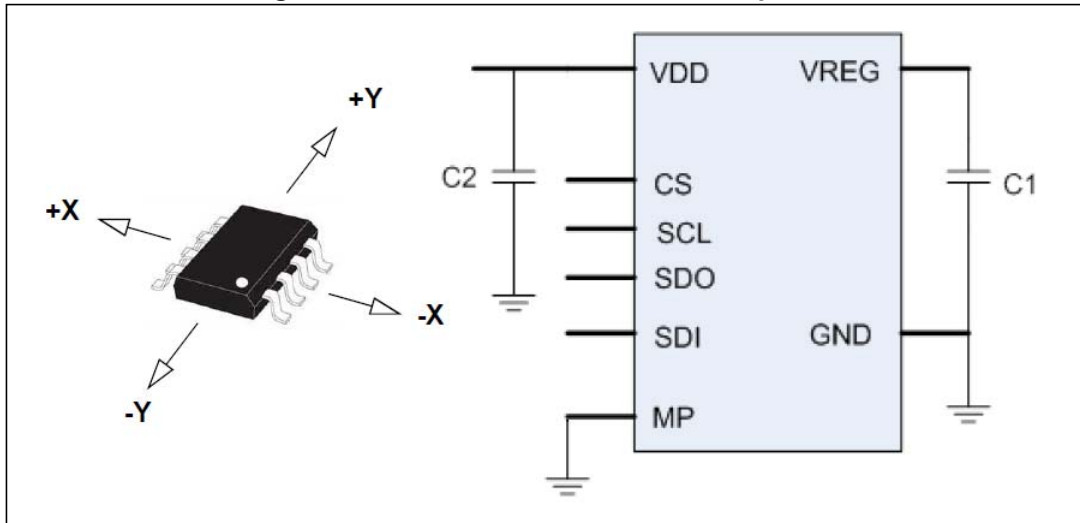


Key blocks of the power section are:

1. **Pre-regulator:** based on a self-biased supply-thermal independent structure, which is able to produce an internal stable voltage of  $2.8\text{ V} \pm 15\%$ , with a maximum output current of 3 mA. The architecture is based on a bandgap cell, which produces a thermal-independent reference, which is used in turn to produce the voltage pre-regulator output; the pre-regulator is powered by VDD, and is designed to supply only some internal low-power blocks.
2. **Regulator:** an on-chip 2.8 V regulator supplies internal power for the device; it should not be used to power other devices via the VREG terminal. A bypass capacitor is required on the VREG pin to keep the regulator stable.
3. **Bandgap reference:** the voltage bandgap is powered by the voltage pre-regulator and is used as voltage reference for all other circuits including the front-end, supervision circuits and A/D converter.
4. **Charge-to-voltage converter:** the C/V converter consists of a fully differential charge integrator with a continuous time ICMFB (Input Common Mode Feedback) control loop, discrete time ICMFB, and a Switched Capacitor OCMFB (Output Common Mode Feedback) control loop. Furthermore the C/V converter has one 9-bit DAC in order to trim the offset of the measurement chain and mechanical element.
5. **Self-test charge pump:** the self-test charge pump internally generates a voltage higher than the 2.8 V regulated supply voltage. The charge pump is activated when the self-test mode is enabled and provides an excitation voltage of 6.6 V. During the self-test the voltage is applied and disconnected to the sensor according to a duty cycle which allows simulating a well-known force on the sensor.

## 1.2 Pin description

Figure 15. Detectable accelerations and pinout



C1 = 1  $\mu$ F  $\pm$  10%, 10 V (ceramic, VREG capacitor)

C2 = 0.1  $\mu$ F  $\pm$  10%, 10 V (ceramic, power supply decoupling capacitor)

*Note:* An acceleration of the device in the "+X" or "+Y" directions results in a positive output change, a deceleration in this direction (or acceleration to the opposite side) results in a negative output signal.

Table 2. Pin description

Pin#	Name	Function
1	SCL	SPI clock
2	SDI	SPI data in
3	SDO	SPI data out
4	CS	SPI chip select
5	GND	Power supply return pin (ground level)
6	VREG	Voltage regulator output. A ceramic capacitor of 1.0 $\mu$ F $\pm$ 10% 10 V must be connected to this pin, which should not be used to power other devices.
7	VDD	This pin provides power to the device. A ceramic capacitor of 0.1 $\mu$ F $\pm$ 10% 10 V must be connected to this pin.
8	MP	Connect to GND





## 2 Customer accessible data arrays (registers)

Figure 16. Accessible registers

Address	Name	b[7]	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]	
0x00	REG_CTRL_0	0	0	0	0	0	0	0	END_OF_INIT	
0x01	REG_CTRL_1	0	0	0	0	0	SELF_TEST_CMD[2:0]			
0x02	REG_CONFIG	FIR_BW_SEL_CHY[1:0]		FIR_BW_SEL_CHX[1:0]		DIS_OFF_MON_CHY	DIS_OFF_MON_CHX	DIS_OFF_CANC_CHY	DIS_OFF_CANC_CHX	
0x03	REG_STAT_US_0	STAT_US[1:0]		TESTMODE_ENABLED	REG_CTRL_0_WR_ERR_LATCH	0	LOSSCAP_ERR_LATCH	END_OF_PWRUP_LATCH	RST_ACTIVE_LATCH	
0x04	REG_STAT_US_1	SPI_ERR	EEPROM_ERR_LATCH	0	0	OFF_CANC_CHY_ERR	OFF_CANC_CHX_ERR	REG_CONFIG_WR_ERR_LATCH	REG_CTRL_1_WR_ERR_LATCH	
0x05	REG_STAT_US_2	A2D_SAT_CHY_ERR	A2D_SAT_CHX_ERR	0	CHARGE_PUMP_ERR_LATCH	VREG_LOW_ERR	VREG_HIGH_ERR	VDD_LOW_ERR	VDD_HIGH_ERR	
0x06	REG_CHID_REVID	0	0	CHY_ACTIVE	CHX_ACTIVE	0	REVID[2:0]			
0x07	REG_ACC_CHX_LOW				REG_ACC_CHX[7:0]					
0x08	REG_ACC_CHX_HIGH	AccelDataXLatch	0				REG_ACC_CHX[13:8]			
0x09	REG_ACC_CHY_LOW				REG_ACC_CHY[7:0]					
0x0A	REG_ACC_CHY_HIGH	AccelDataYLatch	0				REG_ACC_CHY[13:8]			
0x0B	REG_OSC_COUNTER				OSC_COUNTER[7:0]					
0x0C	REG_ID_SENSOR_TYPE				ID_SENSOR_TYPE[7:0]					
0x0D	REG_ID_VEH_MANUF	0	0	0	0	ID_VEH_MANUF[3:0]				
0x0E	REG_ID_SENSOR_MANUF				ID_SENSOR_MANUF[7:0]					
0x0F	REG_ID_LOT_0				ID_LOT[7:0]					
0x10	REG_ID_LOT_1				ID_LOT[15:8]					
0x11	REG_ID_LOT_2				ID_LOT[23:16]					
0x12	REG_ID_LOT_3	0	0				ID_LOT[29:24]			
0x13	REG_ID_WAFER	0	0	0				ID_WAFER[4:0]		
0x14	REG_ID_COOR_X				ID_COOR_X[7:0]					
0x15	REG_ID_COOR_Y				ID_COOR_Y[7:0]					
0x16	REG_RESET	0	0	0	0	0	0	SOFT_RST[1:0]		
0x17	OFF_CHX_HIGH				OFF_CHX[10:3]					
0x18	OFF_CHX_LOW	OffDataXLatch	0	0	0	0	OFF_CHX[2:0]			
0x19	OFF_CHY_HIGH				OFF_CHY[10:3]					
0x1A	OFF_CHY_LOW	OffDataYLatch	0	0	0	0	OFF_CHY[2:0]			
0x1B	Not used	0	0	0	0	0	0	0	0	
0x1C	Not used	0	0	0	0	0	0	0	0	
0x1D	Not used	0	0	0	0	0	0	0	0	
0x1E	Reserved									
0x1F	Reserved									

## 2.1 REG\_CTRL\_0

Table 3. REG\_CTRL\_0

REG_CTRL_0 (address: 0x00)				
Name	Bit#	R/W	Reset state	Description
0	[7:1]	R	0	
END_OF_INIT	0	R/W	0	<p>End of initialization: Initialization is the time interval from reset to Self-test end:</p> <p>= "0" then device is in Initialization Phase</p> <p>= "1" then the device is in end of initialization phase (device is in normal mode)</p> <p>Rules :</p> <ul style="list-style-type: none"> <li>-When END_OF_BIT="1" then writing operations of REG_CTRL_1 and REG_CONFIG bits do not have effect and generate error flags CTRL_REG_1_WR_ERR="1"/CONFIG_REG_WR_ERR="1".</li> <li>-Cannot write EOI='1' if there is EE or HE error.</li> <li>-Cannot write EOI='1' if device is in +ve or -ve self-test (either CHX or CHY). Doing so, RE error (and CONFIG_REG_0_WR_ERR='1') will be produced</li> </ul>

## 2.2 REG\_CTRL\_1

Table 4. REG\_CTRL\_1

REG_CTRL_1 (address: 0x01)				
Name	Bit#	R/W	Reset state	Description
0	[7:3]	R	0	
SELF_TEST_CMD	[2:0]	R/W	0	<p>Self-test commands:</p> <ul style="list-style-type: none"> <li>= "000" then device is in 0 g self-test if EOI='0';</li> <li>= "001" then device starts self-test on channel X with positive voltage;</li> <li>= "010" then device starts self-test on channel X with negative voltage;</li> <li>= "011" then device is in 0 g self-test if EOI='0'</li> <li>= "100" then device is in 0 g self-test if EOI='0'</li> <li>= "101" then device starts self-test on channel Y with positive voltage;</li> <li>= "110" then device starts self-test on channel Y with negative voltage;</li> <li>= "111" then device is in 0 g self-test if EOI='0'</li> </ul> <p>Rules :</p> <ul style="list-style-type: none"> <li>-Cannot write if EOI='1'</li> <li>-Cannot start a self-test on CHX/CHY if the channel is not enabled</li> <li>-Cannot switch from non-0g(-ve/+ve) self_test to another non-0g self_test(-ve/+ve) without going to 0g self-test</li> </ul> <p>Note:</p> <p>When starting channel X self-test:</p> <ul style="list-style-type: none"> <li>Channel X acceleration command will read channel X self-test value</li> <li>Channel Y acceleration command will read temperature sensor value for self-test temperature compensation algorithm.</li> </ul> <p>When starting channel Y self-test:</p> <ul style="list-style-type: none"> <li>Channel X acceleration command will read temperature sensor value for self-test temperature compensation algorithm.</li> <li>Channel Y acceleration command will read channel Y self-test value</li> </ul>

## 2.3 REG\_CONFIG

Table 5. REG\_CONFIG

REG_CONFIG (address: 0x02)				
Name	Bit#	R/W	Reset state	Description
FIR_BW_SEL_CHY[1:0]	[7:6]	R/W	00	<p>Channel Y FIR bandwidth selection bits:</p> <p>if = "00" FIR with F3DB = 400 Hz is selected;</p> <p>if = "01" FIR with F3DB = 800 Hz is selected;</p> <p>if = "10" FIR with F3DB = 1600 Hz is selected (resolution is 10/11bits in this mode);</p> <p>if = "11" FIR with F3DB = 400 Hz is selected.</p> <p>FIR_BW_SEL_CHY[1:0] is writable if END_OF_INIT="0".</p> <p>Writing FIR_BW_SEL_CHY[1:0] when END_OF_INIT="1" or when Channel Y self-test is activated, does not have effect and generates an error:</p> <p>CONFIG_REG_WR_ERR="1".</p>
FIR_BW_SEL_CHX[1:0]	[5:4]	R/W	00	<p>Channel X FIR bandwidth selection bits:</p> <p>if = "00" FIR with F3DB = 400 Hz is selected;</p> <p>if = "01" FIR with F3DB = 800 Hz is selected;</p> <p>if = "10" FIR with F3DB = 1600 Hz is selected (resolution is 10/11bits in this mode);</p> <p>if = "11" FIR with F3DB = 400 Hz is selected.</p> <p>FIR_BW_SEL_CHX[1:0] is writable if END_OF_INIT="0".</p> <p>Writing FIR_BW_SEL_CHX[1:0] when END_OF_INIT="1" or when Channel X self-test is activated does not have effect and generates an error:</p> <p>CONFIG_REG_WR_ERR="1".</p>
DIS_OFF_MON_CHY	3	R/W	0	<p>Offset monitor channel Y disable bit.</p> <p>if = "0" then channel Y offset monitor is on;</p> <p>if = "1" then channel Y offset monitor is off.</p> <p>DIS_OFF_MON_CHY is writable if END_OF_INIT="0".</p> <p>Writing DIS_OFF_MON_CHY when END_OF_INIT="1" does not have effect and generates an error:</p> <p>CONFIG_REG_WR_ERR="1"</p>

Table 5. REG\_CONFIG (continued)

REG_CONFIG (address: 0x02)				
Name	Bit#	R/W	Reset state	Description
DIS_OFF_MON_CHX	2	R/W	0	Offset monitor channel X disable bit. = "0" then channel X offset monitor is on; = "1" then channel X offset monitor is off. DIS_OFF_MON_CHX is writable if END_OF_INIT="0". Writing DIS_OFF_MON_CHX when END_OF_INIT="1" does not have effect and generates an error: CONFIG_REG_WR_ERR="1"
DIS_OFF_CANC_CHY	1	R/W	0	Offset cancellation channel Y disable bit. = "0" then channel Y offset cancellation circuit is on; = "1" then channel Y offset cancellation circuit is off. DIS_OFF_CANC_CHY is writable if END_OF_INIT="0". Writing DIS_OFF_CANC_CHY when END_OF_INIT="1" does not have effect and generates an error: CONFIG_REG_WR_ERR="1"
DIS_OFF_CANC_CHX	0	R/W	0	Offset cancellation channel X disable bit. = "0" then channel X offset cancellation circuit is on; = "1" then channel X offset cancellation circuit is off. DIS_OFF_CANC_CHX is writable if END_OF_INIT="0". Writing DIS_OFF_CANC_CHX when END_OF_INIT="1" does not have effect and generates an error: CONFIG_REG_WR_ERR="1"

## 2.4 REG\_STATUS

Table 6. REG\_STATUS\_0

REG_STATUS_0 (address: 0x03)				
Name	Bit#	R/W	Reset state	Description
STATUS [1:0]	[7:6]	R	00	Status Error bits: if = "00" device is in initialization phase (power-up, configuration, fast offset cancellation); if = "01" device is in normal mode (EOI = 1); if = "10" device is test phase (0 g test or active self test); EOI = 0; if = "11" device is in initialization phase or normal mode and some errors are detected: acceleration data are disregarded due to errors in device.
TESTMODE_ENABLED	5	R	0	"0": normal mode; "1": test mode
REG_CTRL_0_WR_ERR <sup>(1)</sup>	4	R	0	Will be set to '1' if write EOI = '1' attempt is made with the device in +ve or -ve self-test (either CHX or CHY).
Not used	3	R	0	"0" always
LOSS_CAP	2	R	0	Loss of capacitor: if = "0" then loss of capacitor is not detected (correct behavior); if = "1" then loss of capacitor is detected (wrong behavior).  Note: 1.LOSS_CAP check is done during the power-up stage (~400 µs after POR) only. 2.Recommended VDD ramp rate >1 V/ms 3.It is recommended that LOSS_CAP flag (and all other hardware flags) be reconfirmed with soft POR after power up (END_OF_PWRUP='1').
END_OF_PWRUP	1	R	0	"1": end of power-up sequence; ready for self-test.
RST_ACTIVE	0	R	0	Reset Active bit: if = "0" then device is out of reset; if = "1" then device has undergone a soft reset sequence. Cleared by a read.

1. Bit not latched (cleared by any read command).

Table 7. REG\_STATUS\_1

REG_STATUS_1 (address: 0x04)				
Name	Bit#	R/W	Reset state	Description
SPI_ERR <sup>(1)</sup>	7	R	0	SPI error: if = "0" then SPI format data is compliant with specifications (correct behavior); if = "1" then SPI format data is not complaint with specifications (wrong behavior).
EEPROM_ERR	6	R	0	EEPROM Error: CRC error reading EEPROM. if = "0" EEPROM reading is correct. if = "1" EEPROM reading is wrong. The bit can be cleared by a READ if NVM bit ErrFlgCfg='1'. If ErrFlgCfg='0', then this bit can't be cleared.
Not used	5:4	R	0	"0" always
OFF_CANC_CHY_ERR	3	R	0	The sensor sets this flag when the offset is outside the offset monitoring threshold ( $\pm 1020$ LSB) during slow offset cancellation for channel Y; this also creates hardware failure. When the offset is within the threshold, the flag will be '0' (not latched)
OFF_CANC_CHX_ERR	2	R	0	The sensor sets this flag when the offset is outside the offset monitoring threshold ( $\pm 1020$ LSB) during slow offset cancellation for channel X; this also creates hardware failure. When the offset is within the threshold, the flag will be '0' (not latched)
REG_CONFIG_WR_ERR <sup>(1)</sup>	1	R	0	Configuration register writing operation error: if = "0" then a writing operation is not addressed by the SPI on REG_CONFIG register when END_OF_INIT=1 (correct behavior); if = "1" then a writing operation is addressed by the SPI on REG_CONFIG register when END_OF_INIT=1 (wrong behavior).
REG_CTRL_1_WR_ERR <sup>(1)</sup>	0	R	0	Control register 1 writing operation error: if = "0" then a writing operation is not addressed by the SPI on REG_CNTR_1 register when END_OF_INIT=1 (correct behavior); if = "1" then a writing operation is addressed by the SPI on REG_CNTR_1 register when END_OF_INIT=1 (wrong behavior).

1. Bit not latched (cleared by any read command).

Table 8. REG\_STATUS\_2

REG_STATUS_2 (address: 0x05)				
Name	Bit#	R/W	Reset state	Description
A2D_SAT_CHY	7	R	0	if = "1" then CHY ADC saturation detected (wrong behavior).
A2D_SAT_CHX	6	R	0	if = "1" then CHX ADC saturation detected (wrong behavior).
Not used	5	R	0	
CHARGE_PUMP_ERR	4	R	0	Charge pump error: if = "0" then charge pump error is not detected (correct behavior); if = "1" charge pump error is detected (wrong behavior).
VREG_LOW_VOLT_DET	3	R	0	VREG low-voltage detection: if = "0" then regulated voltage VREG is over the minimum supply voltage (correct behavior); if = "1" then regulated voltage VREG is under the minimum supply voltage (wrong behavior). This also creates hardware failure (not latched).
VREG_HIGH_VOLT_DET	2	R	0	VREG high-voltage detection: if = "0" then regulated voltage VREG is under the maximum supply voltage (correct behavior); if = "1" then regulated voltage VREG is over the maximum supply voltage (wrong behavior). This also creates hardware failure (not latched).
VDD_LOW_VOLT_DET	1	R	0	VDD low-voltage detection: if = "0" then supply voltage VDD is over the minimum supply voltage (correct behavior); if = "1" then supply voltage VDD is under the minimum supply voltage (wrong behavior). This also creates hardware failure (not latched).
VDD_HIGH_VOLT_DET	0	R	0	VDD high-voltage detection: if = "0" then supply voltage VDD is under the maximum supply voltage (correct behavior); if = "1" then supply voltage VDD is over the maximum supply voltage (wrong behavior). This also creates hardware failure (not latched).



## 2.5 REG\_CHID\_REVID

Table 9. REG\_CHID\_REVID

REG_CHID_REVID (address: 0x06)				
Name	Bit#	R/W	Reset state	Description
Not used	7	R	0	
Not used	6	R	0	
CHY_ACTIVE	5	R	0	= "1": CHY reading chain enabled (copied NVM bit)
CHX_ACTIVE	4	R	0	= "1": CHX reading chain enabled (copied NVM bit)
Not used	3	R	0	
REVID	[2:0]	R	0	Copied NVM bits 0x7C: bit 7 to bit 5 011 for A3 100 for A4

## 2.6 REG\_ACC\_CHX\_LOW

Table 10. REG\_ACC\_CHX\_LOW

REG_ACC_CHX_LOW (address: 0x07)				
Name	Bit#	R/W	Reset state	Description
REG_ACC_CHX	[7:0]	R	0x00	Channel X acceleration data LSBs register

## 2.7 REG\_ACC\_CHX\_HIGH

Table 11. REG\_ACC\_CHX\_HIGH

REG_ACC_CHX_HIGH (address: 0x08)				
Name	Bit#	R/W	Reset state	Description
AccelDataXLatch	7	R	0	Reading REG_ACC_CHX_LOW register sets the bit to '1' and REG_ACC_CHX_HIGH is locked to its corresponding LOW byte i.e REG_ACC_CHX_LOW; Cleared when it is read.
Not used	6	R	0	
REG_ACC_CHX	[5:0]	R	0	Channel X acceleration data MSBs register

## 2.8 REG\_ACC\_CHY\_LOW

Table 12. REG\_ACC\_CHY\_LOW

REG_ACC_CHY_LOW (address: 0x09)				
Name	Bit#	R/W	Reset state	Description
REG_ACC_CHY	[7:0]	R	0x00	Channel Y acceleration data LSBs register

## 2.9 REG\_ACC\_CHY\_HIGH

Table 13. REG\_ACC\_CHY\_HIGH

REG_ACC_CHY_HIGH (address: 0x0A)				
Name	Bit#	R/W	Reset state	Description
AccelDataYLatch	7	R	0	Reading REG_ACC_CHY_LOW register sets the bit to '1' and REG_ACC_CHY_HIGH is locked to its corresponding LOW byte, i.e. REG_ACC_CHY_LOW; Cleared when it is read.
Not used	6	R	0	
REG_ACC_CHY	[5:0]	R	0	Channel Y acceleration data MSBs register

## 2.10 REG\_OSC\_COUNTER

Table 14. REG\_OSC\_COUNTER

REG_OSC_COUNTER (address: 0x0B)				
Name	Bit#	R/W	Reset state	Description
OSC_COUNTER	[7:0]	R	0x00	Free run oscillator counter to verify oscillator is running. The counter is updated every 8 kHz. To verify oscillator frequency, the ECU can compare the oscillator counter by reading the ECU clock.

## 2.11 REG\_ID\_SENSOR\_TYPE

Table 15. REG\_ID\_SENSOR\_TYPE

REG_ID_SENSOR_TYPE (address: 0x0C)				
Name	Bit#	R/W	Reset state	Description
ID_SENSOR_TYPE	[7:0]	R	0x00	0x1A for single axis sensor; 0x2A for dual axis sensor.

## 2.12 REG\_ID\_VEH\_MANUF

Table 16. REG\_ID\_VEH\_MANUF

REG_ID_VEH_MANUF (address: 0x0D)				
Name	Bit#	R/W	Reset state	Description
Not used	[7:4]	R	0	
ID_VEH_MANUF	[3:0]	R	0x00	Vehicle manufacturer ID number "0x00"

## 2.13 REG\_ID\_SENSOR\_MANUF

Table 17. REG\_ID\_SENSOR\_MANUF

REG_ID_SENSOR_MANUF (address: 0x0E)				
Name	Bit#	R/W	Reset state	Description
ID_SENSOR_MANUF	[7:0]	R	0x00	Sensor manufacturer ID number LSBs ("0x00")

## 2.14 REG\_ID\_LOT\_0

Table 18. REG\_ID\_LOT\_0

REG_ID_LOT_0 (address: 0x0F)				
Name	Bit#	R/W	Reset state	Description
ID_LOT[7:0]	[7:0]	R	0	ASIC lot ID number [7:0]

## 2.15 REG\_ID\_LOT\_1

Table 19. REG\_ID\_LOT\_1

REG_ID_LOT_1 (address: 0x10)				
Name	Bit#	R/W	Reset state	Description
ID_LOT[15:8]	[7:0]	R	0	ASIC lot ID number [15:8]

## 2.16 REG\_ID\_LOT\_2

Table 20. REG\_ID\_LOT\_2

REG_ID_LOT_2 (address: 0x11)				
Name	Bit#	R/W	Reset state	Description
ID_LOT[23:16]	[7:0]	R	0	ASIC lot ID number [23:16]

## 2.17 REG\_ID\_LOT\_3

Table 21. REG\_ID\_LOT\_3

REG_ID_LOT_3 (address: 0x12)				
Name	Bit#	R/W	Reset state	Description
Not used	[7:6]	R	0	
ID_LOT[29:24]	[5:0]	R	0	ASIC lot ID number [29:24]

## 2.18 REG\_ID\_WAFER

Table 22. REG\_ID\_WAFER

REG_ID_WAFER (address: 0x13)				
Name	Bit#	R/W	Reset state	Description
Not used	[7:5]	R	0	
ID_WAFER	[4:0]	R	0	ASIC wafer ID number

## 2.19 REG\_ID\_COOR\_X

Table 23. REG\_ID\_COOR\_X

REG_ID_COOR_X (address: 0x14)				
Name	Bit#	R/W	Reset state	Description
ID_COOR_X	[7:0]	R	0x00	Die coordinate X

## 2.20 REG\_ID\_COOR\_Y

Table 24. REG\_ID\_COOR\_Y

REG_ID_COOR_Y (address: 0x15)				
Name	Bit#	R/W	Reset state	Description
ID_COOR_Y	[7:0]	R	0x00	Die coordinate Y

## 2.21 REG\_RESET

Table 25. REG\_RESET

REG_RESET (address: 0x16)				
Name	Bit#	R/W	Reset state	Description
Not used	[7:3]	R	0	
SOFT_RST	[1:0]	R/W	00	Software reset: device is caused to go under reset if 3 consecutive SPI write operations are executed in the following sequence: 1. SOFT_RST[1:0]=10; 2. SOFT_RST[1:0]=01; 3. SOFT_RST[1:0]=10.

## 2.22 OFF\_CHX\_HIGH

Table 26. OFF\_CHX\_HIGH

OFF_CHX_HIGH (address: 0x17)				
Name	Bit#	R/W	Reset state	Description
OFF_CHX[10:3]	[7:0]	R	0x00	Channel X offset correction data MSB register

## 2.23 OFF\_CHX\_LOW

Table 27. OFF\_CHX\_LOW

OFF_CHX_LOW (address: 0x18)				
Name	Bit#	R/W	Reset state	Description
OFFDataXLatch	7	R	0	Reading OFF_CHX_HIGH register sets the bit to "1" and OFF_CHX_LOW is locked to its corresponding HIGH byte i.e. OFF_CHX_HIGH; Cleared when it is read.
Not used	[6:3]	R	0	
OFF_CHX[2:0]	[2:0]	R	0	Channel X offset correction data LSB register

## 2.24 OFF\_CHY\_HIGH

Table 28. OFF\_CHY\_HIGH

OFF_CHY_HIGH (address: 0x19)				
Name	Bit#	R/W	Reset state	Description
OFF_CHY[10:3]	[7:0]	R	0x00	Channel Y offset correction data MSB register

## 2.25 OFF\_CHY\_LOW

Table 29. OFF\_CHY\_LOW

OFF_CHY_LOW (address: 0x1A)				
Name	Bit#	R/W	Reset state	Description
OFFDataYLatch	7	R	0	Reading OFF_CHY_HIGH register sets the bit to "1" and OFF_CHY_LOW is locked to its corresponding HIGH byte i.e. OFF_CHY_HIGH; Cleared when it is read.
Not used	[6:3]	R	0	
OFF_CHY[2:0]	[2:0]	R	0	Channel Y offset correction data LSB register

## 2.26 Other addresses

0x1B: not used

0x1C: not used

0x1D: not used

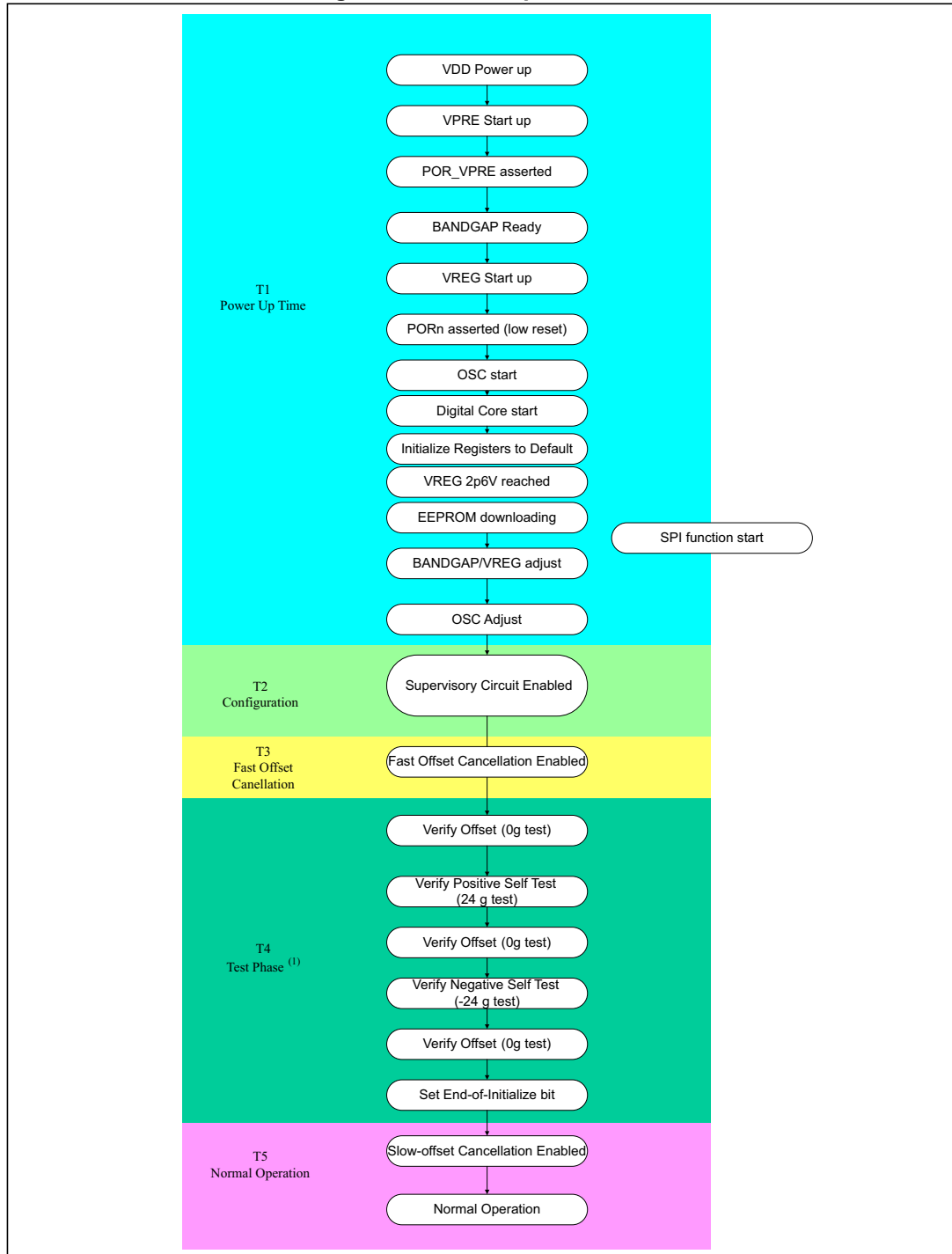
0x1E: Reserved

0x1F: Reserved

### 3 Power-on phase and initialization

#### 3.1 Initialization procedure

Figure 17. Power-up flowchart



1. User initiated

### 3.2 Phase1 (T1): Power-up timing

The power domain block diagram is shown in section 1.1.11. Power-up timing and sequence are shown in Figure 18. Once VDD has ramped up, VPRE follows that. After VPRE reaches a threshold value, internal signal nPOR\_VPRE is asserted. The signal resets the EEPROM registers. Therefore, EEPROM settings are ready for bandgap and regulator output (VREG). Then, another POR circuit will monitor the output VREG. If it reaches a target threshold, nPOR will be asserted. nPOR is used to reset all the registers of the main digital core.

The device waits for regulator and bandgap to be at appropriate levels (regulator >2.6 V, bandgap >1.1 V) before it starts executing its state machine (starting with EEPROM download). The device starts its state machine approximately 5 μs (deglitch time) after the bandgap and regulator reach their threshold levels.

Figure 18. Power-up timing

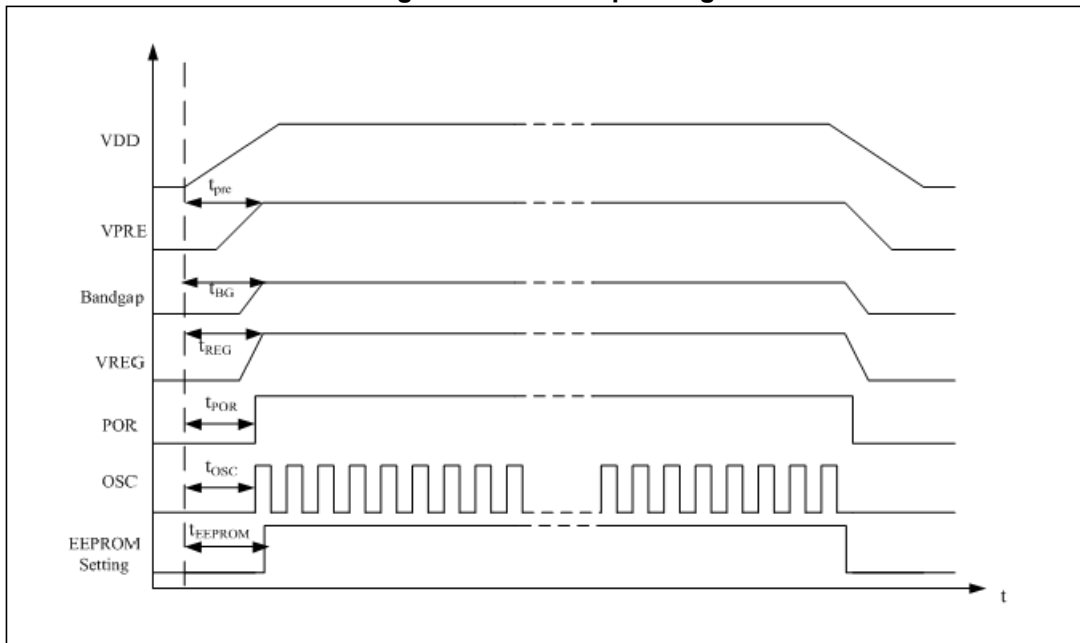


Table 30 shows the typical timing delay for each block:

Table 30. Timing delay by block

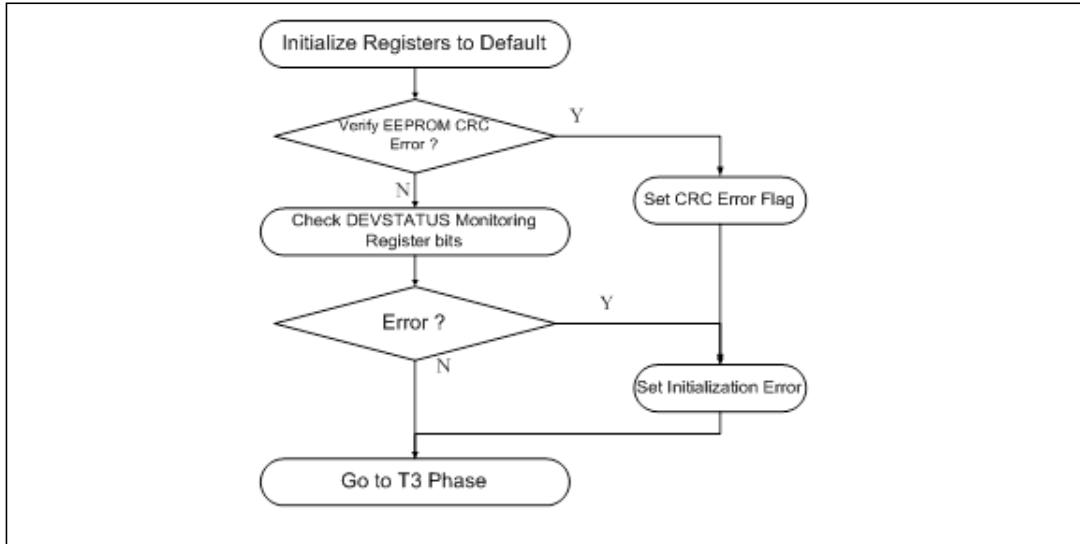
Timing	Condition (VDD rising time of 100μs)	Delay [μs]
$t_{pre}$	VPRE settles down to 90%	90
$t_{BG}$	VREF settles down to 90%	250
$t_{POR}$		190
$t_{REG}$	VREG settles down to 90%	250
$t_{EEPROM}$		450
$t_{OSC}$		195



### 3.3 Phase2 (T2): configuration

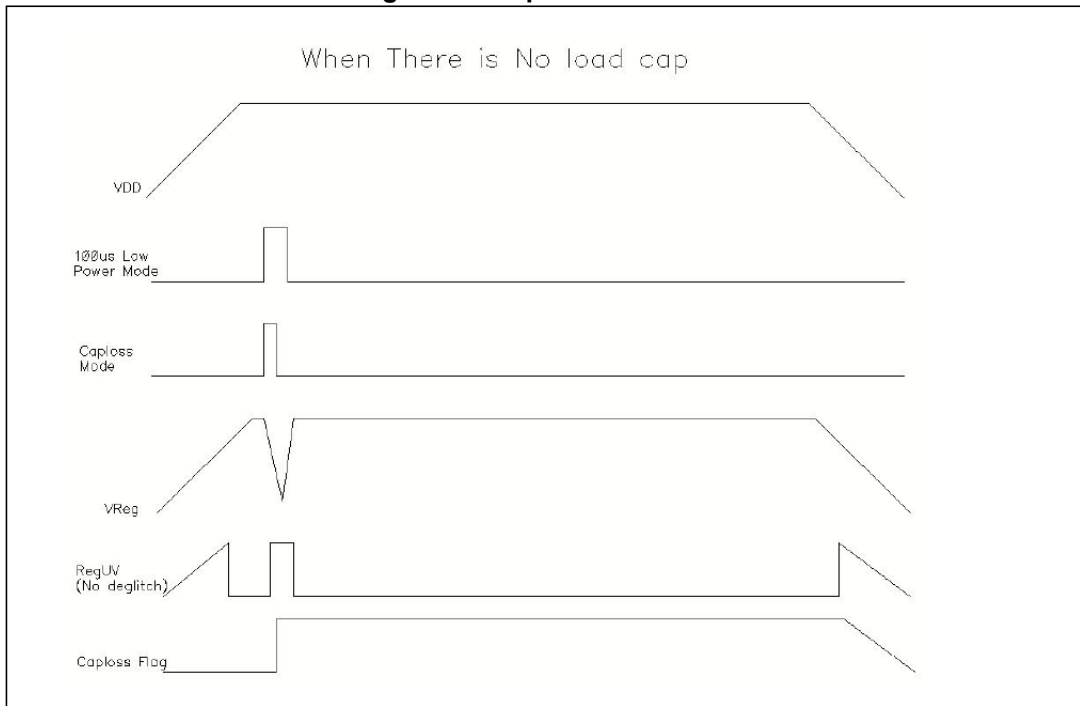
Once nPOR is asserted, the device will initialize the registers to the default settings and start ASIC diagnostic procedure. If an error is detected, the corresponding error bit will be set in DEVSTAT register. This phase is characterized by (ST1:ST0 = "00").

Figure 19. Phase 2 state flow



The diagnostic procedure in this stage includes cap-loss detection, charge pump check for self-test, and VREG/VCC low-voltage monitoring. Cap-loss mode is initiated after EEPROM download where the regulator is disabled 1  $\mu$ s. Without a load cap the regulator voltage would fall below the UV threshold and the device latches it as cap-loss flag.

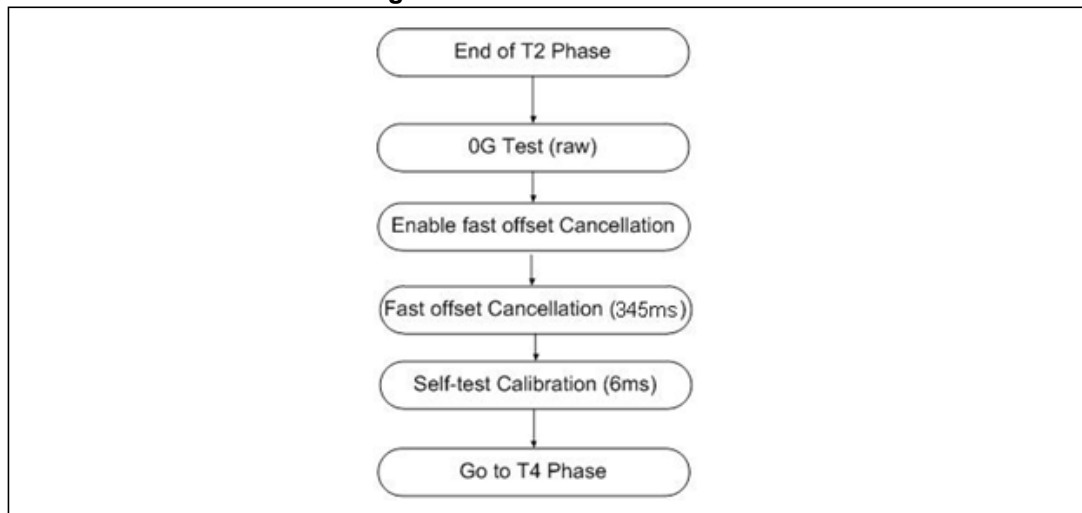
Figure 20. Cap-loss detection



### 3.4 Phase 3 (T3): fast offset cancellation

After the configuration/initialization phase (t2), the device will start fast offset cancellation which takes max. 345 ms. Also there is 6 ms window for self-test calibration. During phase 3 (t3), sensor data is still available through the SPI but the ND flag (see [Section 5.1.1: Acceleration commands](#)) will be used and ST1:ST0 is still kept "00" if no error occurs until phase T4.

Figure 21. Phase 3 state flow



### 3.5 Phase 4 (T4): test phase

After phase 3 the device is still in the programming phase. Offset is close to 0. This phase is characterized by (ST1:ST0 = "10"). The device can be programmed to execute the active self-test. The actuation of transducer will be controlled through SPI command.

The active self-test applies an electrostatic force to the mechanical sensor. When the self-test mode is activated, the voltage between the rotor and stator is changed. This generates an attractive electrostatic force and causes the rotor to move towards the stator. The displacement of the rotor will be measured at the output of the ADC.

*Note: For the 2-axis version the self-test has to be executed sequentially.*

When starting channel X self-test:

- a) Channel X acceleration command will read channel X self-test value
- b) Channel Y acceleration command will read temperature sensor value for self-test temperature compensation algorithm.

When starting channel Y self-test:

- a) Channel X acceleration command will read temperature sensor value for self-test temperature compensation algorithm.
- b) Channel Y acceleration command will read channel Y self-test value

The acceleration data is given in 14-bit format (bit 25-12 of SDO data frame). Its MSB (D13) represents the sign bit and the negative value is in two's complementary format.

When configured/read as a temperature sensor value, the 14-bit output is unsigned data. Its value could be estimated as:

$$\text{ADC\_out} = -16 \times (\text{Temp} - 25) + 7280$$

The following table shows a few examples of temperature sensor data.

**Table 31. Temperature sensor data example**

Temp. (°C)	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
-40	1	0	0	0	0	0	1	0	0	0	0	0	0	0
25	0	1	1	1	0	0	0	1	1	1	0	0	0	0
105	0	1	0	1	1	1	0	1	1	1	0	0	0	0

Temperature compensation is only enabled during the active self-test phase.

### 3.6 Phase 5 (T5): normal operation

After the programming phase the ECU will set the End-of-Initialization (EOI) bit and the device will start normal operation. ST1:ST0 is switched to "01".

## 4 Mechanical and electrical specifications

### 4.1 Mechanical characteristics

$3.13\text{ V} \leq V_{DD} \leq 3.47\text{ V}$ ,  $-40^{\circ}\text{C} \leq T_{OP} \leq 105^{\circ}\text{C}$ , acceleration = 0 g, over lifetime, unless otherwise noted.

**Table 32. Mechanical characteristics**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
FS	Full-scale range <sup>(1)</sup>	Offset cancellation ON	±114	±120		g
S <sub>0</sub>	Sensitivity			68		LSB/g
S <sub>E</sub>	Sensitivity Error	V <sub>DD</sub> = 3.3 V T = 25°C Frequency = 0 Hz At time t = 0 Including ratiometric error	-5		+5	%
S <sub>RE</sub>	Sensitivity ratiometricity error	V <sub>DD</sub> = 3.6 V to PD threshold	-1		+1	%
TCS <sub>0</sub>	Sensitivity change vs temperature	-40°C ≤ T <sub>OP</sub> ≤ 105°C		±0.02		LSB/g/°C
S <sub>O_drift</sub>	Sensitivity drift	Over lifetime			1	%
DNL	Differential non linearity				4	LSB
Off_Raw <sub>1</sub>	Zero-g level offset <sup>(2)</sup>	Including ratiometric error, excluding noise effects, offset cxl disabled	-680		680	LSB
Off_Cxl <sub>1</sub>	Zero-g level offset	Including ratiometric error, excluding noise effects, offset cxl enabled	-2		2	LSB
Off_Mon_Th	Offset monitor threshold	Signed value	-1020		1020	LSB
Off_Mon_HdD	Offset monitor Headroom		-400		400	LSB
NL	Non linearity of sensitivity <sup>(1)</sup>	Best fit straight line			+2	% FS
CrAx	Cross axis <sup>(1)</sup>	Package alignment error	-5		+5	%
Cut_Off	MEMS cutoff frequency (-3 dB)		13.7	15.86	18.94	kHz
F <sub>0</sub>	MEMS resonant frequency		10.25	11.34	12.45	kHz
Gclip	g-cell clipping		951	1108	1231	g
T <sub>op</sub>	Operating temperature range		-40		+105	°C

1. Guaranteed by design, verified at characterization level

2. 14-bit data, equivalent to ±170 LSB on 12 bits

## 4.2 Electrical characteristics

$3.13\text{ V} \leq V_{DD} \leq 3.47\text{ V}$ ,  $-40^\circ\text{C} \leq T_{OP} \leq 105^\circ\text{C}$ , acceleration = 0 g, over lifetime, unless otherwise noted.

**Table 33. Electrical characteristics**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{DD}$	Supply voltage		-5%	3.3	+5%	V
Vreg			-5%	2.8	+5%	V
$I_{SS}$	Supply current	Single axis	3		6	mA
$I_{SD}$	Supply current	Dual axis	4		8	mA
<b>Offset cancellation<sup>(1)</sup></b>						
AVG	Averaging period		-5%	1024	+5%	ms
Off_CVU	Offset correction value per update		-1		+1	LSb
Off_DSPE	Default startup phase enable time	Time to guarantee the internal offset is removed	317	334	351 <sup>(2)</sup>	ms
Off_Fast	Fast offset cancellation		-5%	8000	+5%	LSb/s
Off_Slow	Slow offset cancellation		0.8	1	1.2	LSb/s
<b>Self-test</b>						
ST	Self-test output change	$V_{DD} = 3.30\text{ V}$ , $T = 25^\circ\text{C}$ , Frequency = 0 Hz		1632		LSb
ST_TOL	Self-test tolerance	Across temp, over life time	-15		15	%
ST_TON_ TOFF	Self-test turn-on/off time	Specification reached for a 400 Hz 3-pole filter			2	ms
<b>Noise</b>						
Nois_RMS	Output noise	RMS			+4	LSb
Nois_P2P	Output noise	peak-to-peak			+16	LSb
<b>Angular acceleration sensitivity<sup>(3)</sup></b>						
AAS	Angular acceleration sensitivity				$5 \cdot 10^{-6}$	$\text{g} \cdot \text{s}^2 / \text{rad}$
<b>SDO pin load<sup>(4)</sup></b>						
LOAD	Capacitive load drive				60	pF
<b>Oscillator frequency</b>						
$F_{osc}$	Oscillator frequency		-5%	16.384	+5%	MHz
<b>Power supply rejection ratio</b>						
PSRR	Power supply RR	1*Fsw, 2*Fsw, 3*Fsw, 4*Fsw, 5*Fsw, 6*Fsw			0.5	LSb/mV

Table 33. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
<b>Clipping</b>						
Dig_Clip	Digital output		-5%	120	+5%	g
<b>Low-pass filter</b>						
Cut_off	Cut-off frequency (400 Hz filter)		370	400	430	Hz

1. Offset cancellation can vary with oscillator frequency
2. Internal offset is removed in max. 345 ms; another 6 ms are needed for self-test calibration. During this phase, SPI will report ND flag if acceleration command being sent.
3. Based on simulation and characterization
4. Guaranteed by design

### 4.3 Digital blocks

Table 34. Digital range and levels

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Bit	ADC resolution				14	bit
ACC_RNG	Range for acceleration data		-8192		+8191	LSb
Out_Hi	Logic output high (SDO pin)	Max static current = 2 mA	$V_{DD}-0.6$		$V_{DD}$	V
Out_Low	Logic output low (SDO pin)	Max static current = 2 mA	0.0		0.6	V
In_Hi	Logic input high (all inputs)		2		$V_{DD}$	V
In_Low	Logic input low (all inputs)		0.0		1	V
$C_{IN1}$	Input capacitance at high impedance (SDO pin)				2	pF
$C_{IN2}$	Input capacitance at CS/SDI/SCK pin				10	pF
I_Pull_D	Internal pull-down current (SDI, SCK)	$V_{in} = V_{cc}$ to 0 V	10	27	50	$\mu$ A
I_Pull_U	Internal pull-up current (CS)	$V_{in} = V_{cc}$ to 0 V	10	27	50	$\mu$ A
UVT_VDD	Undervoltage threshold ( $V_{DD}$ )		2.7	2.9	3.1	V
UVT_VREG	Undervoltage threshold (VREG)		2.1	2.3	2.5	V
UV_DET1	Under/overvoltage detection time	VDD below threshold VREG below threshold	6 1.5	25 5	40 10.5	$\mu$ s $\mu$ s
Hard_Res	Hard reset threshold (VREG)		1.8	2.1	2.2	V
Res_t	Reset activation time	After SPI command	1.5		2	$\mu$ s
Rec_t	Reset recovery time	Reset to first SPI access			1	ms

**Table 35. 400 Hz digital filter**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Signal delay<sup>(1)</sup></b>						
	Overall signal delay		0.84	0.976	1.0	ms
<b>Sampling rate<sup>(1)</sup></b>						
	Interpolation output				256	kHz

1. Based on simulations

**Table 36. 800 Hz digital filter**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Signal delay<sup>(1)</sup></b>						
	Overall signal delay		0.4	0.507	0.6	ms
<b>Sampling rate<sup>(1)</sup></b>						
	Interpolation output				256	kHz

1. Based on simulations

**Table 37. 1600 Hz digital filter**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Signal delay<sup>(1)</sup></b>						
	Overall signal delay		0.19	0.273	0.32	ms
<b>Sampling rate<sup>(1)</sup></b>						
	Interpolation output				256	kHz

1. Based on simulations



## 4.4 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 38. Absolute maximum ratings**

Symbol	Ratings	Value	Unit
V <sub>DD</sub>	Supply voltage	-0.3 to 7.0 <sup>(1)</sup>	V
VREG		-03. to 3.0	V
SCK,SDI		-0.3 to V <sub>DD</sub>	V
A <sub>UNP</sub>	Mechanical shock with device unpowered	2000	g
h <sub>DROP</sub>	Drop shock survivability (concrete floor)	1.2	m
ESD	ESD protection HBM (low-voltage pins)	2	kV
	CDM	750	V
T <sub>STG</sub>	Storage temperature range	-55 to +150	°C
T <sub>j</sub>	Operating temperature range	-40 to +105	°C

1. Not for continued operation



This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.



This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

## 4.5 Factory calibration

The IC interface is factory calibrated for sensitivity (S<sub>0</sub>) and Zero-g level (Off\_Raw). The trimming values are stored inside the device in a non-volatile structure. When the device is turned on, the trimming parameters are downloaded into the registers to be employed during normal operation which allows the device to be used without further calibration.

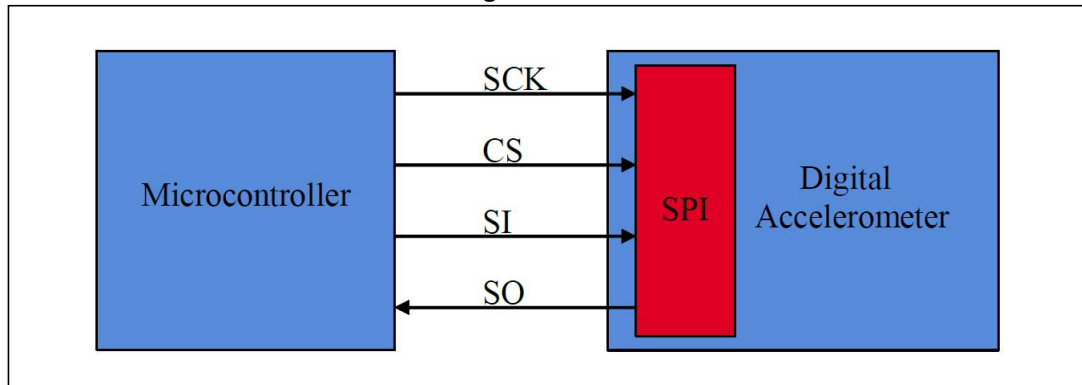
## 5 Interface description

The AIS1120SX / AIS2120SX provides a bi-directional 3.3 V SPI interface for communication with the MCU at a 32-bit data word size. Each transfer consists of two frames of 32 clocks per frame.

The sensor always operates in slave mode whereas the MCU provides the master function.

The interface consists of 4 ports as shown below.

Figure 22. SPI



Serial clock (SCK): input for master clock signal. This clock determines the speed of data transfer and all receiving and sending is done synchronous to this clock.

Chip Select (CS): CS activates the SPI interface. As long as CS is high, the IC does not accept the clock signal or data and the output SDO is in high impedance. Whenever CS is in a low logic state, data can be transferred from and to the microcontroller.

Serial Input (SDI): accelerometer data in is latched by the rising edge of SCL (see [Figure 23: SPI timings](#)).

Serial Output (SDO): accelerometer data out is set by the falling edge of SCL (see [Figure 23: SPI timings](#)).

### 5.1 32-bit communication protocol

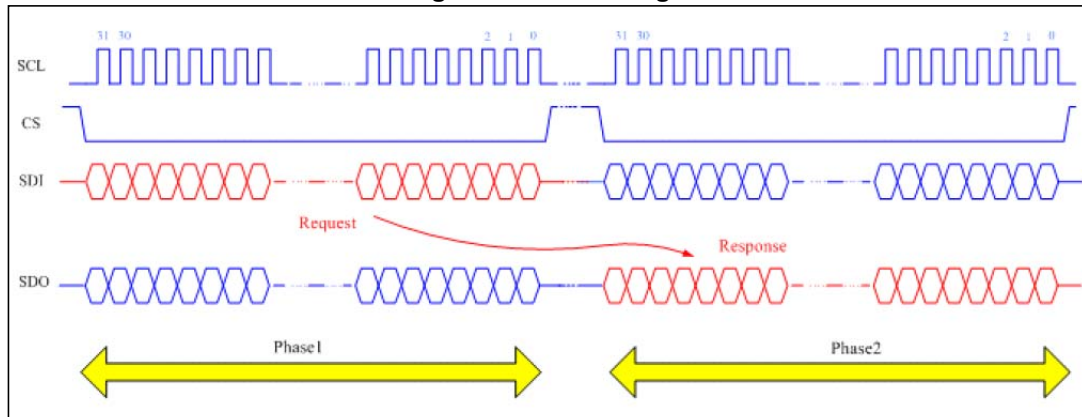
The communication between slave and master is transmitted by 32-bit data word, MSB first.

An off-frame protocol is used meaning that each transfer is completed through a sequence of 2 phases.

The answer of a given request is sent within the very next frame.

The acceleration data for the x-axis, y-axis channel will be frozen at the rising edge of CS of the Request and submitted during the Response (see [Figure 23](#)).

Figure 23. SPI timings



CS is the Chip Select and it is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end of a phase. SCL is the Serial port Clock and it is controlled by the SPI master. It is stopped high when CS is high (no transmission). SDI is Serial Data Input and SDO is Serial Data Output. SDI is captured at the rising edge of SCL and SDO is driven at the falling edge of SCL.

The SPI instructions used can be subdivided into two classes, acceleration and non-acceleration commands.

### 5.1.1 Acceleration commands

These commands are used to request sensor data for channel X or Y. The acceleration data is given in 14-bit format (bit 25-12 of SDO data frame). The MSB (D13) represents the sign bit and the negative value is in two's complementary format.

The following table shows a few examples of full range and 0 g offset:

Table 39. Acceleration data example

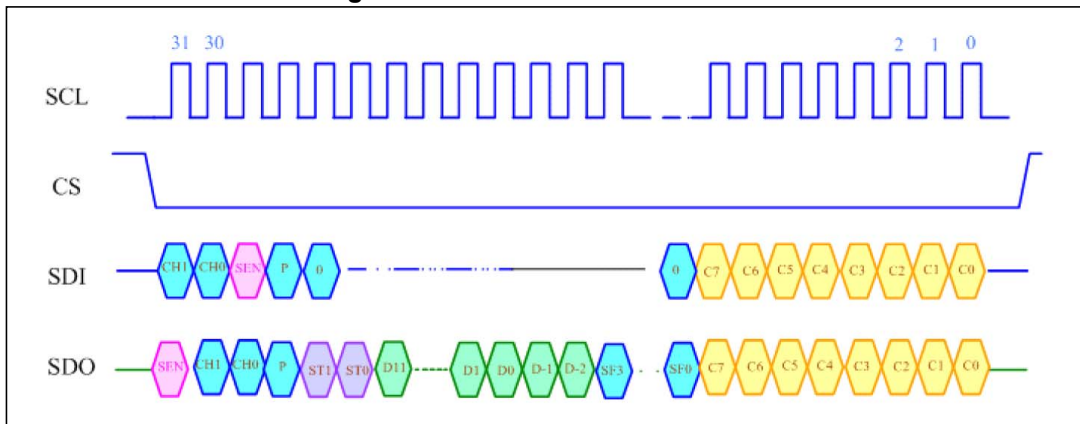
Accel [g]	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
120.4	0	1	1	1	1	1	1	1	1	1	1	1	1	1
-120.5	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0.015	0	0	0	0	0	0	0	0	0	0	0	0	0	1
-0.015	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Each 32-bit frame can request one of two channels (X or Y), see definition of bits CH1:CH0.

- 00 x data
- 01 y data

The format of the acceleration commands is shown below.

**Figure 24. Acceleration commands**



The function of the individual bits of SDI and SDO is shown in [Table 40](#) and [Table 41](#).

**Table 40. Acceleration commands function of SDI bits**

Name	Bit position	Description	Definition
CH1:CH0	[31:30]	Channel select	Sensor channel source for data: 00: X-data (CH1) 01: Y -data (CH2) 10: CH3 11: CH4
SEN	29	SEN bit	Identifies sensor data request: 1: sensor data 0: non-sensor data
P	28	Parity bit	Odd parity bit, cover bit 31-8
Not used	[27:8]	N/A	Always 0
C7:C0	[7:0]	CRC	CRC bits for SDI

**Table 41. Acceleration commands function of SDO bits**

Name	Bit position	Description	Definition
SEN	31	SEN bit	Identifies sensor data request: 1: sensor data 0: non-sensor data
CH1-CH0	[30:29]	Channel select	Sensor channel source for data: 00: X-data (CH1) 01: Y -data (CH2) 10: CH3 11: CH4
P	28	Parity bit	Odd parity bit, cover bit 31-8

**Table 41. Acceleration commands function of SDO bits (continued)**

Name	Bit position	Description	Definition
ST1:ST0	[27:26]	Status	Type of data: 00: Initialization 01: Normal mode 10: Self-test mode 11: Error data
D13:D0	[25:12]	Data	Sensor data / self-test data (14 bit)
SF3-SF0	[11:8]	Status flag bits	0000: No error 0001: EEPROM Error (EE) 0010: SPI Error (SE) 0011: Request Error (RE) 0100: Condition Not Correct (CNC) 0101: No Data available (ND) 0110: Hardware Error (HE) 1000: ADC saturation error (AS) 1111: In test mode (TE)
C7:C0	[7:0]	CRC	CRC error bits for SDO

Error codes are to be interpreted as follows:

**EEPROM Error (EE):** any error related to internal EEPROM e.g. mismatch of internal CRC.

**SPI Error (SE):** any violation of SPI format e.g. incorrect number of clocks during the frame, or parity mismatch of SDI, or CRC mismatch of SDI.

**Request Error (RE):** set when unexpected or invalid command is received by sensor, locked registers are read or written during any undefined state of sensor.

**Condition Not Correct (CNC):** set when data for undefined channel (for single axis sensor), CH3 or CH4 are requested.

**No Data available (ND):** set when data is requested during power-up sequence (cap-loss/charge pump/fast offset cancel).

**X channel Hardware Error (X\_HE):** Set when there is cap-loss error, charge pump error, VDD\_low, VREG\_low or X offset cancel saturate (after EOI) occurs.

**Y channel Hardware Error (Y\_HE):** Set when there is cap loss error, charge pump error, VDD\_low, VREG\_low or Y offset cancel saturate (after EOI) occurs.

**Test mode (TE):** Set when the part is in test mode.

**Priority of error codes:** EE (Highest) -> SE -> RE -> CNC -> ND -> HE -> TE (lowest)

**Table 42. Error codes**

ST1:ST0	SF flags
11	EE = 0001 NVM CRC error
11	SE = 0010 frame CRC error
11	RE = 0011 request error (register 03, bit4 shows this error also)

**Table 42. Error codes (continued)**

11	CNC = 0100 condition not correct error
11	ND = 0101 no data error
11	HE = 0110 (cap loss error + charge pump error + VDD undervoltage + VREG undervoltage + VDD overvoltage + VREG overvoltage + SLOW offset max)
00	AS = 1000 (ADC internal > 160G)

*Table 43* provides some examples of SDO bit sequence interpretation.

**Table 43. SDO bit examples**

31	30	29	28	27	26	[25:12]	[11:8]	[7:0]	Definition
SEN	CH1	CH0	P	ST1	ST2	D11:D2/error	SF3:SF0	CRC	Device status
1	0	0		0	0	X, Init no ST	0101	CRC	INIT, self test off
1	0	1		0	0	Y, Init no ST	0101	CRC	INIT, self test off
1	0	0		0	1	X data	0000	CRC	Normal mode
1	0	1		0	1	Y data	0000	CRC	Normal mode
1	0	0		1	0	X data	0000	CRC	Self-test mode
1	0	1		1	0	Y data	0000	CRC	Self-test mode
1	0	0		1	1	X data	Status flag	CRC	Error response
1	0	1		1	1	Y data	Status flag	CRC	Error response

**Notes:**

1. Once the device finishes fast offset cancellation (and self-test calibration), it automatically enters into the programming phase (ST1:ST0 status "10") until the EOI command has been sent. During this phase, if there is not any self-test initialization command from SPI, 0 g in self-test phase on both channels could be read from the acceleration commands.

2. When starting channel X self-test:

a. Channel X acceleration command will read channel X self-test value

b. Channel Y acceleration command will read temperature sensor value for self-test temperature compensation algorithm.

3. When starting channel Y self-test:

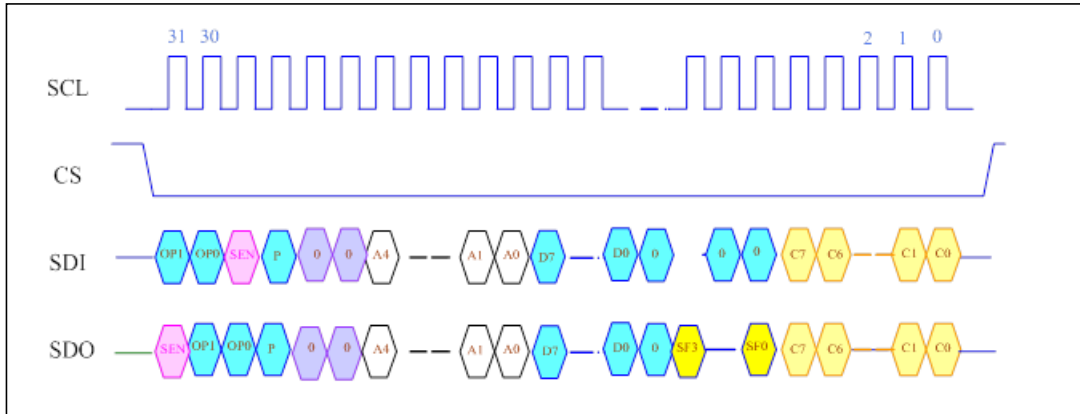
c. Channel X acceleration command will read temperature sensor value for self-test temperature compensation algorithm.

d. Channel Y acceleration command will read channel Y self-test value

### 5.1.2 Non-acceleration commands

These commands are used to write/read control and status registers.

**Figure 25. Non-acceleration commands**



The function of the individual bits of SDI and SDO are shown in [Table 44](#) and [Table 45](#).

**Table 44. Non-acceleration command function of SDI bits**

Name	Bit position	Description	Definition
OP1:OP0	[31:30]	Opcode	Operation type: 00: N/A 01: Write 10: N/A 11: Read
SEN	29	SEN bit	Sensor data request type: 1: sensor data 0: non-sensor data
P	28	Parity bit	Odd parity bit, cover bit 31-8
Not used	[27:26]	N/A	Always 0
A4:A0	[25:21]	Address	Register address for R/W operations
D7:D0	[20:13]	Data	Data for write
Not used	[12:8]	N/A	Always 0
C7:C0	[7:0]	CRC	CRC bits for SDI

Table 45. Non-acceleration commands function of SDO bits

Name	Bit position	Description	Definition
SEN	31	SEN bit	Sensor data request type: 1: sensor data 0: non-sensor data
OP1:OP0	[30:29]	Opcode	Copied from SDI request if accepted 00: N/A 01: Write 10: N/A 11: Read
P	28	Parity bit	Odd parity bit, cover bit 31-8
Not used	[27:26]	N/A	Always 0
A4:A0	25:21	Address	Register address for R/W operations
D7:D0	20:13	Data	Read data / error code
Not used	12	N/A	Always 0
SF3:SF0	[11:8]	Status flag bits	0000: No error 0001: EEPROM Error (EE) 0010: SPI Error (SE) 0011: Request Error (RE) 1111: In test mode (TE)
C7:C0	[7:0]	CRC	CRC bits for SDO

Error codes are to be interpreted as follows:

**EEPROM Error (EE):** any error related to internal EEPROM e.g. mismatch of internal CRC.

**SPI Error (SE):** any violation of SPI format e.g. incorrect number of clocks during the frame, parity mismatch of SDI, or CRC mismatch of SDI.

**Request Error (RE):** set when unexpected or invalid command is received by sensor, locked registers are read or written during any undefined state of sensor.

**Test mode (TE):** set when the part is in test mode

**Priority of error codes:** EE (Highest) -> SE -> RE -> TE (lowest)

### 5.1.3 SPI CRC polynomial

To check the integrity of the sensor signals (SO) and commands (SI) to the sensor, an 8-bit CRC (Cyclic Redundancy Check, Baicheva C2) is used.

The applied polynomial is:  $X^8+X^5+X^3+X^2+X+1 = 0x97$

with:

HD = 4 for 32-bit data

Initial value = 0000 0000b

Target value = 0x00



## 5.2 32-bit SPI bit information

**Table 46. 32-bit SPI command: bits from 31 to 16**

Acceleration																
BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SDI	CH1	CH0	SEN	P	0	0	0	0	0	0	0	0	0	0	0	0
SDO	SEN	CH1	CH0	P	ST1	ST0	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4
Non-acceleration																
BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SDI	OP1	OP0	SEN	P	0	0	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3
SDO	SEN	OP1	OP0	P	0	0	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3

**Table 47. 32-bit SPI command: bits from 15 to 0**

Acceleration																
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDI	0	0	0	0	0	0	0	0	C7	C6	C5	C4	C3	C2	C1	C0
SDO	D3	D2	D1	D0	SF3	SF2	SF1	SF0	C7	C6	C5	C4	C3	C2	C1	C0
Non-acceleration																
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDI	D2	D1	D0	0	0	0	0	0	C7	C6	C5	C4	C3	C2	C1	C0
SDO	D2	D1	D0	0	SF3	SF2	SF1	SF0	C7	C6	C5	C4	C3	C2	C1	C0

**Table 48. Bit decoding**

	CH[1:0]	OP[1:0]	SEN	ST[1:0]	SF[3:0]
000	X Data	N/A	Non-sensor	Initialization	No error
001	Y Data	Write	Sensor	Normal mode	EEPROM error
010	N/A	N/A		Self-test mode	SPI error (SE)
011	N/A	Read		Error data	Request error (RE)
100					Condition not correct (CNC)
101					No data (ND)
110					Hardware error (HE)
1000					ADC saturation (AS)
1111					In test mode (TE)

### 5.3 Timing parameters

Figure 26. SPI timing parameters

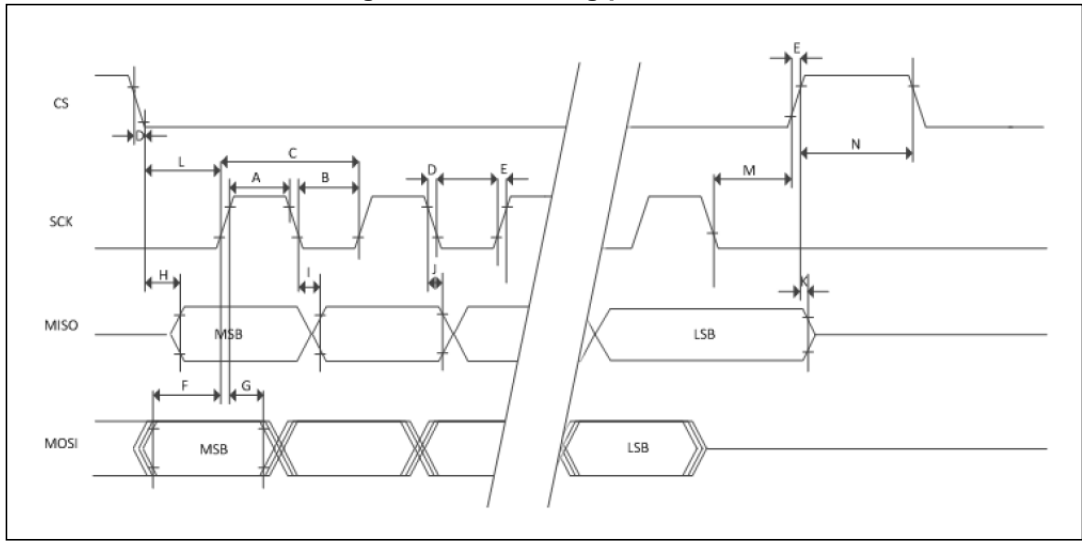


Figure 27. Additional SPI timing parameters

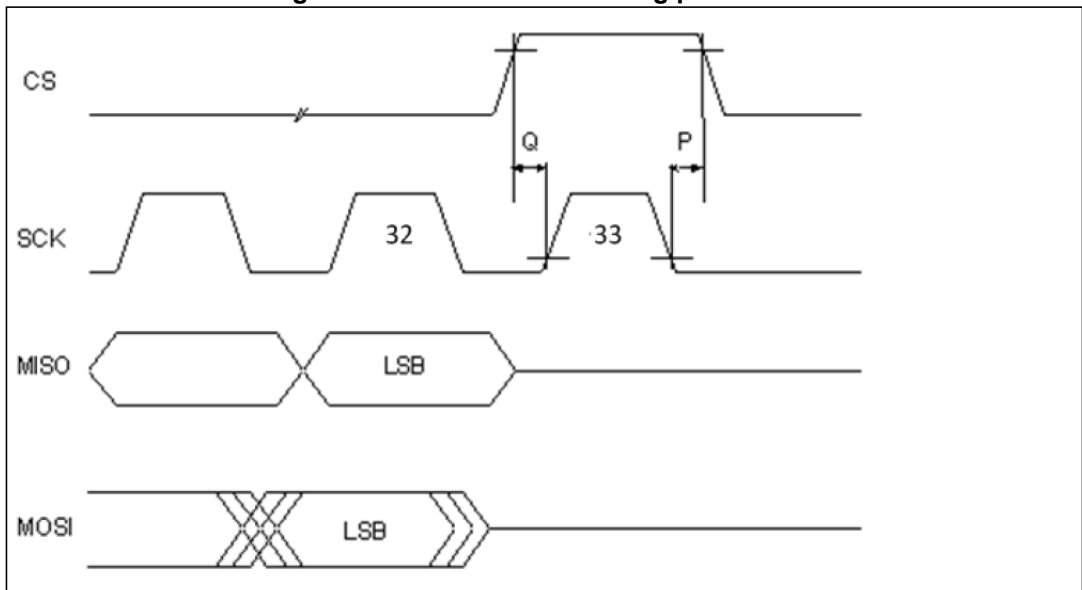


Table 49. SPI timing table

No.	Parameter	Symbol	Min.	Max.	Unit
-	SPI operating frequency	f <sub>OP</sub>	-	5	MHz
A	Clock (SCK) high time	t <sub>WSCKh</sub>	49	-	ns
B	Clock (SCK) low time	t <sub>WSCKl</sub>	95	-	ns
C	SCK period	t <sub>SCK</sub>	200	-	ns
D	Clock (SCK) and CS fall time	t <sub>f</sub>	5.5	50	ns
E	Clock (SCK) and CS rise time	t <sub>r</sub>	5.5	50	ns
F	Data input (MOSI) setup time	t <sub>su</sub>	10	-	ns
G	Data input (MOSI) hold time	t <sub>hi</sub>	10	-	ns
H	Data output (MISO) access time	t <sub>a</sub>	-	60	ns
I	Data output (MISO) valid after SCK	t <sub>v</sub>	-	60	ns
K	Data output (MISO) disable time	t <sub>dis</sub>	-	100	ns
L	Enable (SS) lead time	t <sub>lead</sub>	10	-	ns
M	Enable (SS) lag time	t <sub>lag</sub>	25	-	ns
N	Sequential transfer delay	t <sub>td</sub>	1.9	-	μs
P	Clock enable time	t <sub>CLE</sub>	10	-	ns
Q	Clock disable time	t <sub>CLD</sub>	10	-	ns

Timing reference: 0.2 Vs - 0.8 Vs (Vs = V<sub>VDD</sub>-D<sub>GND</sub>)

Explanation:

- c) Q: SCK stable (low or high) before CS falling
- d) P: SCK stable (low or high) after CS rising

## 5.4 Error management

The device replies with an error response if one of the following errors has occurred:

**Table 50. Error flags and description**

Flags	Description
REG_CTRL_0_WR_ERR	'1': when there is a request error writing the REG_CTRL_0(Address=0x00) register
LOSSCAP	'1': when there a loss of cap on VREG PAD (set only during power-up)
END_OF_PWRUP	'1': when power-up sequencer has finished initialization (completed charge pump test, cap-loss test, fast offset cancel);
RST_ACTIVE	'1': when soft reset is issued
SPI_ERR	'1': when SPI error occurs
EEPROM_ERR	'1': when EEPROM error (e.g mismatch in CRC) occurs during power-up
OFF_CANC_CHY_ERR	'1': when offset cancellation error for CHY occur
OFF_CANC_CHX_ERR	'1': when offset cancellation error for CHX occurs
REG_CONFIG_WR_ERR	'1':when there is a request error writing the REG_CONFIG (Address=0x012) register
REG_CTRL_1_WR_ERR	'1': when there is a request error writing the REG_CTRL_1 (Address=0x01) register
A2D_SAT_CHY	'1': when A2D saturates for CHY
A2D_SAT_CHX	'1': when A2D saturates for CHX
CHARGE_PUMP_ERR	'1': when charge pump test fails at power-up
VREG_LOW_ERR	'1': when VREG falls below its LOW threshold
VREG_HIGH_ERR	'1': when VREG goes above its HIGH threshold
VDD_LOW_ERR	'1': when VDD falls below its LOW threshold
VDD_HIGH_ERR	'1': when VDD goes above its HIGH threshold

## 6 Recommendations for operation

1. It's recommended to power up VDD first, then provide SPI logic signals. This is recommended to avoid the potential of powering the device via the SPI pins when VDD is not in the specified operating range.
2. Recommended VDD ramp rate > 1 V/ms
3. It is recommended that all flags be reconfirmed with soft POR after power-up.

# 7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

## 7.1 SOIC8 package information

Figure 28. SOIC8 package outline

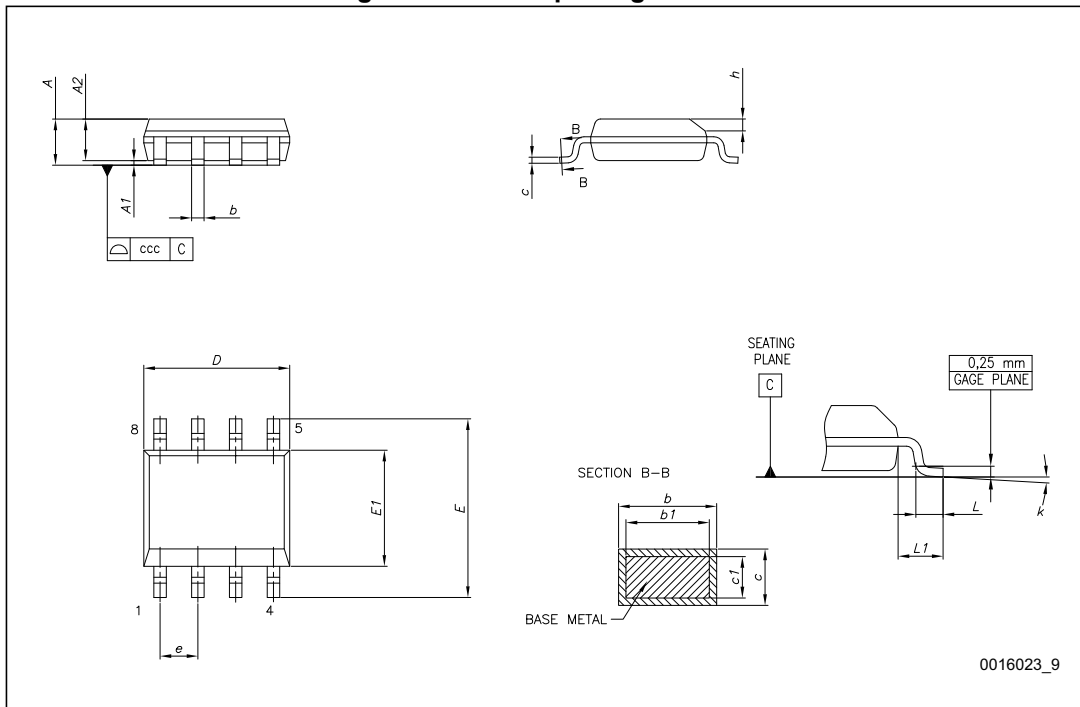


Table 51. SOIC8 package mechanical data

Ref.	Databook (mm)		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
c	0.10		0.25
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
L2		0.25	
k	0		8°
ccc			0.10

Figure 29. SOIC8 package marking

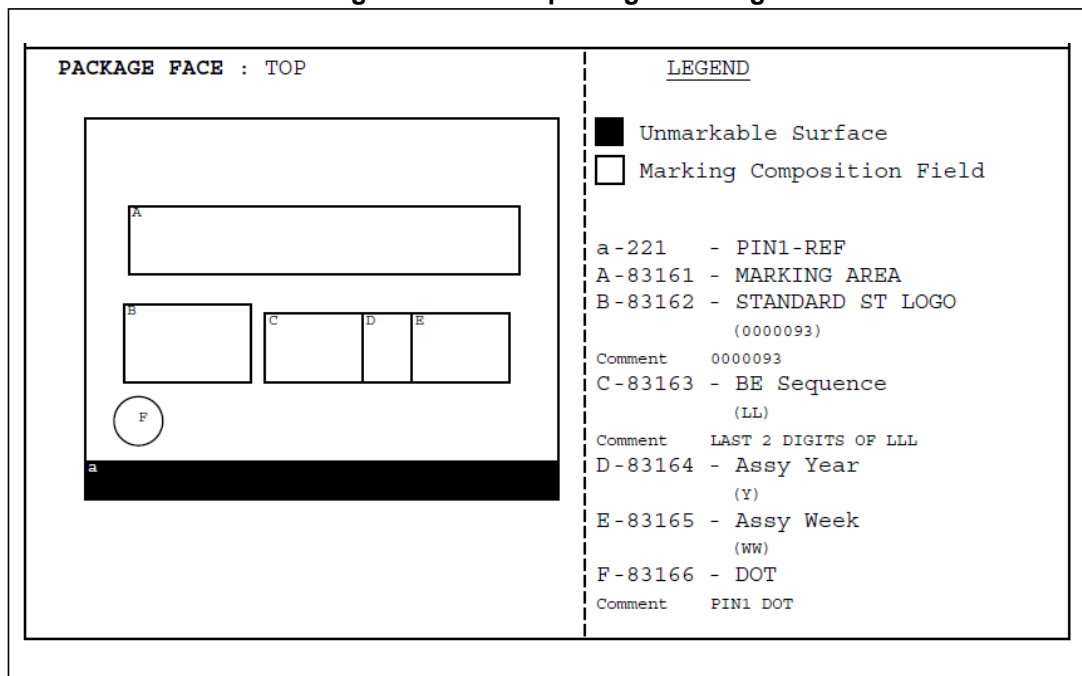
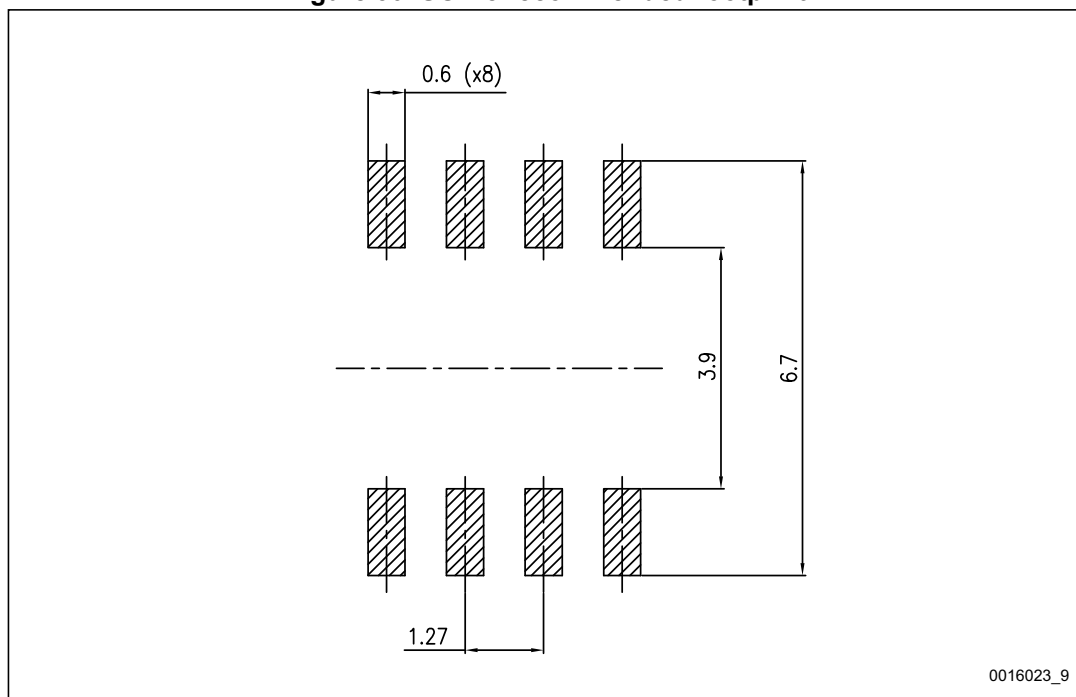


Figure 30. SOIC8 recommended footprint





## 8 Revision history

**Table 52. Revision history**

Date	Revision	Changes
18-Sep-2015	1	Initial release
19-Aug-2016	2	Updated <a href="#">Section 5.1.3: SPI CRC polynomial</a>
20-Jan-2017	3	Document status promoted to production data Updated SDO pin load in <a href="#">Table 33: Electrical characteristics</a> Updated $t_{SCK}$ and $t_v$ in <a href="#">Table 49: SPI timing table</a>

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