# P-Channel Enhancement-Mode MOSFET Transistors

## Product Summary

| Part Number | $V_{(BR)DSS}$ Min (V) | $V_{GS(th)}$ (V) | $r_{DS(on)}$ Max (Ω) | $I_{D(on)}$ Min (mA) | $C_{rss}$ Max (pF) | $t_{ON}$ Typ (ns) |
|---|---|---|---|---|---|---|
| 3N163 | –40 | –2 to –5 | 250 | –5 | 0.7 | 18 |
| 3N164 | –30 | –2 to –5 | 300 | –3 | 0.7 | 18 |

## Features

- Ultra-Low Input Leakage: 0.02 pA Typ.
- High Gate Breakdown Voltage: ±125 V
- Normally Off

## Benefits

- High Input Impedance Isolation
- Minimize Handling ESD Problems
- High Off Isolation without Power

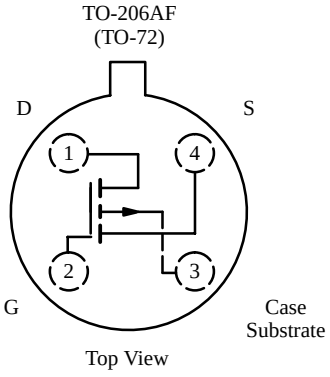
## Applications

- Ultra-High Input Impedance Amplifier
- Smoke Detectors
- Electrometers
- Analog Switching
- Digital Switching

## Description

The 3N163/164 are lateral p-channel MOSFETs designed for analog switch and preamplifier applications where high speed and low parasitic capacitances are required.

The hermetic TO-206AF package is compatible with military processing per military standards (see Military information).




## Absolute Maximum Ratings ($T_A$ = 25°C Unless Otherwise Noted)

Drain-Source Voltage (3N163) . . . . . –40 V
(3N164) . . . . . –30 V

Gate-Source Voltage . . . . . ±30 V

Continuous Drain Current . . . . . –50 mA

Lead Temperature ($^1/_{16}$" from case for 10 seconds) . . . . . 300°C

Storage Temperature . . . . . –65 to 200°C

Operating Junction Temperature . . . . . –55 to 150°C

Power Dissipation[a] . . . . . 375 mW

Notes:
a. Derate 3 mW/°C above 25°C

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70228.

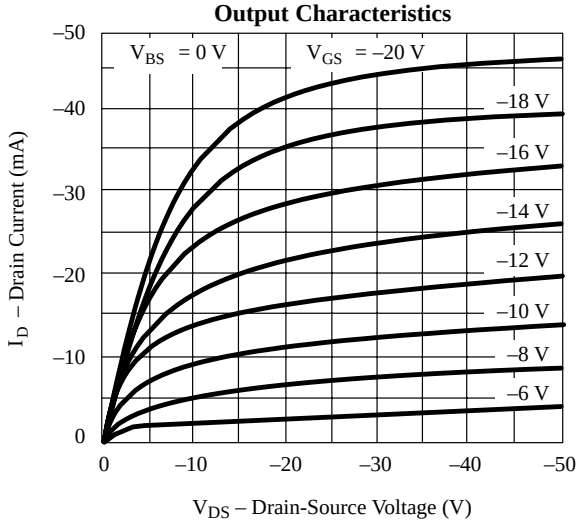
## Specifications[a]

| Parameter | Symbol | Test Conditions | Typ[b] | Limits 3N163 Min | Limits 3N163 Max | Limits 3N164 Min | Limits 3N164 Max | Unit |
|---|---|---|---|---|---|---|---|---|
| **Static** | | | | | | | | |
| Drain-Source Breakdown Voltage | $V_{(BR)DSS}$ | $I_D$ = –10 µA, $V_{DS}$ = 0 V | –70 | –40 | | –30 | | V |
| Source-Drain Breakdown Voltage | $V_{(BR)SDS}$ | $I_S$ = –10 µA, $V_{GD}$ = $V_{BD}$ = 0 V | –70 | –40 | | –30 | | V |
| Gate-Threshold Voltage | $V_{GS(th)}$ | $I_D$ = –10 µA, $V_{GS}$ = $V_{DS}$ | –2.5 | –2 | –5 | –2 | –5 | V |
| Gate-Source Voltage | $V_{GS}$ | $I_D$ = –0.5 mA, $V_{DS}$ = –15 V | –3.5 | –3 | –6.5 | –2.5 | –6.5 | V |
| Gate-Body Leakage | $I_{GSS}$ | $V_{GS}$ = –40 V, $V_{DS}$ = 0 V | <–1 | | –10 | | | pA |
| | | $T_A$ = 125°C[d] | –1 | | | | | pA |
| | | $V_{GS}$ = –30 V, $V_{DS}$ = 0 V | <–1 | | | | –10 | pA |
| | | $T_A$ = 125°C[d] | –1 | | | | | pA |
| Zero-Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = –15 V, $V_{GS}$ = 0 V | –8 | | –200 | | –400 | pA |
| | | $T_A$ = 125°C[d] | –20 | | | | | nA |
| Zero-Gate Voltage Source Current | $I_{SDS}$ | $V_{GD}$ = $V_{BD}$ = 0 V, $V_{SD}$ = –20 V | –10 | | –400 | | –800 | pA |
| | | $T_A$ = 125°C[d] | –25 | | | | | nA |
| On-State Drain Current[c] | $I_{D(on)}$ | $V_{DS}$ = –15 V, $V_{GS}$ = –10 V | –10 | –5 | –30 | –3 | –30 | mA |
| Drain-Source On-Resistance | $r_{DS(on)}$ | $V_{GS}$ = –20 V, $I_D$ = –100 µA | 180 | | 250 | | 300 | Ω |
| | | $T_A$ = 125°C[d] | 270 | | | | | Ω |
| **Dynamic** | | | | | | | | |
| Forward Transconductance[c] | $g_{fs}$ | $V_{DS}$ = –15 V, $I_D$ = –10 mA f = 1 kHz | 2.7 | 2 | 4 | 1 | 4 | mS |
| Common-Source Output Conductance[c] | $g_{os}$ | $V_{DS}$ = –15 V, $I_D$ = –10 mA f = 1 kHz | 150 | | 250 | | 250 | µS |
| Input Capacitance | $C_{iss}$ | $V_{DS}$ = –15 V, $I_D$ = –10 mA f = 1 MHz | 2.4 | | 3.5 | | 3.5 | pF |
| Output Capacitance | $C_{oss}$ | $V_{DS}$ = –15 V, $I_D$ = –10 mA f = 1 MHz | 2.5 | | 3 | | 3 | pF |
| Reverse Transfer Capacitance | $C_{rss}$ | $V_{DS}$ = –15 V, $I_D$ = –10 mA f = 1 MHz | 0.5 | | 0.7 | | 0.7 | pF |
| **Switching[e]** | | | | | | | | |
| Turn-On Time | $t_{d(on)}$ | $V_{DD}$ = –15 V, $R_L$ = 1500 Ω $I_D$ ≅ –10 mA, $V_{GEN}$ = –12 V $R_G$ = 50 Ω | 5 | | 12 | | 12 | ns |
| | $t_r$ | $V_{DD}$ = –15 V, $R_L$ = 1500 Ω $I_D$ ≅ –10 mA, $V_{GEN}$ = –12 V $R_G$ = 50 Ω | 13 | | 24 | | 24 | ns |
| Turn-Off Time | $t_{d(off)}$ | $V_{DD}$ = –15 V, $R_L$ = 1500 Ω $I_D$ ≅ –10 mA, $V_{GEN}$ = –12 V $R_G$ = 50 Ω | 25 | | 50 | | 50 | ns |

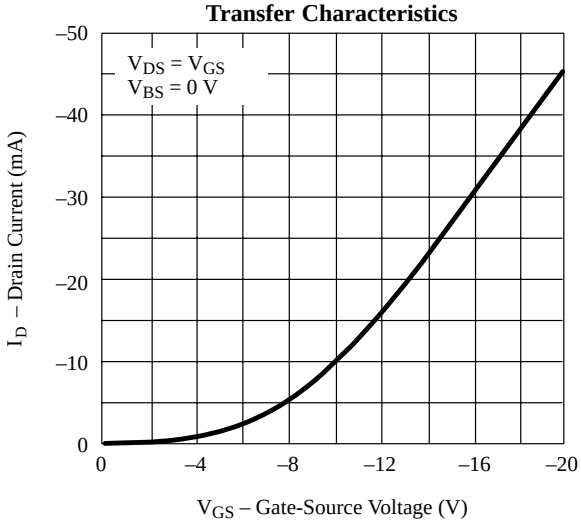
Notes:
a. $T_A$ = 25°C unless otherwise noted. MRA
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. Pulse test: PW ≤ 300 µs duty cycle ≤ 3%.
d. This parameter not registered with JEDEC.
e. Switching time is essentially independent of operating temperature.

# Typical Characteristics

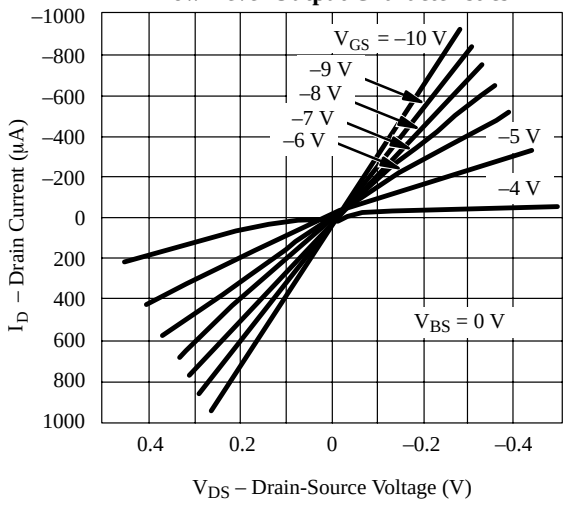
**Output Characteristics**



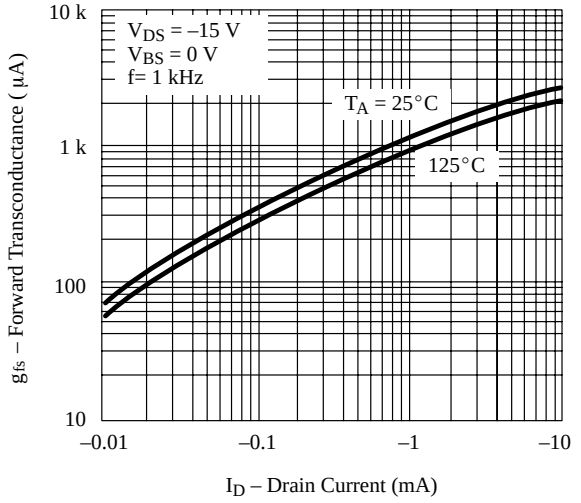

**Transfer Characteristics**



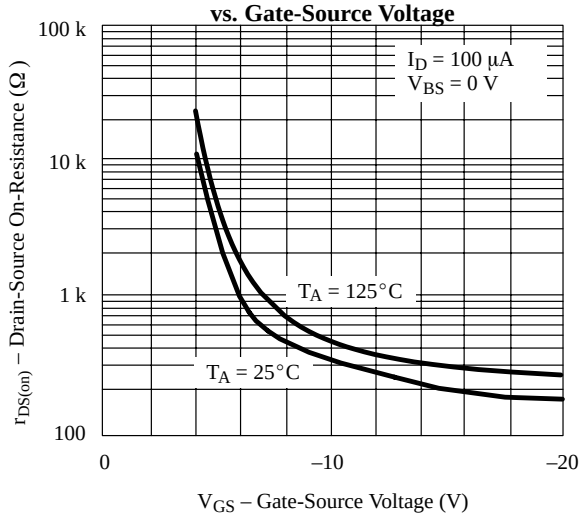

**Low-Level Output Characteristics**



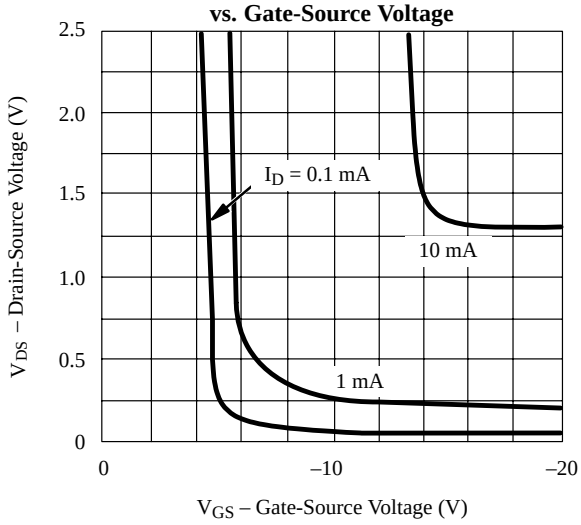

**Common-Source Forward Transconductance vs. Drain Current**




**Drain-Source On-Resistance vs. Gate-Source Voltage**

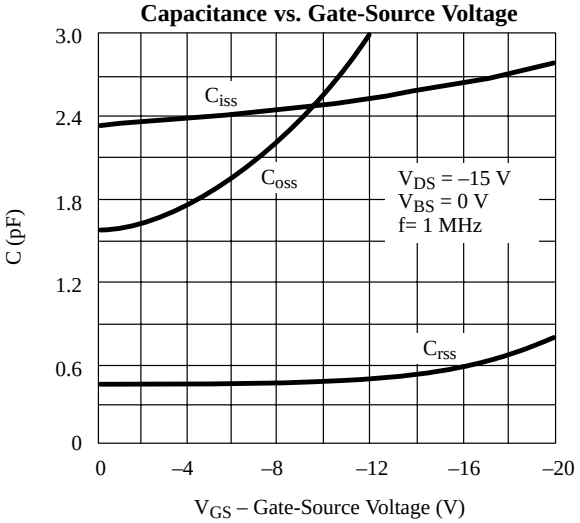



**Low-Level Drain-Source On-Voltage vs. Gate-Source Voltage**

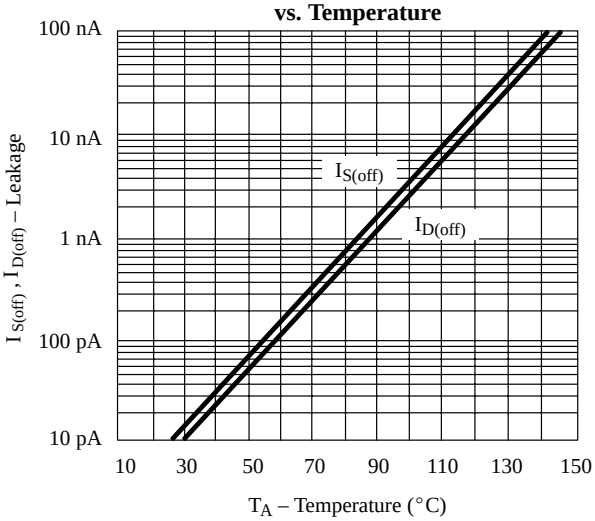


## Typical Characteristics (Cont'd)

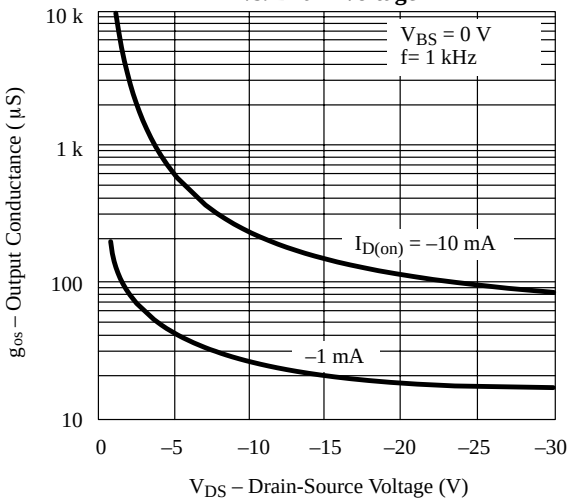
**Capacitance vs. Gate-Source Voltage**



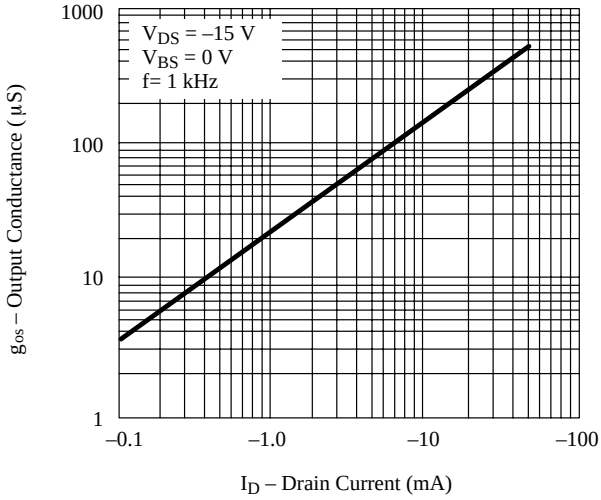

**Drain-Source Leakage Current vs. Temperature**




**Common-Source Output Conductance vs. Drain Voltage**




**Common-Source Output Conductance vs. Drain Current**




## Switching Time Test Circuit