uP7561Q

Two-Channel Input Power Management Controller

General Description

The uP7561Q is a 2-channel input power management controller specifically designed for dynamic input power switching application and under voltage boot application. It supports wide input voltage range from 2.7V~13.2V. The power for internal logic circuit is supported from input voltage by integrated charge pump circuit.

The uP7561Q has two embedded drivers to drive the external power MOSFET, and it also provides two integrated MOSFETs as internal power paths for application flexibility. The VIN1 internal power path supports maximum 200mA continuous current capability, and the VIN2 internal power path supports maximum 1A continuous current capability.

The output voltage of uP7651Q is switched between VIN1 and VIN2 according to SWITCH# logic input. The STEER logic input controls both DRV1 & DRV2 to turn on at the same time if the under voltage boot condition is detected.

The uP7561Q provides adjustable soft-start function to prevent the surge current during power up. The uP7561Q is available in WQFN3x3-20L package.

Features

- **VIN Operating Range: 2.7V to 13.2V**
- **Integrated Charge Pump for VCC, DRV1 and DRV2**
- **Current Capability for Internal Power Path**
  - **Maximum 200mA Continuous Current for VIN1**
  - **Maximum 1A Continuous Current for VIN2**
- **50mV Voltage Drop for Internal Path Application**
- **Two Embedded Driver Outputs for External Power MOSFET Control**
- **Adjustable Soft-Start**
- **RoHS Compliant and Halogen Free**

Applications

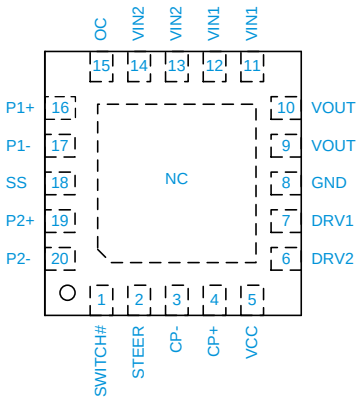
- **Desktop Graphic Card**

Ordering Information

Order Number	Package Type	Top Marking
uP7561QQKF	WQFN3x3-20L	uP7561Q

Note:
(1) Please check the sample/production availability with uPI representatives.
(2) uPI products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

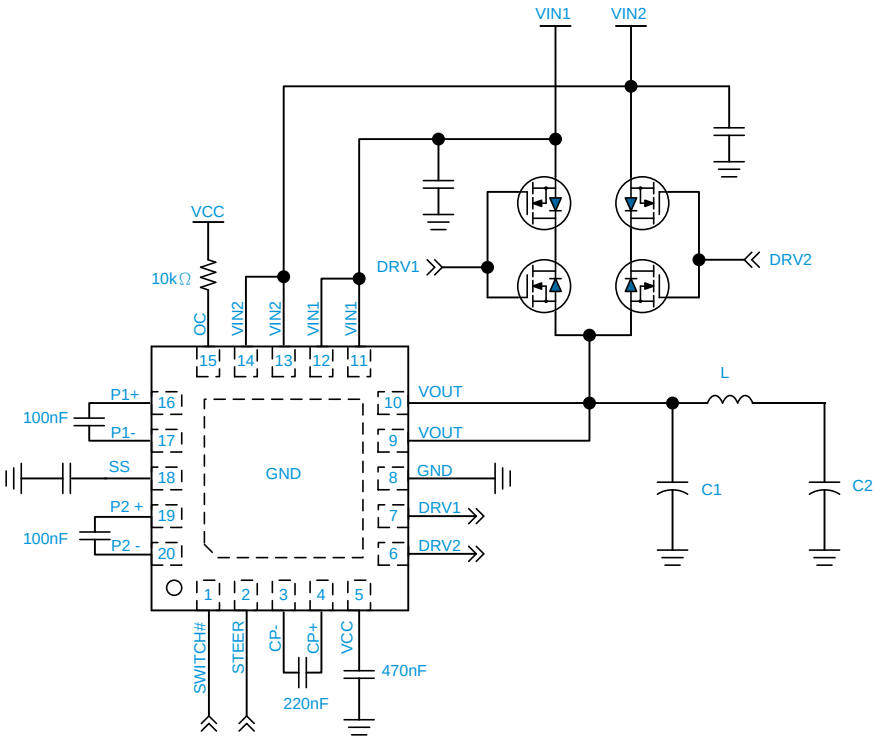
Pin Configuration



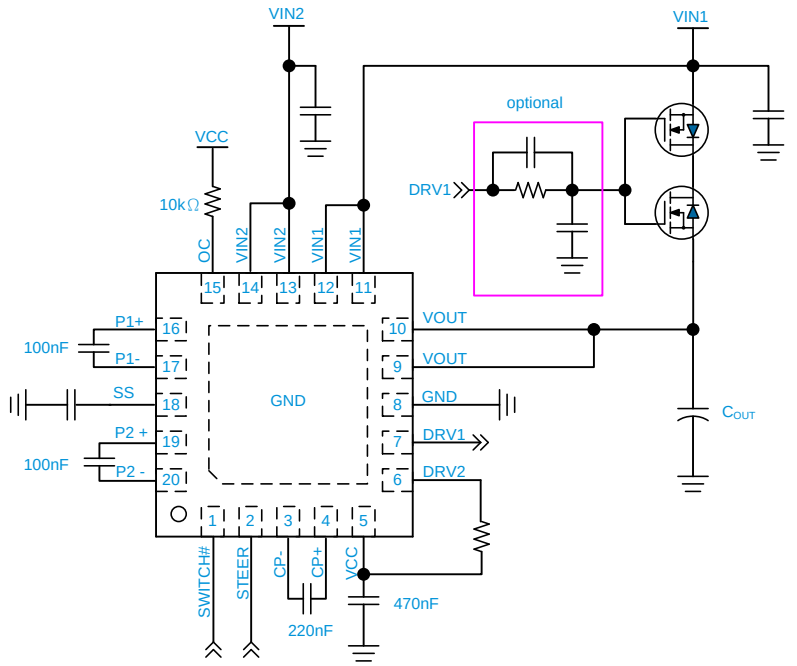
uP7561Q

Typical Application Circuit

Fast Switching Application



Slow Switching Application

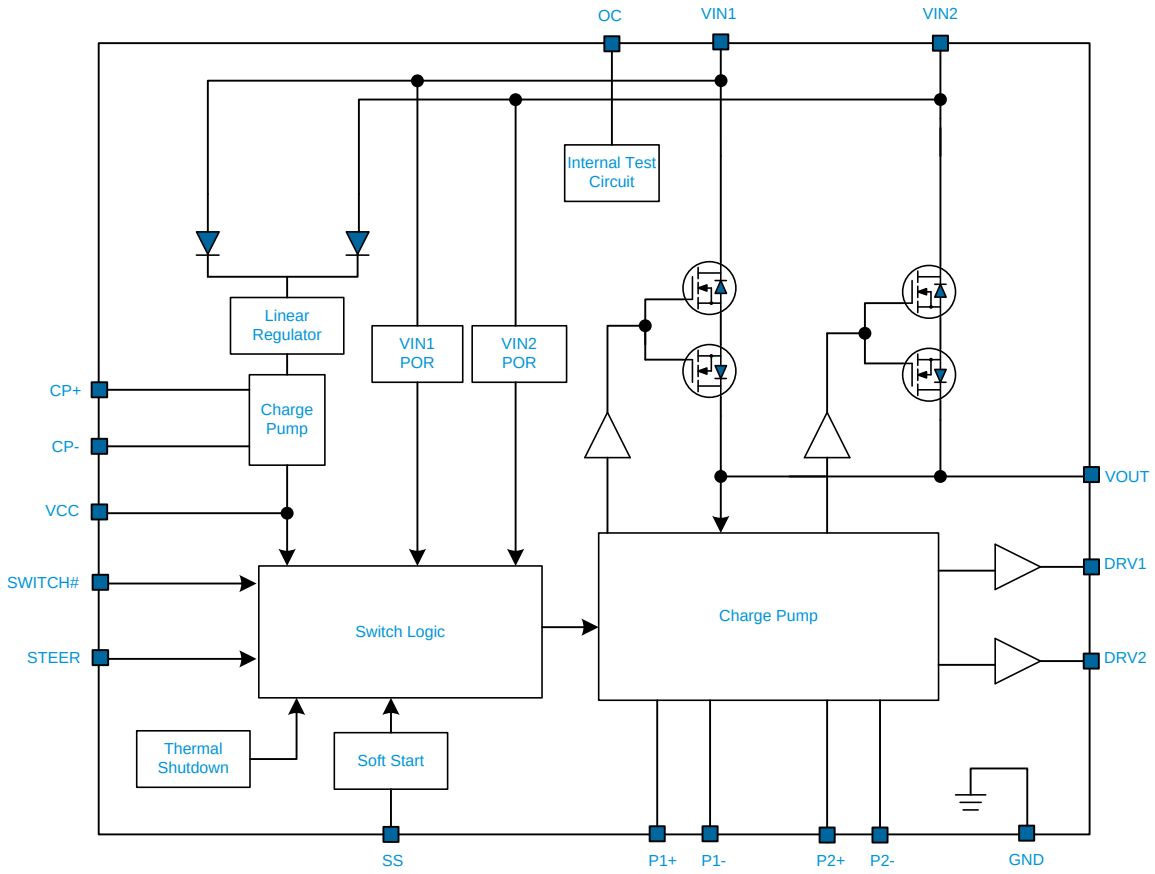


Functional Pin Description

Pin No.	Name	Pin Function
1	SWITCH#	**SWITCH# Logic Input.** The logic input of SWITCH# controls the dynamic power switch. This pin is an active low logic input. Refer to Table 1 for logic input truth table.
2	STEER	**STEER Logic Input.** The logic input of STEER controls the DRV1 and DRV2 to turn on simultaneously when the under voltage boot condition is detected.
3	CP-	**Charge Pump Negative Node.** Connect a 220nF capacitor from this pin to CP+.
4	CP+	**Charge Pump Positive Node.** Connect a 220nF capacitor from this pin to CP-.
5	VCC	**VCC Output Pin.** Output of charge pump circuit. Connect a 470nF capacitor from this pin to GND.
6	DRV2	**Driver Output for VIN2.** Connect this pin to the gate of external N-MOSFET. Connect this pin to VCC with 1kΩ resistor to disable VIN2 external path. When VIN2 external path is disabled, the VIN2 internal power path is active.
7	DRV1	**Driver Output for VIN1.** Connect this pin to the gate of external N-MOSFET. Connect this pin to VCC with 1kΩ resistor to disable VIN1 external path. When VIN1 external path is disabled, the VIN1 internal power path is active.
8	GND	**Ground.**
9,10	VOUT	**Output Voltage.** These pins are the output of the power device.
11,12	VIN1	**Supply Input 1.** These pins are the input of the power device.
13,14	VIN2	**Supply Input 2.** These pins are the input of the power device.
15	OC	**Reserved.** For internal test purpose. Connect this pin to VCC with 10kΩ.
16	P1+	**Charge Pump Positive Node.** Connect a100nF capacitor from this pin to P1-.
17	P1-	**Charge Pump Negative Node.** Connect a 100nF capacitor from this pin to P1+.
18	SS	**Soft-Start.** Connect a capacitor from this pin to GND to control the DRV1/DRV2 ramp up time during soft-start period.
19	P2+	**Charge Pump Positive Node.** Connect a 100nF capacitor from this pin to P2-.
20	P2-	**Charge Pump Negative Node.** Connect a100nF capacitor from this pin to P2+.
Exposed Pad	NC	**Not Internally Connected.** Although the exposed pad of uP7561Q is not electrically connected to GND. It is still highly recommended to connect the exposed pad to GND plane or maximum heat dissipation.

uP7561Q

Functional Block Diagram



Functional Description

Charge Pumps (VCC, CP+, CP-, P1+, P1-, P2+, P2-)

The uP7561Q has three integrated charge pump circuits. One is to generate the VCC power for internal logic circuit and the other two are for DRV1 and DVR2 to drive the internal/ external power MOSFET. Connect a 220nF capacitor between CP+ to CP- and 470nF capacitor from VCC pin to GND. Connect a 100nF capacitor between P1+/P1- and P2+/ P2-. **Do NOT** use other capacitance value other than the values specified here.

Drivers (DRV1 & DRV2)

The DRV1 and DRV2 are the output of internal driver. Connect DRV1 to the gate of the external power MOSFET for VIN1 and connect DRV2 to the gate of the external power MOSFET for VIN2. In some applications, extra RC circuit on DRV1/DRV2 pins is allowed to slow down DRV1/DRV2 response. Pull up DRV1/DRV2 to VCC with 1kΩ resistor to disable the external power path and select the internal power path, the internal MOSFET will be activated.

SWITCH# and STEER

The SWITCH# logic input controls DRV1 and DRV2 switch behavior. The output voltage is switched between VIN1 and VIN2 according to SWITCH# logic input.

The STEER input is a signal used to control both the DRV1 and DRV2 to turn on at the same time. When the STEER logic input is high, both power MOSFET of VIN1 and VIN2 are turned on immediately. **The STEER signal has higher priority to control the DRV1 and DRV2 behavior, improper controls of the STEER signal may cause catastrophic damage to power MOSFET.** Table 1 shows the truth table of SWITCH# and STEER signals.

Table 1. Truth Table of SWITCH# and STEER Signals

STEER	SWITCH#	VOUT
0	0	VIN1
0	1	VIN2
1	X	VIN1= VIN2

Fast Switching Application

For fast switching application, the VIN1 and VIN2 input voltage should be the same nominal voltage and both they are required to be greater than 5V. The output voltage will switch frequently between VIN1 and VIN2 according to SWITCH# input signal. Take dynamic input switch application as an example, for better understanding, assume VIN1 (from an external 12V power connector) = 12V-10% and VIN2 (from the gold finger of PCIE bus 12V) = 12V+10% and the SWITCH# frequency is around 20kHz (Figure 1).

When SWITCH# logic input is low, DRV1 ramps up to VOUT+VCC-0.8V voltage to turn on the power MOSFET of VIN1. When SWITCH# signal switches from low to high, DRV1 drives down to 0V and DRV2 ramps up from 0V to VOUT+VCC-0.8V after a 10ns dead time (Td). VIN2 power MOSFET then turns on, and the output voltage switches to VIN2 input.

Functional Description

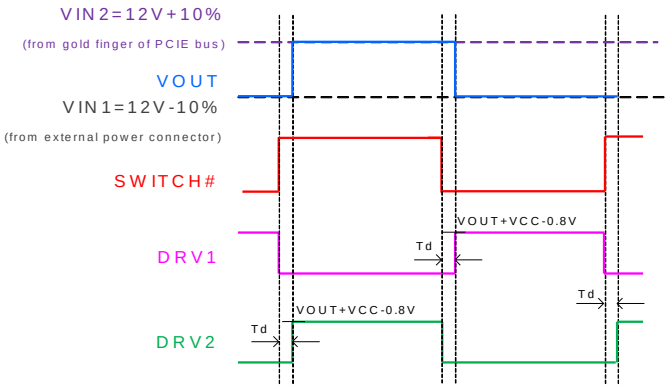


Figure 1. Fast Switching Application

Slow Switching Application

For slow switching application, the output voltage switches between VIN1 and VIN2 with different nominal voltages. The switch frequency is not fast but the voltage delta could be larger. Take RTD3 input switch application as an example, the VIN1=12V+/-10% and VIN2=3.3V+/-10%.

When one of the input voltages is lower than 5V, the uP7561Q will recognize that it works in slow switching application. When output voltage switches from high voltage to low voltage, the DRV voltage will not turn on immediately. The uP7561Q waits for the output voltage decay to its new target and then turns on the corresponding DRV and switches to its target smoothly. This mechanism avoids the output voltage undershoot and prevents the VIN2 boost from output voltage during the SWITCH# change from low to high.

For output voltage switches from low voltage to high voltage, the uP7561Q implement soft-start function to prevent the inrush current during output voltage ramps up. When one of the input voltage is greater than 5V (e.g. 3.3V ↔ 12V switch case), the soft-start time for output voltage transition is same as power up soft-start time. When both input voltages are lower than 5V (e.g. 3.3V ↔ 3.3V switch case), the soft-start time for output voltage transition is 4 times faster than power up soft-start. The uP7561Q also implements an anti-drop function for slow switching application. The anti-drop function regulates the output voltage during the dead time of the voltage transition to avoid the output voltage undershoot. Both the soft-start function and anti-drop function are only activated while at least VIN1 or VIN2 uses internal power path (Figure 2).

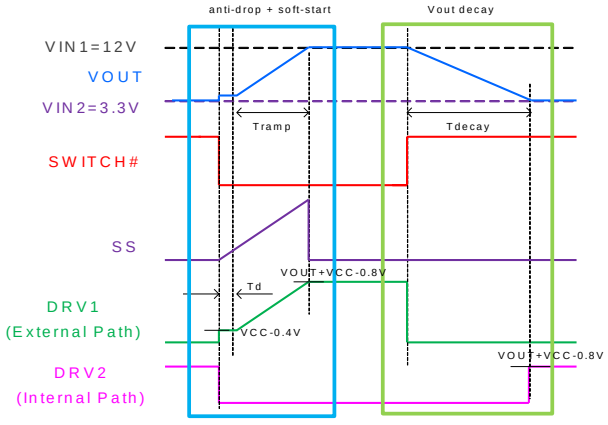


Figure 2. Slow Switching Application

uP7561Q

Functional Description

Power Up Sequence

The uP7561Q detects the VIN1 and VIN2 input voltage for power up.When either VIN1 or VIN2 input voltage is higher than 2.5V, the integrated LDO and charge pump circuit are activated. The VCC power for internal logic circuit is pumped up from input VIN1 or VIN2, and the device initializes when VCC voltage is greater than 4.25V.

The uP7561Q starts the soft-start process right upon the input voltage VIN1/VIN2 reaches its POR threshold. After typical 1.5ms initialization time, the SS voltage starts to ramp up with a constant slew rate, which can be controlled by a timing capacitor connected from SS pin to GND. The ramp up time Tss is calculated as:

$$T_{SS} = \frac{VIN \times C_{SS}}{I_{SS}}$$

Once the uP7561Q is enabled, the DRV1 and DRV2 switch behavior is controlled by SWITCH# and STEER signals even in the soft-start period. Therefore, there are 3 power-up scenarios according to different SWITCH# and STEER signals. Each power-up scenario is described in the following paragraphs.

Scenario 1: Power up by VIN1 with SWITCH# = Low. (Or power up by VIN2 with SWITCH# = High).

In this case, the DRV1 (for SWITCH#=Low) output tracks the SS signal with a constant offset (~1V) and drives the external power MOSFET to let it turn on gradually to prevent the surge current during power up. When the output voltage reaches 90% of its target, the soft-start process ends and the SS signal is internally pulled down to GND. At the same time, the DRV output is pulled up to a voltage of VOUT+VCC-0.8V (Figure 3).

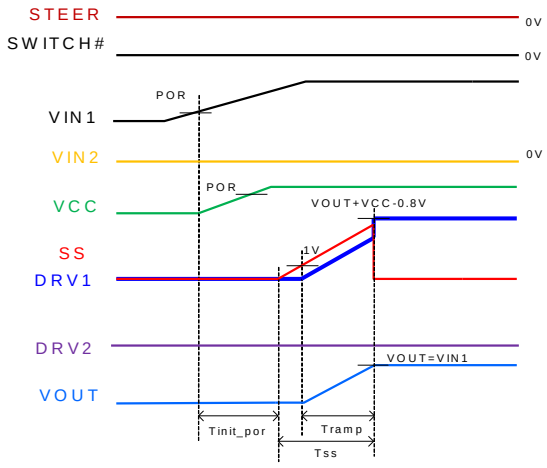


Figure 3. Power-Up Sequence of Scenario 1

Functional Description

Scenario 2 : Power up by VIN1 with SWITCH# = High. (Or power up by VIN2 with SWITCH# = Low).

When VIN1 reaches its POR threshold, the DRV1 stays low and DRV2 ramps to VCC-0.8V (for SWITCH#=High). In that time, the output voltage keeps a 0V voltage(due to DRV1=Low) even the VIN1 is ready. However, the power MOSFET of VIN2 is turned on due to DRV2=VCC-0.8V. When VIN2 input power up, the output voltage will track the VIN2 input voltage ramps up to its target (Figure 4).

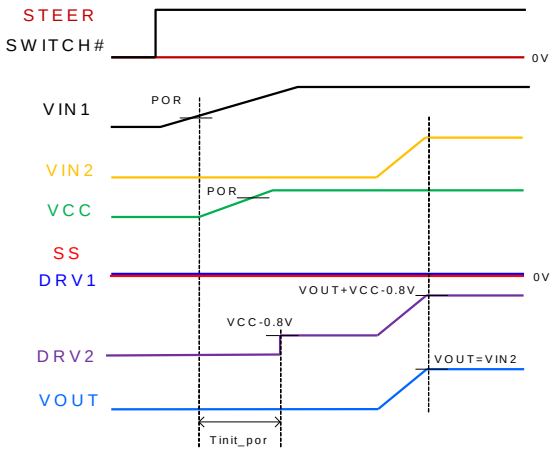


Figure 4. Power-Up Sequence of Scenario 2

Scenario 3: STEER=High before VIN POR.

STEER signal has higher priority to control the DRV1 and DRV2. When STEER=High before VIN POR, both the DRV1 and DRV2 are turned on initially. In this case, the SS voltage ramp up time becomes 5 times of the default setting timing. The output voltage, VIN1 and VIN2 voltage will ramp up synchronously to its target (Figure 5).

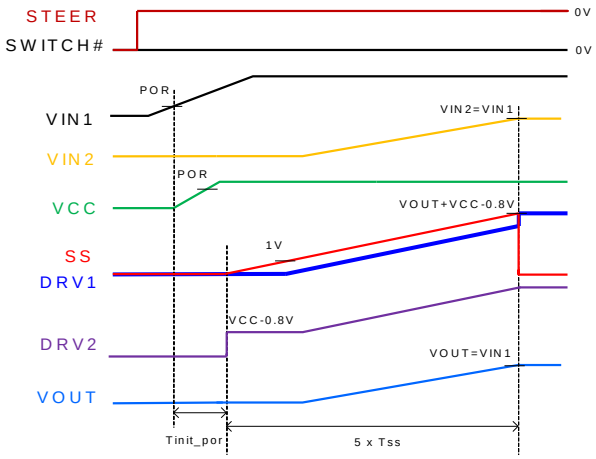


Figure 5. Power-Up Sequence of Scenario 3

Functional Description

Over Temperature Protection

The uP7561Q continuously monitors the operating temperature of the device for over temperature protection. If the junction temperature rises to approximately 160℃, the uP7561Q asserts over temperature and turns off the power MOSFET to prevent the device from damage. The over temperature protection is a latch-off protection, and can only be reset by VIN POR recycle.

uP7561Q

Absolute Maximum Rating

Supply Input Voltage, VIN1 & VIN2 (Note 1) ---------- -0.3V to +16V
Output Voltage, VOUT ---------- -0.3V to +16V
Charge Pump Negative Node, P1- and P2- ---------- -0.3V to +16V
Charge Pump Positive Node, P1+ and P2+ ---------- -0.3V to (P1-/P2- +6.5V)
SS, DRV1, DRV2 ---------- -0.3V to (VIN+6.5V)
Other Pins ---------- -0.3V to +6.5V
Storage Temperature Range ---------- -65℃ to +150℃
Junction Temperature ---------- 150℃
Lead Temperature (Soldering,10 sec) ---------- 260℃
EDS Rating (Note 2)
HBM (Human Body Mode) ---------- 2kV

Thermal Information

Package Thermal Resistance (Note 3)
WQFN3x3-20L θ_{JA} ---------- 68℃/W
WQFN3x3-20L θ_{JC} ---------- 6℃/W
Power Dissipation, P_D @ T_A = 25℃
WQFN3x3-20L ---------- 1.47W

Recommended Operation Conditions

Operating Junction Temperature Range (Note 4) ---------- -40℃ to +125℃
Operating Ambient Temperature Range ---------- -40℃ to +85℃
Supply Input Voltage, VIN1 and VIN2 ---------- +3.3V to +12V

Note 1. Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25℃ on a low effective thermal conductivity test board of *JEDEC 51-3* thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

Electrical Characteristics

(VIN1 & VIN2 = 12V, T_A = 25℃, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input						
VIN1 POR Threshold	V_{VIN1_POR}	VCC = 4.5V	--	2.5	2.7	V
VIN1 POR Hysteresis	V_{VIN1_HYS}	VCC = 4.5V	--	0.25	--	V
VIN1 Quiescent Current	V_{VIN1_Q}	VIN1=12V, DRV1 floating, VIN1 > VIN2	--	15	--	mA
VIN2 POR Threshold	V_{VIN2_POR}	VCC = 4.5V	--	2.5	2.7	V
VIN2 POR Hysteresis	V_{VIN2_HYS}	VCC = 4.5V	--	0.25	--	V
VIN2 Quiescent Current	V_{VIN2_Q}	VIN2=12V, DRV1 floating, VIN2 > VIN1	--	15	--	mA
VCC POR Threshold	V_{VCC_POR}		--	4.25	--	V
VCC POR Hysteresis	V_{VCC_HYS}		--	0.5	--	V
Switch Driver Output						
DRV1 Output Resistance, Source	R_{DRV1_SRC}	VIN1 = 12V, I_{DRV1} = 10mA	--	200	--	Ω
DRV1 Output Resistance, Sink	R_{DRV1_SNK}	VIN1 = 12V, I_{DRV1} = -10mA	--	5	--	Ω
DRV2 Output Resistance, Source	R_{DRV2_SRC}	VIN2 = 12V, I_{DRV2} = 10mA	--	200	--	Ω
DRV2 Output Resistance, Sink	R_{DRV2_SNK}	VIN2 = 12V, I_{DRV2} = -10mA	--	5	--	Ω
Dead Time		from DRV1 low to DRV2 high; from DRV2 low to DRV1 high	--	10	--	ns
Internal Power Switch for VIN1						
Output Drop Voltage		output current = 0.2A	--	50	--	mV
Leakage Current		DRV1 floating	--	--	1	uA
Reverse Leakage Current		DRV1 floating	--	--	1	uA
Internal Power Switch for VIN2						
Output Drop Voltage		output current = 1A	--	50	--	mV
Leakage Current		DRV2 floating	--	--	1	uA
Reverse Leakage Current		DRV2 floating	--	--	1	uA

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Logic Input (SWITCH# and STEER)						
Input High			1.2	--	--	V
Input Low			--	--	0.6	V
Deglitch Time		SWITCH# & STEER de-assertion	--	600	1000	ns
Soft Start						
VIN1, VIN2 POR Initialization Time	T_{INIT_POR}		--	1.5	--	ms
SS Sourcing Current			--	30	--	uA
Protection						
Thermal Shutdown Threshold			--	160	--	℃

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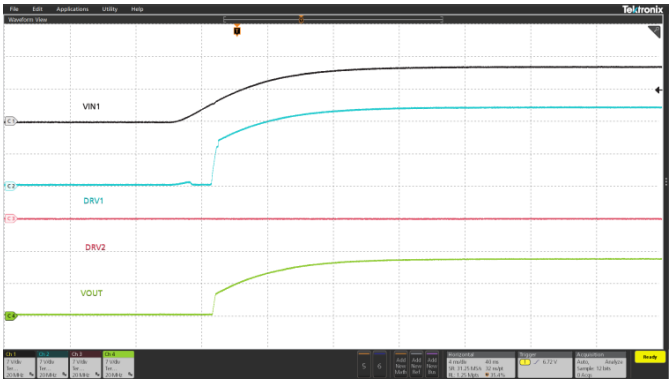
Typical Operation Characteristics

VIN1 Power On, SWITCH# = low

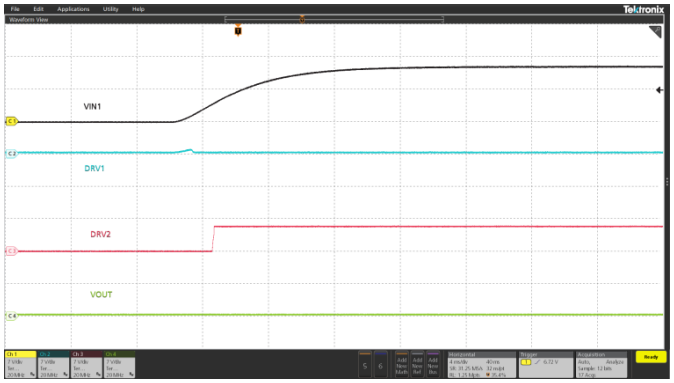


Time: 4ms/Div

VIN1(7V/Div);VOUT(7V/Div);DRV1(7V/Div);DRV2(7V/Div)

VIN1=12V,VIN2=0V,IOUT=0A

VIN1 Power On, SWITCH# = high

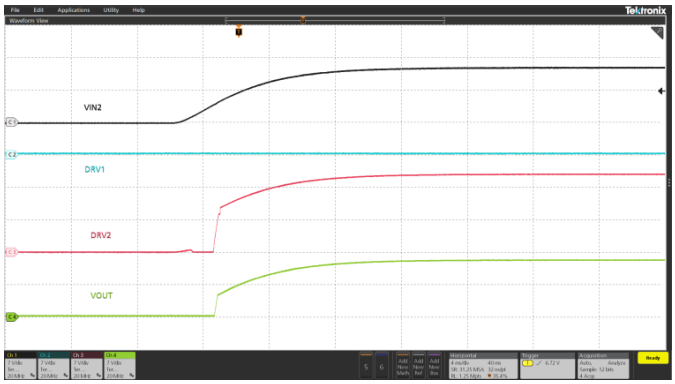


Time:4ms/Div

VIN1(7V/Div);VOUT(7V/Div);DRV1(7V/Div);DRV2(7V/Div)

VIN1=12V,VIN2=0V,IOUT=0A

VIN2 Power On, SWITCH#=high

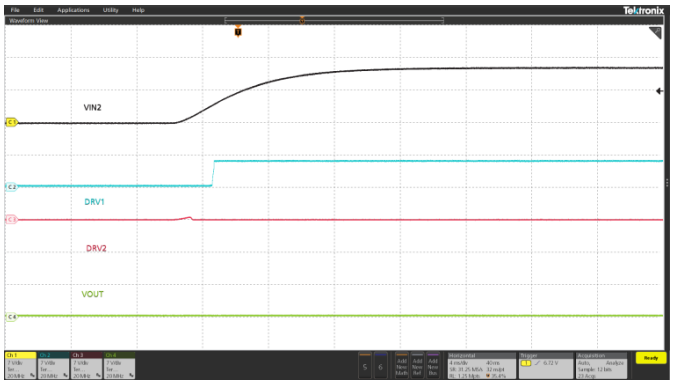


Time: 4ms/Div

VIN2(7V/Div);VOUT(7V/Div);DRV1(7V/Div);DRV2(7V/Div)

VIN1=0V,VIN2=12V,IOUT=0A

VIN2 Power On, SWITCH#=low

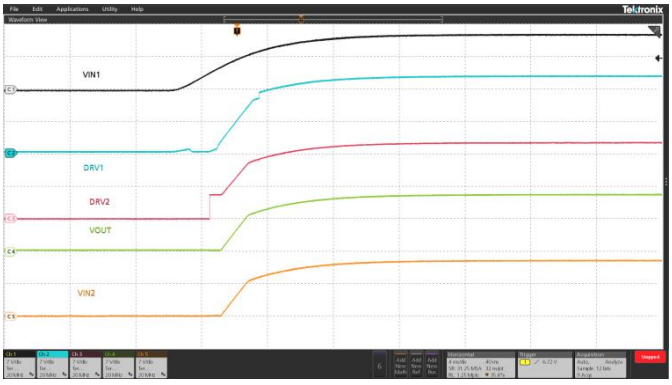


Time: 4ms/Div

VIN2(7V/Div);VOUT(7V/Div);DRV1(7V/Div);DRV2(7V/Div)

VIN1=0V,VIN2=12V,IOUT=0A

VIN1 Power On, STEER=high

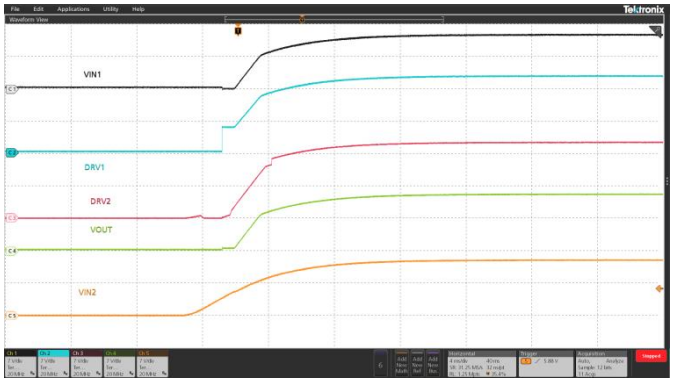


Time: 4ms/Div

VIN1(7V/Div);VOUT(7V/Div);DRV1(7V/Div);DRV2(7V/Div);VIN2(7V/Div)

VIN1=12V,VIN2=floating,IOUT=0A,SWITCH#=low

VIN2 Power On, STEER=high



Time: 4ms/Div

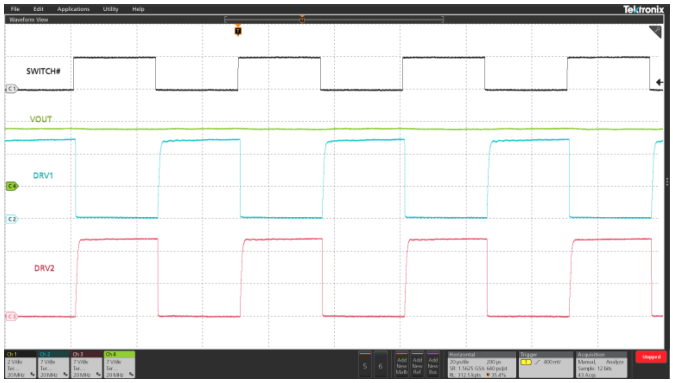
VIN1(7V/Div);VOUT(7V/Div);DRV1(7V/Div);DRV2(7V/Div);VIN2(7V/Div)

VIN1=floating,VIN2=12V,IOUT=0A,SWITCH#=high

uP7561Q

Typical Operation Characteristics

Fast Switching

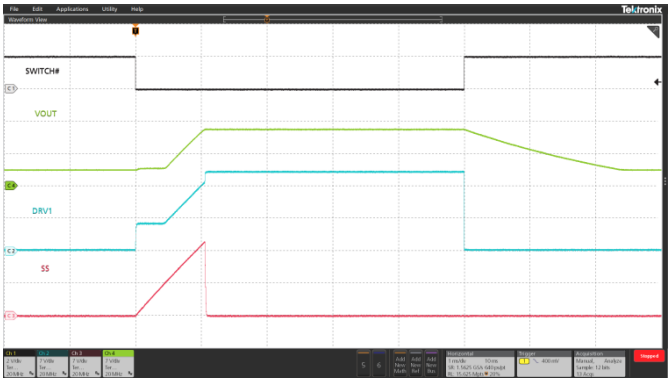


Time: 20us/Div

SWITCH#(2V/Div);VOUT(7V/Div);DRV1(7V/Div);DRV2(7V/Div)

VIN1=12V,VIN2=12V,IOUT=0A,Frequency=20kHz

Slow Switching



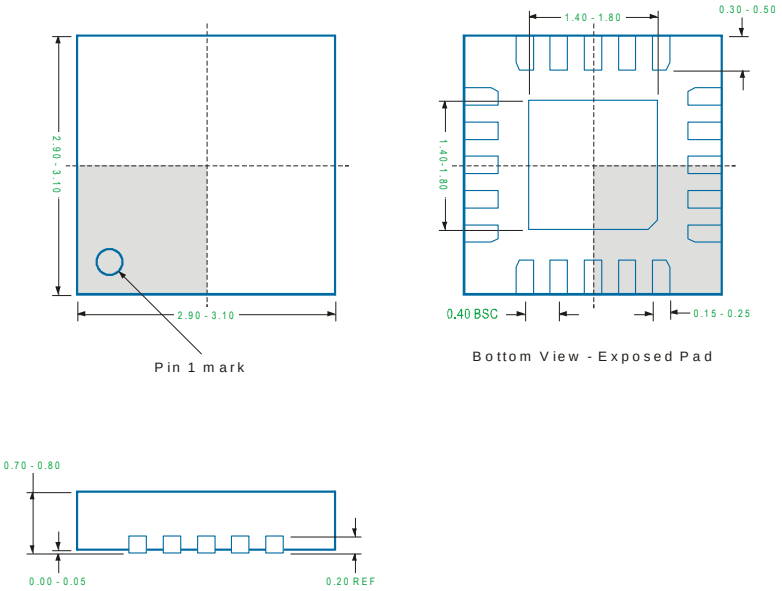
Time: 1ms/Div

SWITCH#(2V/Div);VOUT(7V/Div);DRV1(7V/Div);DRV2(7V/Div)

VIN1=12V(external path),VIN2=3.3V(internal path),IOUT=0.1A

uP7561Q
Package Information

WQFN3x3-20L



Note

1. Package Outline Unit Description:
   MIN: Minimum dimension specified.
   NOM: Nominal. Provided as a general value.
   MAX: Maximum dimension specified.
   BSC: Basic. Represents theoretical exact dimension or dimension target.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

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