

CHIPLINK N-Channel Enhancement Mode Power MOSFET

Description

The LX2300 combines advanced trench technology to provide excellent $R_{DS(ON)}$. This device is suitable for use as a load switch or PWM applications.

Features

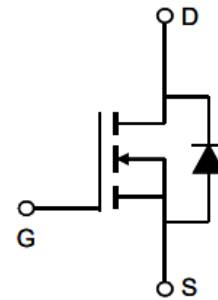
- $V_{DS}=20V$, $I_D=6A$
 $R_{DS(ON)} < 28m\Omega @ V_{DS}=4.5V$
 $R_{DS(ON)} < 33m\Omega @ V_{DS}=2.5V$
- High power and current handling capability
- Termination is Lead-free and RoHS Compliant



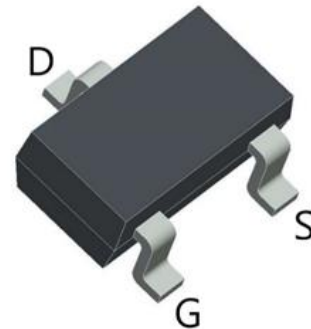
Applications

- PWM applications
- Load switch
- Power Management

schematic diagram



SOT23 Package



Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 10	V
Continuous Drain Current	I_D	6	A
Pulsed Drain Current ^B	I_{DM}	20	A
Maximum Power Dissipation ^A	P_D	1.25	W
Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction to Ambient	R_{QJA}	100	$^\circ C/W$
---	-----------	-----	--------------

Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Test conditions	MIN	TYP	MAX	UNIT
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	20			V
Gate-Threshold Voltage	$V_{th(GS)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.4	0.65	1.1	V
Gate-body Leakage	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 10V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=20V, V_{GS}=0V$			1	μA
Drain-Source On-Resistance	$R_{DS(ON)}$	$V_{GS}=4.5V, I_D=2.5A$		19	28	m Ω
		$V_{GS}=2.5V, I_D=2.0A$		22	33	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_D=1.0A$	2			S
Dynamic Characteristics						
Input Capacitance	C_{iss}	$V_{DS}=10V, V_{GS}=0V, F=1MHz$		457		pF
Output Capacitance	C_{oss}			71		
Reverse Transfer Capacitance	C_{rss}			60		
Switching Capacitance						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=10V, R_L=2.9\Omega, V_{GS}=4.5V, R_{GEN}=3\Omega$		4.1		nS
Turn-on Rise Time	t_r			11.6		nS
Turn-off Delay Time	$t_{d(off)}$			25		nS
Turn-off Fall Time	t_f			7.6		nS
Total Gate Charge	Q_g	$V_{DS}=10V, I_D=2A, V_{GS}=4.5V$		6.6		nC
Gate-Source Charge	Q_{gs}			0.4		nC
Gate-Drain Charge	Q_{gd}			2		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_D=5A$			1.2	V
Diode Forward Current	I_S				2.0	A

Notes:

- A. The Power dissipation P_D is based on $T_{J(MAX)}=150^{\circ}\text{C}$, using $\leq 10s$ junction-to ambient thermal resistance.
- B. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=150^{\circ}\text{C}$. Ratings are based on low frequency and duty cycles to keep initial $T_J=25^{\circ}\text{C}$.
- C. The Static characteristics in Figures are obtained using $< 300\mu s$ pulses, duty cycle 2% max.

Typical Electrical and Thermal Characteristics

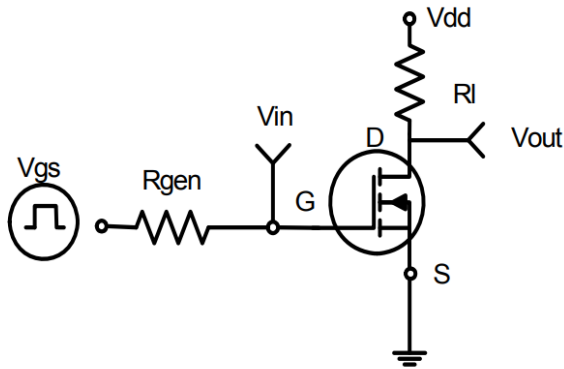


Figure 1: Switching Test Circuit

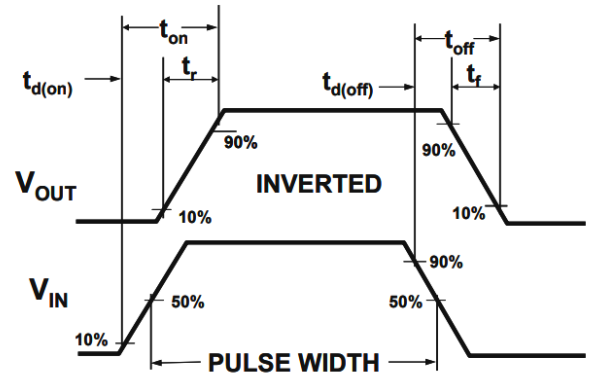


Figure 2: Switching Waveforms

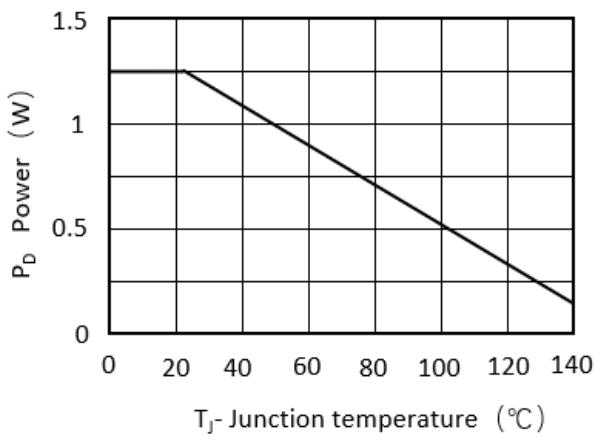


Figure 3 Power Dissipation

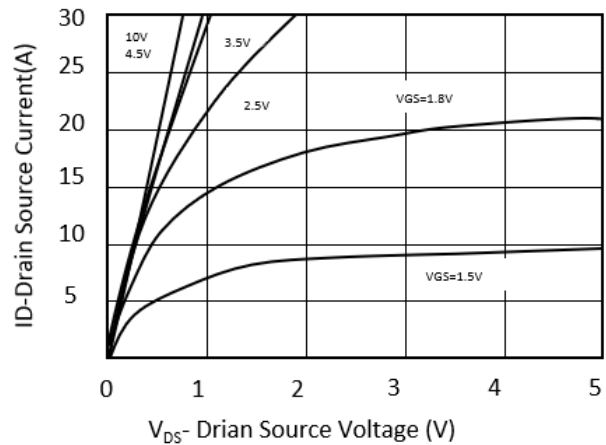


Figure 4 Output Characteristics

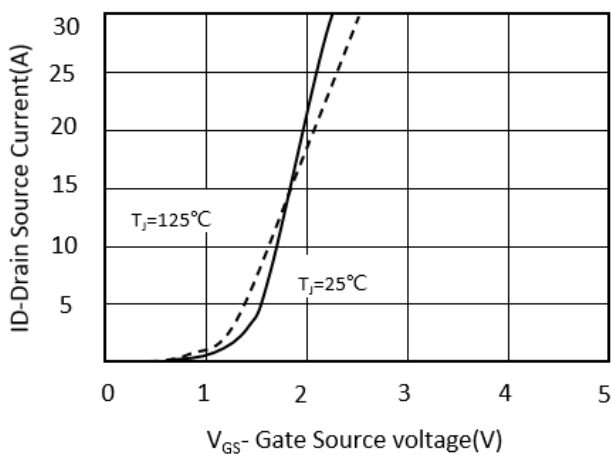


Figure 5 Transfer Characteristics

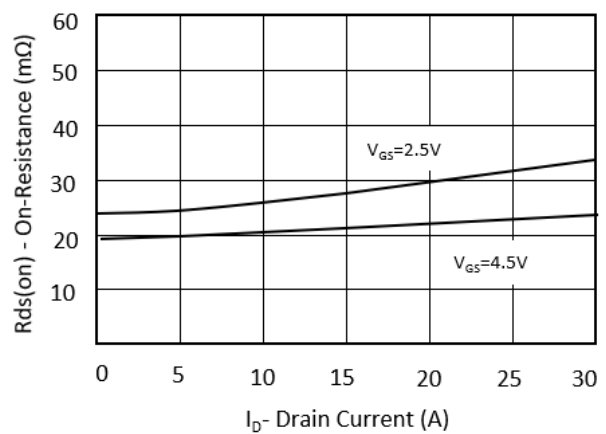


Figure 6 Drain-Source On Resistance

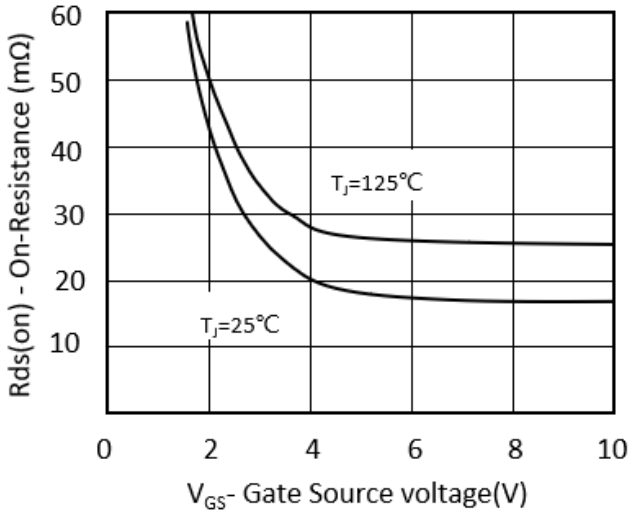


Figure 7 $R_{ds(on)}$ VS V_{GS}

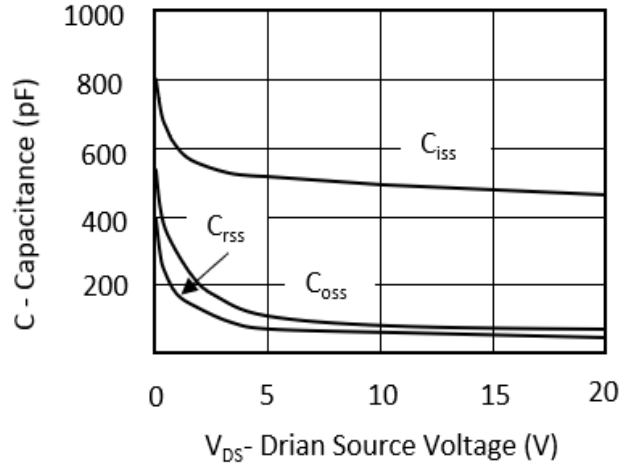


Figure 8 Capacitance VS V_{DS}

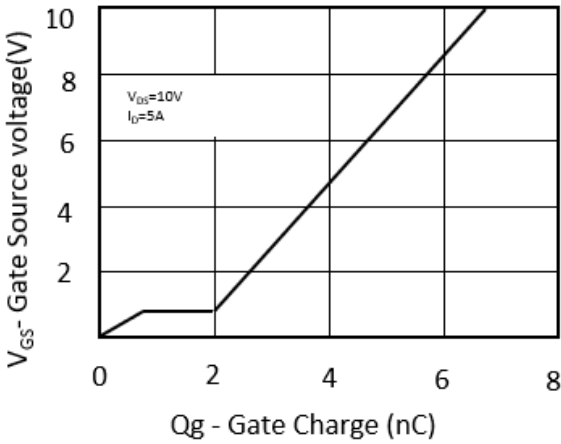


Figure 9 Gate Charge

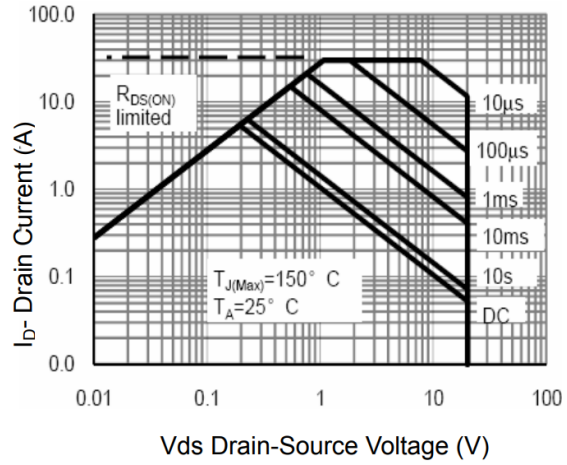


Figure 10 Safe Operation Area

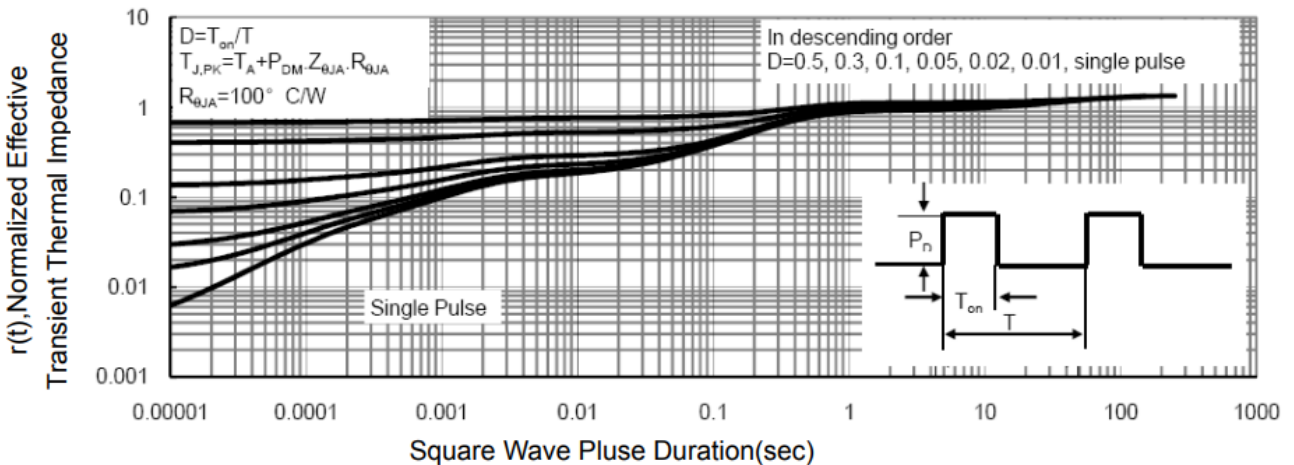
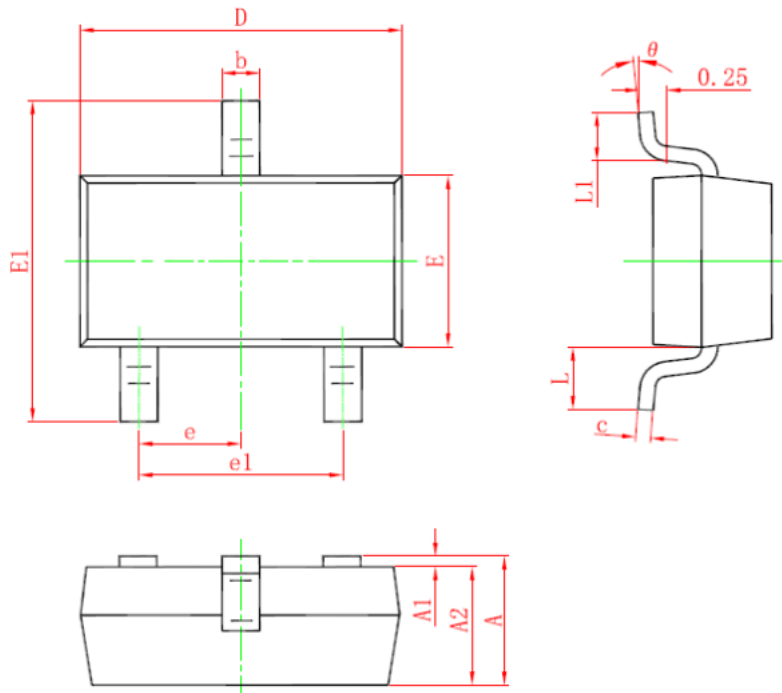


Figure 11 Normalized Maximum Transient Thermal Impedance

SOT-23 Package Information


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP.		0.037 TYP.	
e1	1.800	2.000	0.071	0.079
L	0.550 REF.		0.022 REF.	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°

THIS PRODUCT HAS BEEN DESIGNED AND QUALIFIED FOR THE CONSUMER MARKET. APPLICATIONS OR USES AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED.

CHIPLINK DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS.

THIS DOCUMENT SUPERSEDES AND REPLACES ALL INFORMATION PREVIOUSLY SUPPLIED. CHIPLINK RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN, FUNCTIONS AND RELIABILITY WITHOUT NOTICE.