



PSMP061-60YE

60 V, P-channel Trench MOSFET

13 January 2021

Product data sheet

1. General description

P-channel enhancement mode MOSFET in an LFPAK56 (Power SO8) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- High thermal power dissipation capability
- Suitable for thermally demanding environments due to 175 °C rating
- Trench MOSFET technology

3. Applications

- Reverse battery protection
- Power management
- High-side load switch
- Motor drive

4. Quick reference data

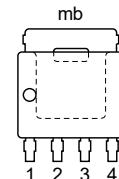
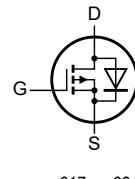
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25 \text{ }^\circ\text{C}$	-	-	-60	V
V_{GS}	gate-source voltage		-20	-	20	V
I_D	drain current	$V_{GS} = -10 \text{ V}; T_{mb} = 25 \text{ }^\circ\text{C}$	-	-	-25	A
P_{tot}	total power dissipation	$T_{mb} = 25 \text{ }^\circ\text{C}$	-	-	66	W
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = -10 \text{ V}; I_D = -4.7 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$		-	48	61
						$\text{m}\Omega$

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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LFPAK56; Power-SO8 (SOT669)	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMP061-60YE	LFPAK56; Power-SO8	plastic, single-ended surface-mounted package; 4 terminals	SOT669

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMP061-60YE	06160YE

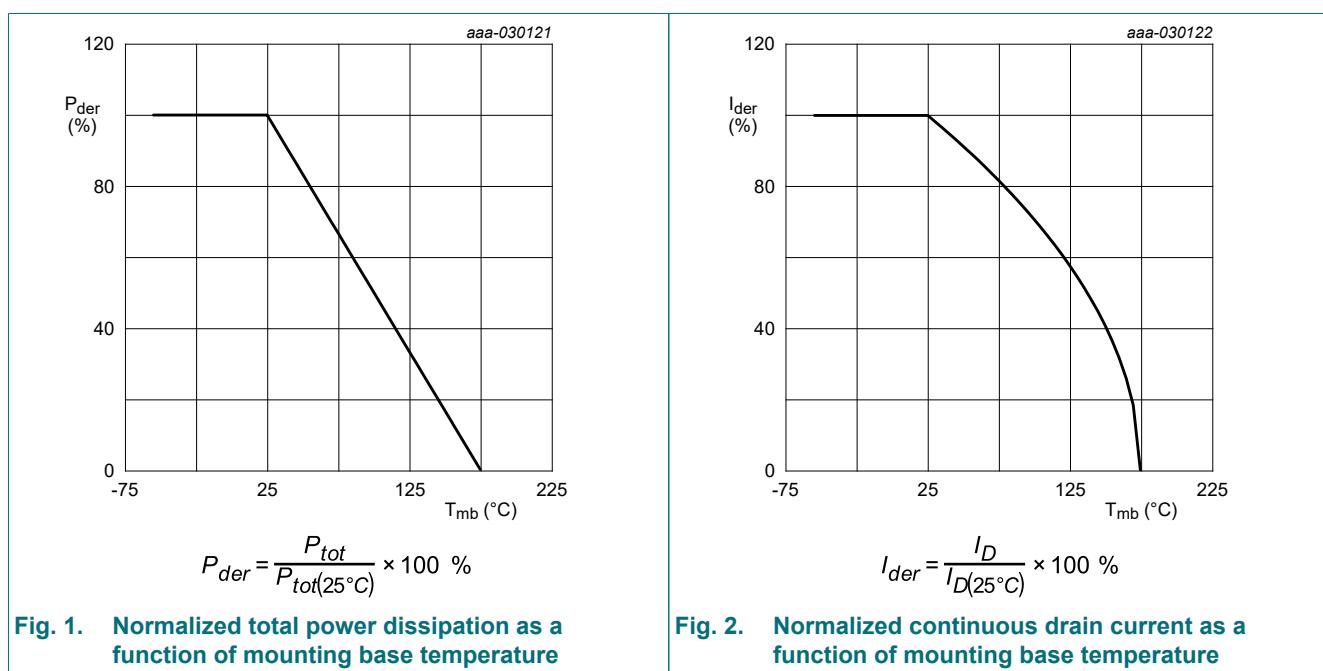
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C		-	-60	V
V _{GS}	gate-source voltage			-20	20	V
I _D	drain current	V _{GS} = -10 V; T _{mb} = 25 °C		-	-25	A
		V _{GS} = -10 V; T _{mb} = 100 °C		-	-17.7	A
I _{DM}	peak drain current	single pulse; t _p ≤ 10 µs; T _{mb} = 25 °C		-	-90	A
P _{tot}	total power dissipation	T _{mb} = 25 °C		-	66	W
T _j	junction temperature			-55	175	°C
T _{amb}	ambient temperature			-55	175	°C
T _{stg}	storage temperature			-65	175	°C
Source-drain diode						
I _S	source current	T _{mb} = 25 °C		-	-25	A
I _{SM}	peak source current	single pulse; t _p ≤ 10 µs; T _{mb} = 25 °C		-	-90	A
ESD maximum rating						
V _{ESD}	electrostatic discharge voltage	HBM	[1]	-	800	V
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	T _{j(init)} = 25 °C; I _D = -4.6 A; DUT in avalanche (unclamped)		-	61	mJ

[1] Measured between all pins.



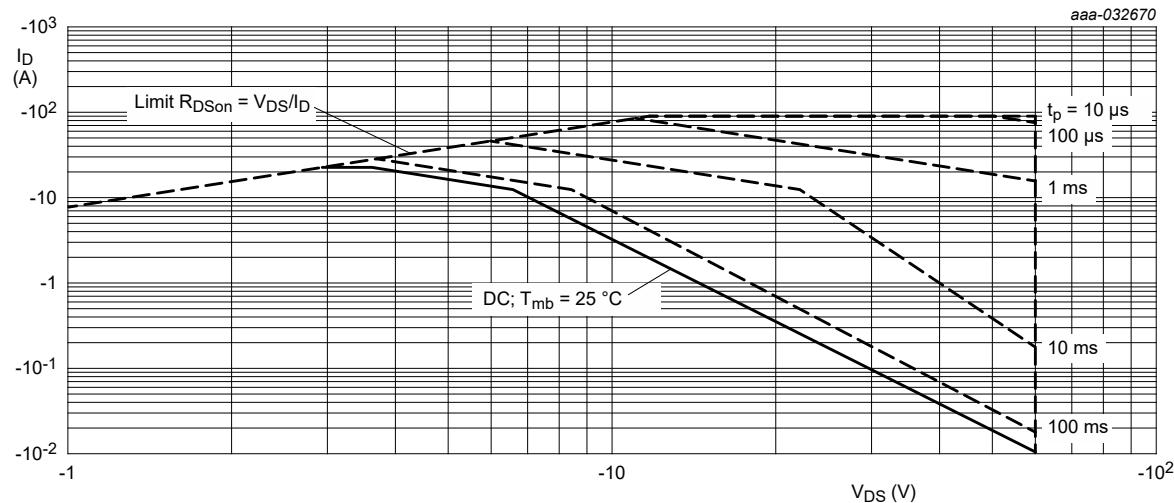


Fig. 3. Safe operating area; junction to mounting base; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	99	109	K/W
			[2]	-	47	52	K/W
$R_{th(j-mb)}$	thermal resistance from junction to mounting base			-	1.8	2.3	K/W

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm^2 .

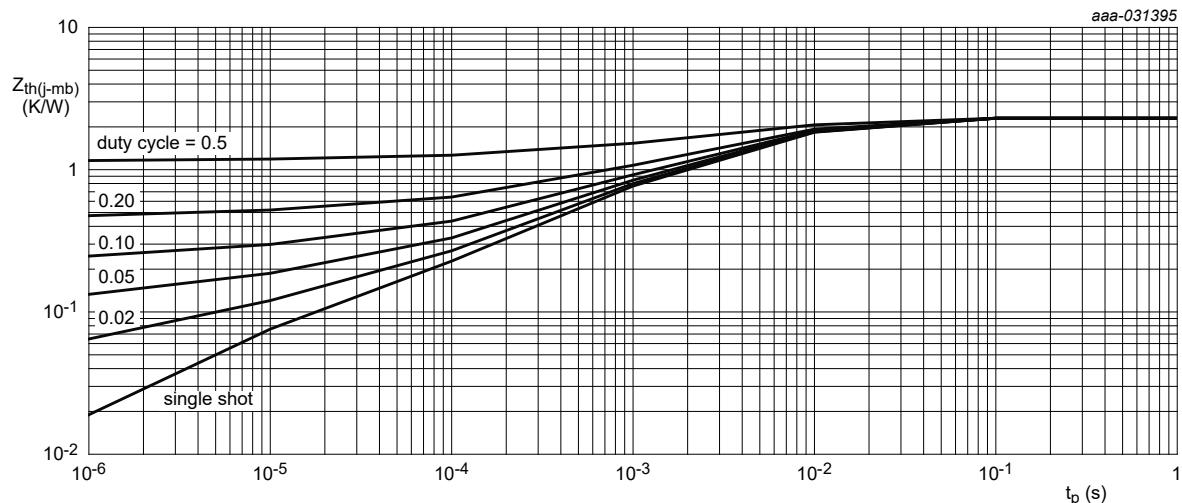
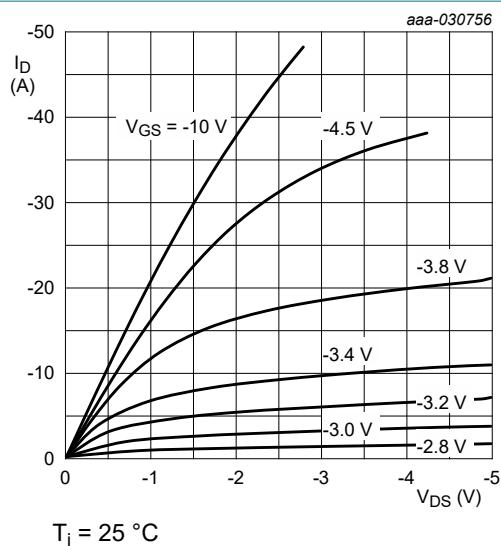


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

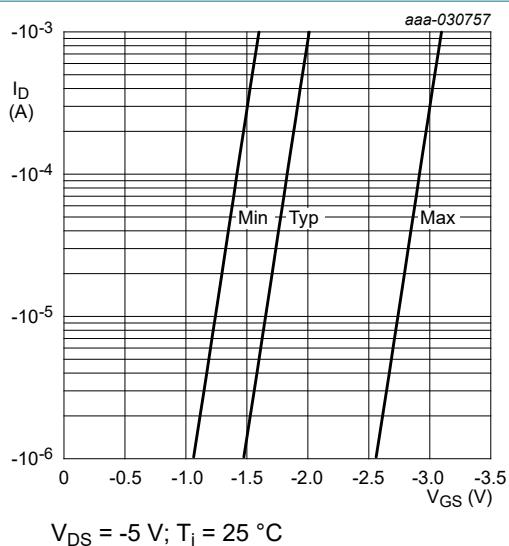
10. Characteristics

Table 7. Characteristics

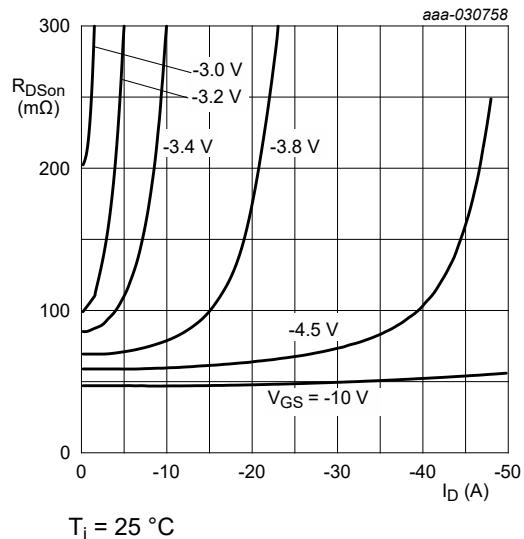
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250 \mu A; V_{GS} = 0 V; T_j = 25^\circ C$		-60	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = -250 \mu A; V_{DS}=V_{GS}; T_j = 25^\circ C$		-1.5	-2	-3	V
I_{DSS}	drain leakage current	$V_{DS} = -60 V; V_{GS} = 0 V; T_j = 25^\circ C$		-	-	-1	μA
		$V_{DS} = -60 V; V_{GS} = 0 V; T_j = 125^\circ C$		-	-	-10	μA
I_{GSS}	gate leakage current	$V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25^\circ C$		-	-	-100	nA
		$V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25^\circ C$		-	-	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = -10 V; I_D = -4.7 A; T_j = 25^\circ C$		-	48	61	$m\Omega$
		$V_{GS} = -10 V; I_D = -4.7 A; T_j = 175^\circ C$		-	100	130	$m\Omega$
		$V_{GS} = -4.5 V; I_D = -3.8 A; T_j = 25^\circ C$		-	62	93	$m\Omega$
g_{fs}	forward transconductance	$V_{DS} = -10 V; I_D = -4 A; T_j = 25^\circ C$		-	65	-	S
R_G	gate resistance	$f = 1 \text{ MHz}; T_j = 25^\circ C$		-	12	-	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	$V_{DS} = -30 V; I_D = -4.7 A; V_{GS} = -10 V; T_j = 25^\circ C$		-	20	30	nC
Q_{GS}	gate-source charge			-	3.3	-	nC
Q_{GD}	gate-drain charge			-	4.3	-	nC
C_{iss}	input capacitance	$V_{DS} = -30 V; f = 1 \text{ MHz}; V_{GS} = 0 V; T_j = 25^\circ C$		-	1060	-	pF
C_{oss}	output capacitance			-	85	-	pF
C_{rss}	reverse transfer capacitance			-	49	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = -30 V; I_D = -4.7 A; V_{GS} = -10 V; R_{G(ext)} = 6 \Omega; T_j = 25^\circ C$		-	12	-	ns
t_r	rise time			-	58	-	ns
$t_{d(off)}$	turn-off delay time			-	21	-	ns
t_f	fall time			-	204	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	$I_S = -22.4 A; V_{GS} = 0 V; T_j = 25^\circ C$		-	-0.7	-1.2	V
t_{rr}	reverse recovery time	$I_S = -22.4 A; dI_S/dt = 100 A/\mu s; V_{GS} = -10 V; V_{DS} = -30 V; T_j = 25^\circ C$		-	30	-	ns
Q_r	recovered charge			-	37	-	nC



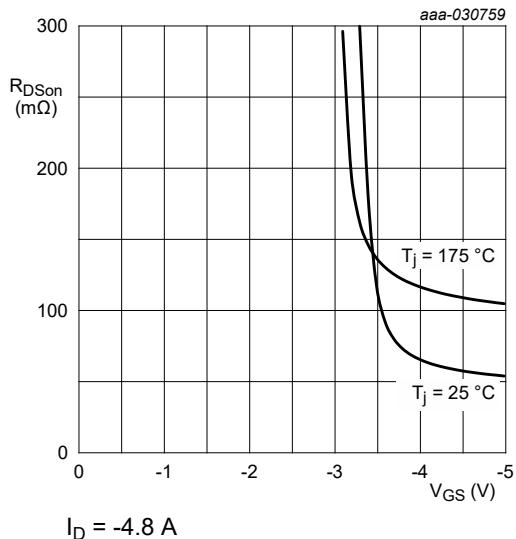
$T_j = 25^\circ\text{C}$



$V_{DS} = -5\text{ V}; T_j = 25^\circ\text{C}$



$T_j = 25^\circ\text{C}$



$I_D = -4.8\text{ A}$

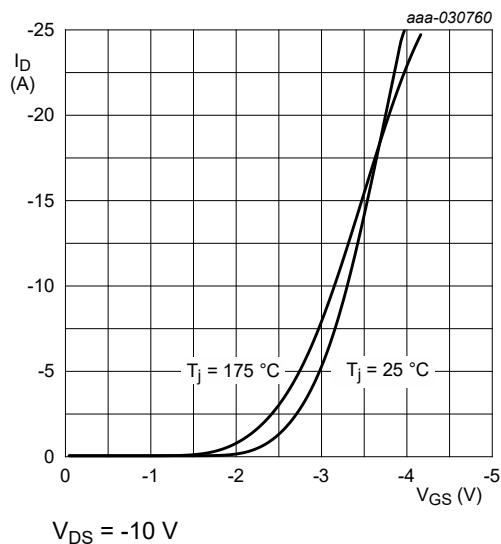


Fig. 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values

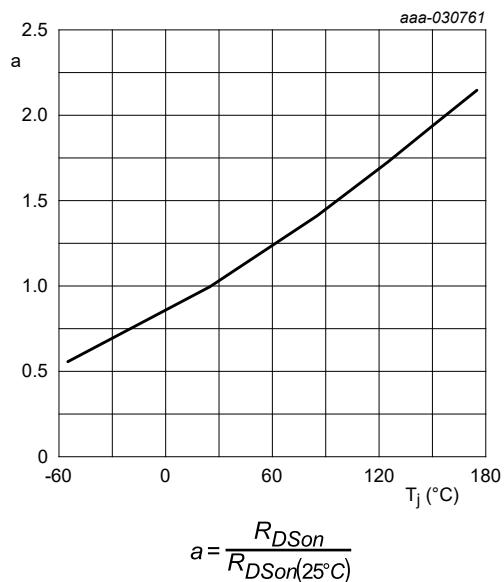


Fig. 10. Normalized drain-source on-state resistance as a function of junction temperature; typical values

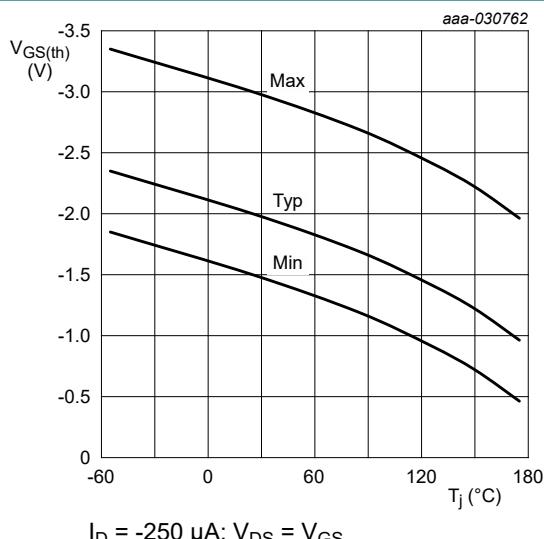


Fig. 11. Gate-source threshold voltage as a function of junction temperature

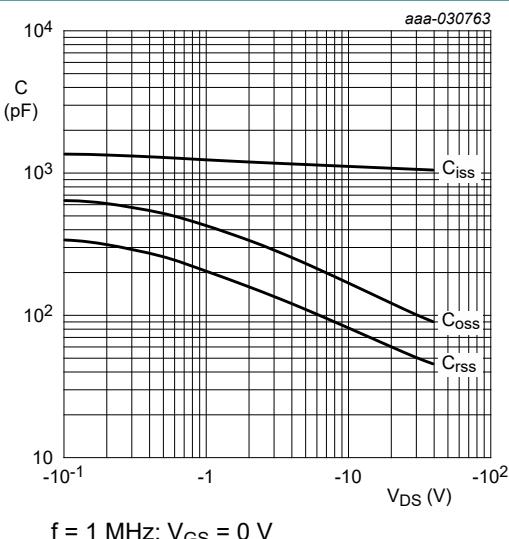
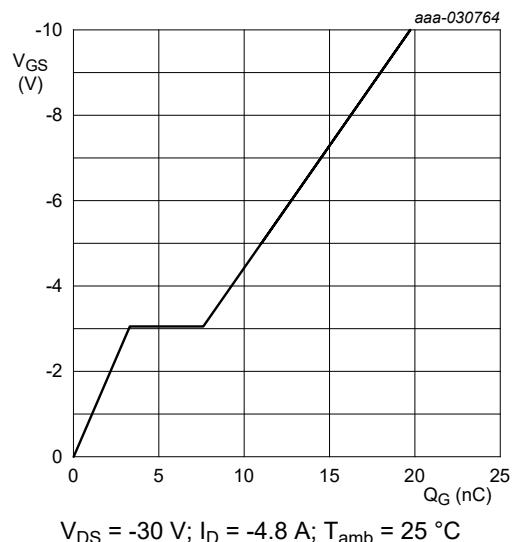


Fig. 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{DS} = -30$ V; $I_D = -4.8$ A; $T_{amb} = 25$ °C

Fig. 13. Gate-source voltage as a function of gate charge; typical values

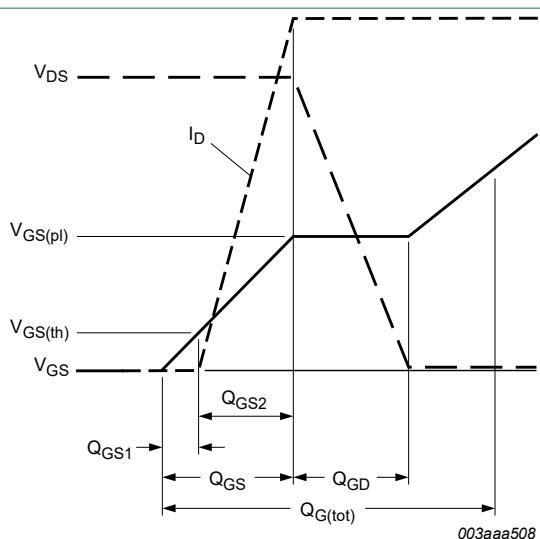
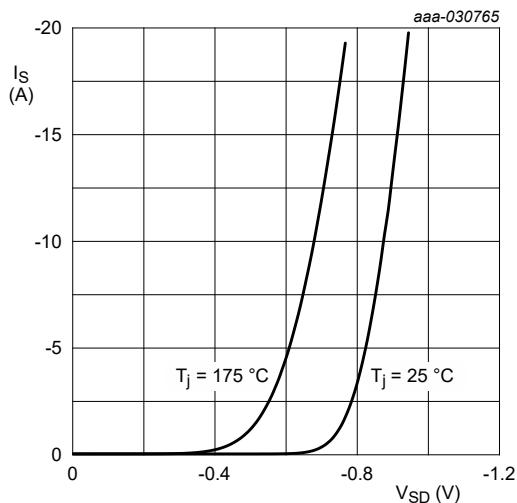


Fig. 14. Gate charge waveform definitions



$V_{GS} = 0$ V

Fig. 15. Source current as a function of source-drain voltage; typical values

11. Test information

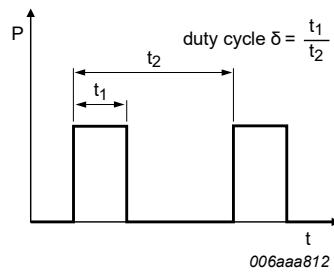
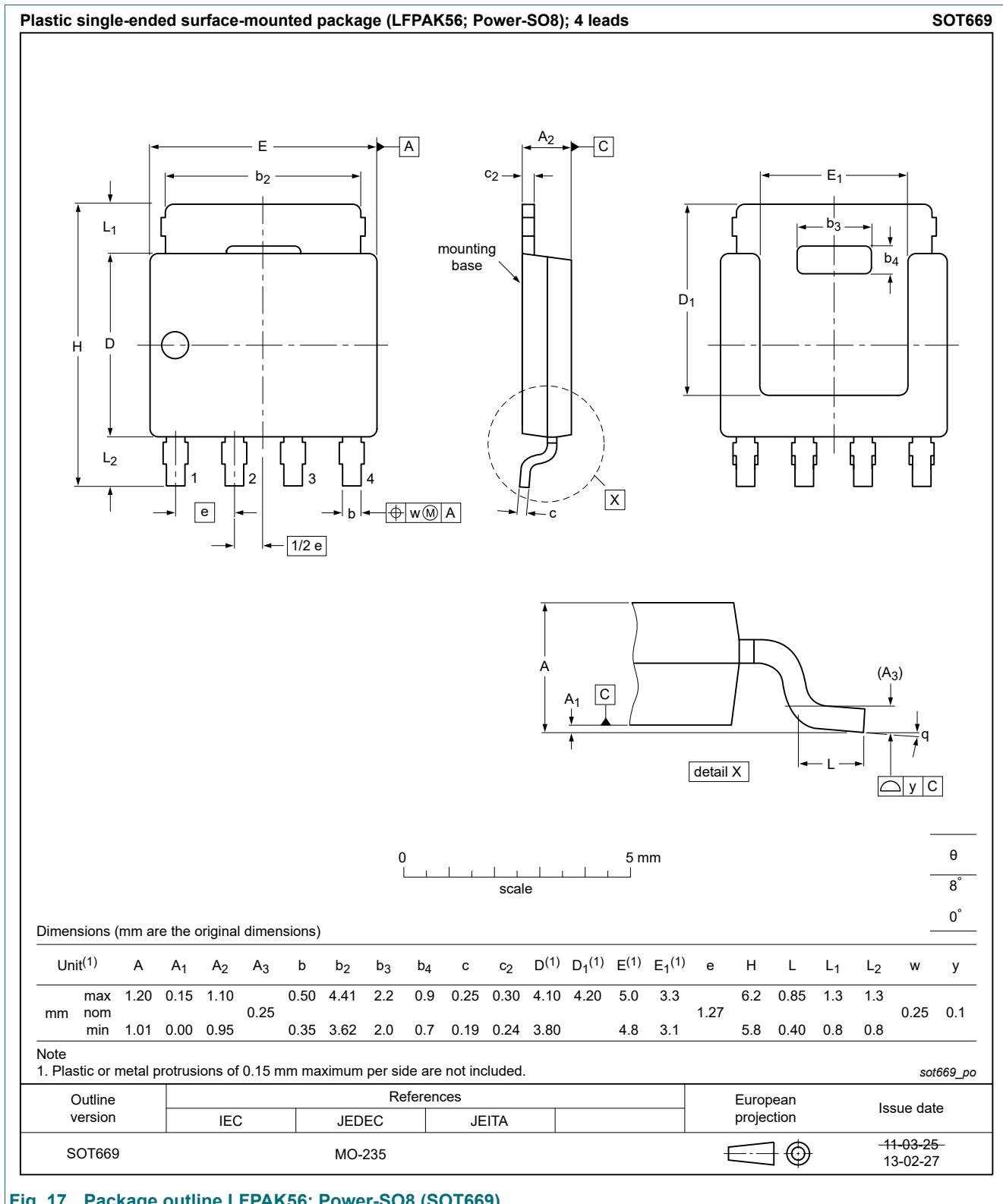


Fig. 16. Duty cycle definition

12. Package outline



13. Soldering

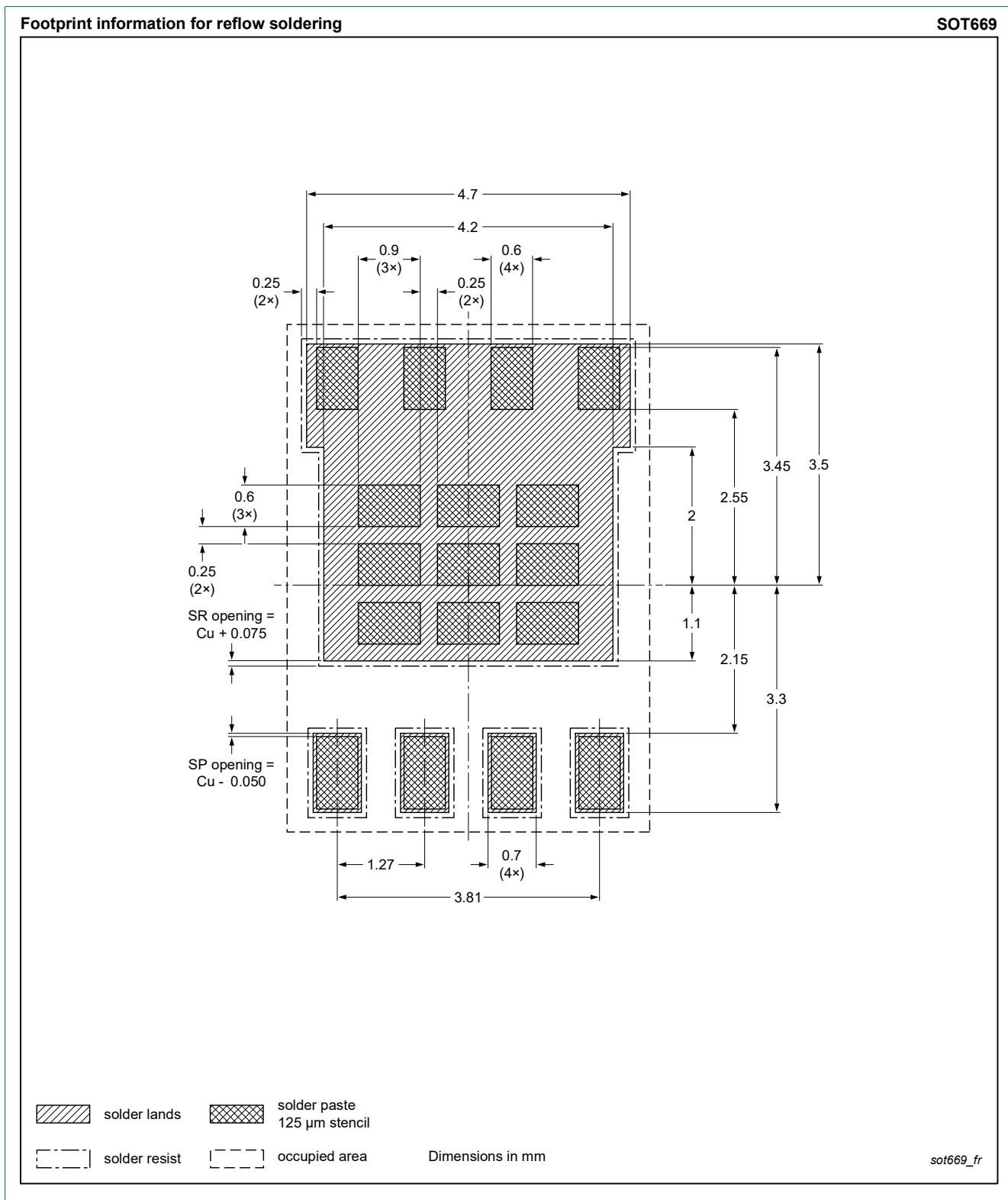
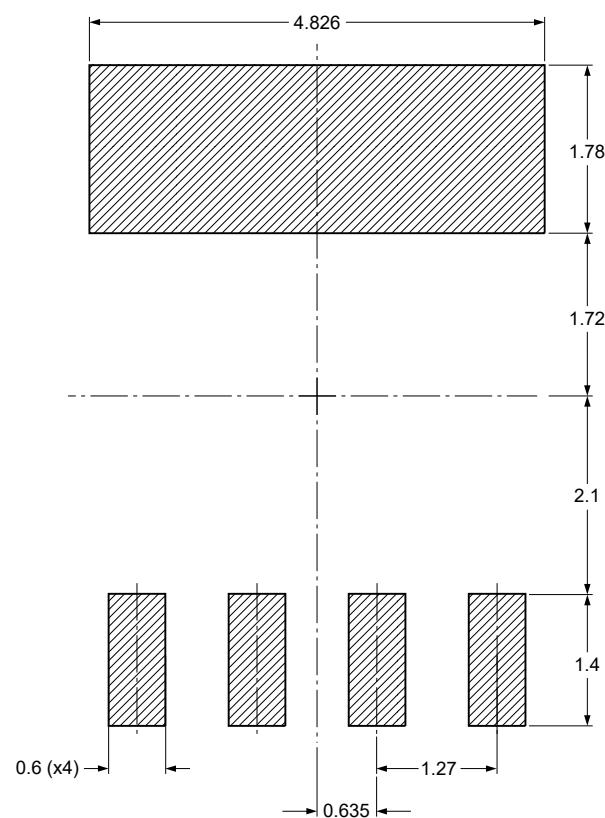


Fig. 18. Reflow soldering footprint for LFPAK56; Power-SO8 (SOT669)

Wave soldering footprint information for LFPAK56 package

SOT669

 solder lands

Dimensions in mm

Issue date 15-04-13
15-04-16

sot669_fw

Fig. 19. Wave soldering footprint for LFPAK56; Power-SO8 (SOT669)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PSMP061-60YE v.1	20210113	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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