



BK7238 Datasheet

DS-BK7238-E10 V1.6

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1. Features

Wi-Fi

- IEEE 802.11 b/g/n 1x1 compliant
- Supports 20 MHz channel
- STBC supported
- Working mode STA, AP, Direct
- Concurrent AP + STA
- TX power up to +19 dBm
- RX sensitivity -99 dBm

Bluetooth Low Energy

- Bluetooth 5.2 Low Energy (LE)
- Supports Bluetooth Low Energy 1 Mbps, 2 Mbps, and long range (125 kbps and 500 kbps)
- Advertising extensions
- Bluetooth direction finding: Angle of Arrival (AoA) and Angle of Departure (AoD)
- Supports an antenna array with up to 16 antennas for precise positioning

Core

- 32-bit MCU at up to 160 MHz
- UART Flash download
- JTAG debug interface

Memory

- SiP Flash: 1 MB, 2 MB, or none
- 288 KB RAM
- 4-byte eFuse

Clock Management

- External oscillator: 26 MHz crystal oscillator (XTALH)
- Internal oscillator: 26–160 MHz digitally controlled oscillator (DCO), 32 kHz ring oscillator (ROSC)
- 480 MHz DPLL



Power Management

- 2.7 to 3.6 V VBAT supply
- On-chip Power-On Reset (POR) and Brown-Out Detector (BOD)
- Embedded LDO regulators
- Low power consumption:
 - Active mode RX: 30 mA
 - Normal sleep mode: 300 μ A
 - Low-voltage sleep mode: 75 μ A
 - Shutdown mode: 0.5 μ A

Peripherals

- GPIOs: 19 in QFN32, 19 in QFN32, 9 in QFN20
- 1x SPI
- 2x UART: 1 with Flash download support
- 1x I2C
- 1x general-purpose DMA controller (GDMA) with 6 channels
- 6x 32-bit PWM channel
- 10-bit AUX ADC, up to 6 channels
- 6x general-purpose 32-bit timer
- 1x watchdog timer (WDT)
- 1x real-time counter (RTC)
- 1x temperature sensor
- 1x true random number generator (TRNG)

Packaging

- QFN40 package, 5 x 5 mm
- QFN32 package, 4 x 4 mm
- QFN20 package, 3 x 3 mm

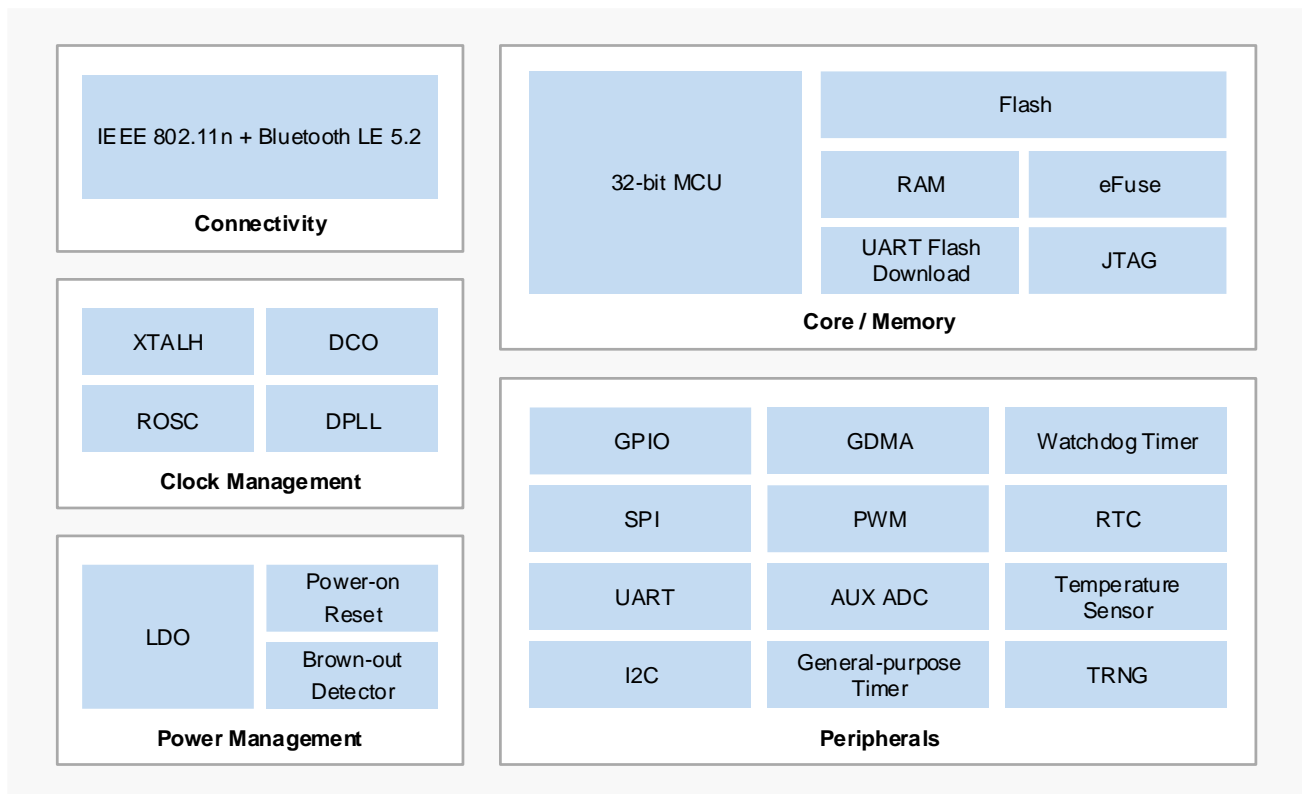
2. Overview

The BK7238 is a highly-integrated single-chip Wi-Fi 802.11n and Bluetooth 5.2 Low Energy (LE) combo solution designed for applications that require low power consumption and compact size. The integration of a powerful 32-bit MCU and a comprehensive set of peripherals and interfaces makes the BK7238 ideal for advanced Internet of Things (IoT) applications.

Using advanced design techniques and process technology, the BK7238 delivers high integration and minimal power consumption in extremely small packages for smart lighting, smart home, positioning, and other advanced IoT applications.

Figure 2-1 shows the general block diagram of BK7238.

Figure 2-1 BK7238 Block Diagram



The BK7238 devices are offered in several packages. The set of included peripherals varies depending on the package. Table 2-1 shows the list of peripherals available on each part number.

Table 2-1 Device Options and Features

Feature	QFN40	QFN32	QFN20
Flash	-	1 MB or 2 MB	1 MB or 2 MB

Feature		QFN40	QFN32	QFN20
GPIO		19	19	9
SPI	Master/Slave	1	1	-
UART		2	2	2
I2C	Master/Slave	1	1	1
GDMA		1	1	1
PWM	PWM0–5	6	6	5
AUX ADC	10 bits	1	1	1
	Number of channels	6	6	4
General-purpose timer		6	6	6
Watchdog timer (WDT)		1	1	1
Real-time counter (RTC)		1	1	1
Temperature sensor		1	1	1
TRNG		1	1	1
Package		5 x 5 mm QFN40	4 x 4 mm QFN32	3 x 3 mm QFN20
Operating voltage		2.7 to 3.6 V		

3. Pin Description

The BK7238 provides WLAN and Bluetooth LE functionality in several packages ranging from 20 pins to 40 pins.

3.1 QFN40 Pin Description

Figure 3-1 shows the pin assignments of the 5 x 5 mm, 40-pin QFN package.

Figure 3-1 QFN40 Pin Assignments

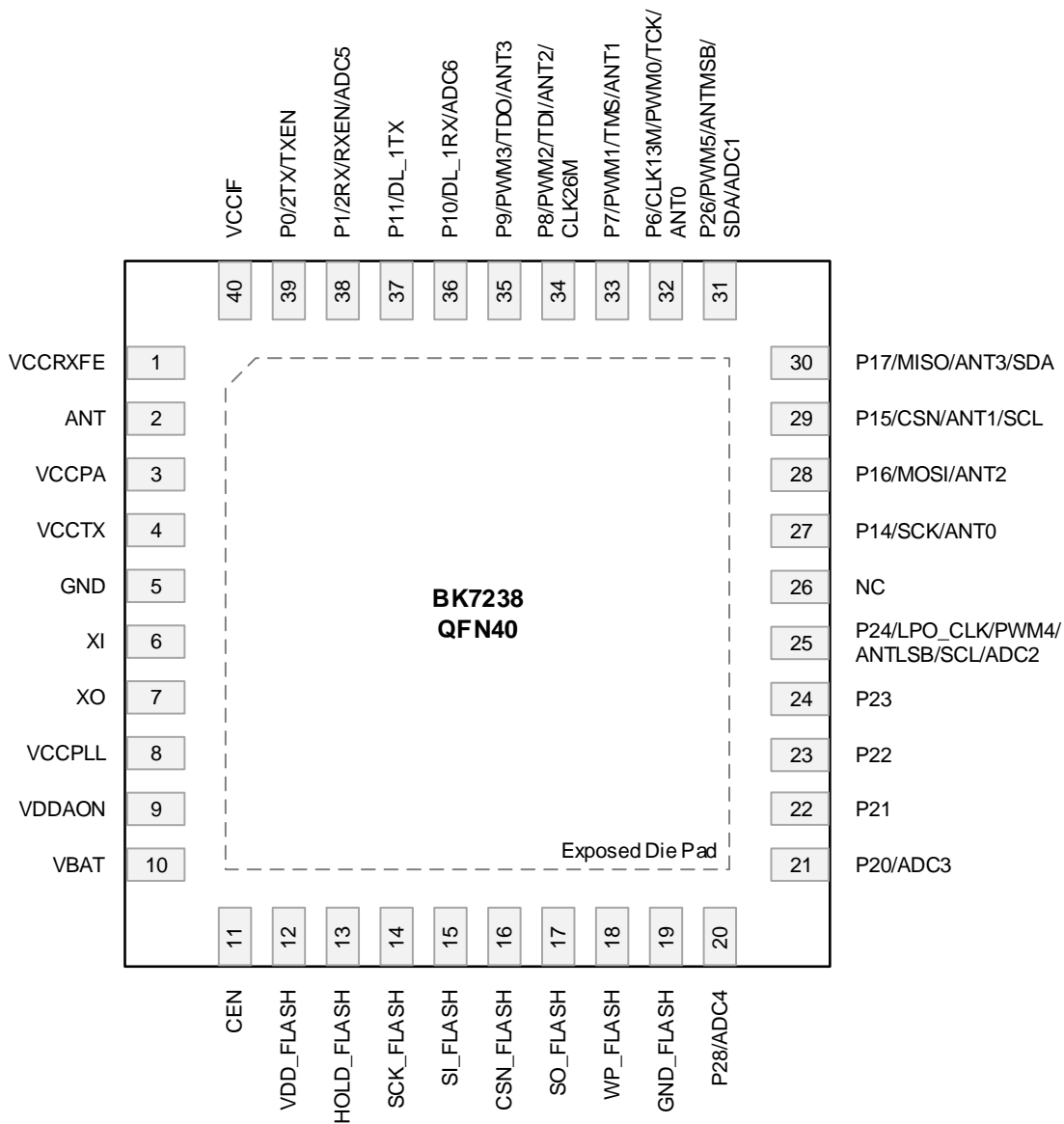


Table 3-1 shows the pin descriptions of the QFN40 package.

Table 3-1 QFN40 Pin Descriptions

Pin #	Name	I/O	Type	Description
1	VCCRxFE	-	Analog input	RF receiver power supply
2	ANT	-	RF	2.4 GHz RF signal port
3	VCCPA	-	Analog input	RF PA power supply
4	VCCTX	-	Analog input	RF transmitter power supply
5	GND	-	GND	Ground
6	XI	-	Analog input	26 MHz crystal input
7	XO	-	Analog output	26 MHz crystal output
8	VCCPLL	-	Analog input	RF PLL power supply
9	VDDAON	-	Analog output	Always-on digital LDO output
10	VBAT	-	Analog input	Chip power supply
11	CEN	-	Analog input	Chip enable, active high
12	VDD_FLASH	-	Analog output	External flash power supply
13	HOLD_FLASH	-	Digital input	External flash hold input
14	SCK_FLASH	-	Digital input	External flash clock input
15	SI_FLASH	-	Digital input	External flash data input
16	CSN_FLASH	-	Digital input	External flash chip select input
17	SO_FLASH	-	Digital output	External flash data output
18	WP_FLASH	-	Digital input	External flash write protect
19	GND_FLASH	-	GND	Ground
20	P28/ADC4	I/O	Digital/Analog	<ul style="list-style-type: none"> GPIO28 ADC4
21	P20/ADC3	I/O	Digital/Analog	<ul style="list-style-type: none"> GPIO20 ADC3
22	P21	I/O	Digital	GPIO21
23	P22	I/O	Digital	GPIO22
24	P23	I/O	Digital	GPIO23

Pin #	Name	I/O	Type	Description
25	P24/LPO_CLK/PWM4/ANTLSB/SCL/ADC2	I/O	Digital/Analog	<ul style="list-style-type: none"> GPIO24 32 kHz clock output PWM4 (differential with PWM5) Bluetooth LE antenna select (LSB) I2C: SCL ADC2
26	NC	-	NC	No connect
27	P14/SCK/ANT0	I/O	Digital	<ul style="list-style-type: none"> GPIO14 SPI: SCK Bluetooth LE antenna select 0
28	P16/MOSI/ANT2	I/O	Digital	<ul style="list-style-type: none"> GPIO16 SPI: MOSI Bluetooth LE antenna select 2
29	P15/CSN/ANT1/SCL	I/O	Digital	<ul style="list-style-type: none"> GPIO15 SPI: CSN Bluetooth LE antenna select 1 I2C: SCL
30	P17/MISO/ANT3/SDA	I/O	Digital	<ul style="list-style-type: none"> GPIO17 SPI: MISO Bluetooth LE antenna select 3 I2C: SDA
31	P26/PWM5/ANTMSB/SDA/ADC1	I/O	Digital/Analog	<ul style="list-style-type: none"> GPIO26 PWM5 (differential with PWM4) Bluetooth LE antenna select (MSB) I2C: SDA ADC1
32	P6/CLK13M/PWM0/TCK/ANT0	I/O	Digital	<ul style="list-style-type: none"> GPIO6 26 MHz clock output (divide by 1/2/4/8) PWM0 (differential with PWM1) JTAG: TCK Bluetooth LE antenna select 0
33	P7/PWM1/TMS/ANT1	I/O	Digital	<ul style="list-style-type: none"> GPIO7 PWM1 (differential with PWM0)

Pin #	Name	I/O	Type	Description
				<ul style="list-style-type: none"> JTAG: TMS Bluetooth LE antenna select 1
34	P8/PWM2/TDI/ANT2/CLK26M	I/O	Digital	<ul style="list-style-type: none"> GPIO8 PWM2 (differential with PWM3) JTAG: TDI Bluetooth LE antenna select 2 26 MHz clock output
35	P9/PWM3/TDO/ANT3	I/O	Digital	<ul style="list-style-type: none"> GPIO9 PWM3 (differential with PWM2) JTAG: TDO Bluetooth LE antenna select 3
36	P10/DL_1RX/ADC6	I/O	Digital/Analog	<ul style="list-style-type: none"> GPIO10 UART1: RX (Flash download support) ADC6
37	P11/DL_1TX	I/O	Digital	<ul style="list-style-type: none"> GPIO11 UART1: TX (Flash download support)
38	P1/2RX/RXEN/ADC5	I/O	Digital/Analog	<ul style="list-style-type: none"> GPIO1 UART2: RX RX enable ADC5
39	P0/2TX/TXEN	I/O	Digital	<ul style="list-style-type: none"> GPIO0 UART2: TX TX enable
40	VCCIF	-	Analog input	IF power supply
Die pad	GND_SLUG	-	GND	Ground

3.2 QFN32 Pin Description

Figure 3-2 shows the pin assignments of the 4 x 4 mm, 32-pin QFN package.

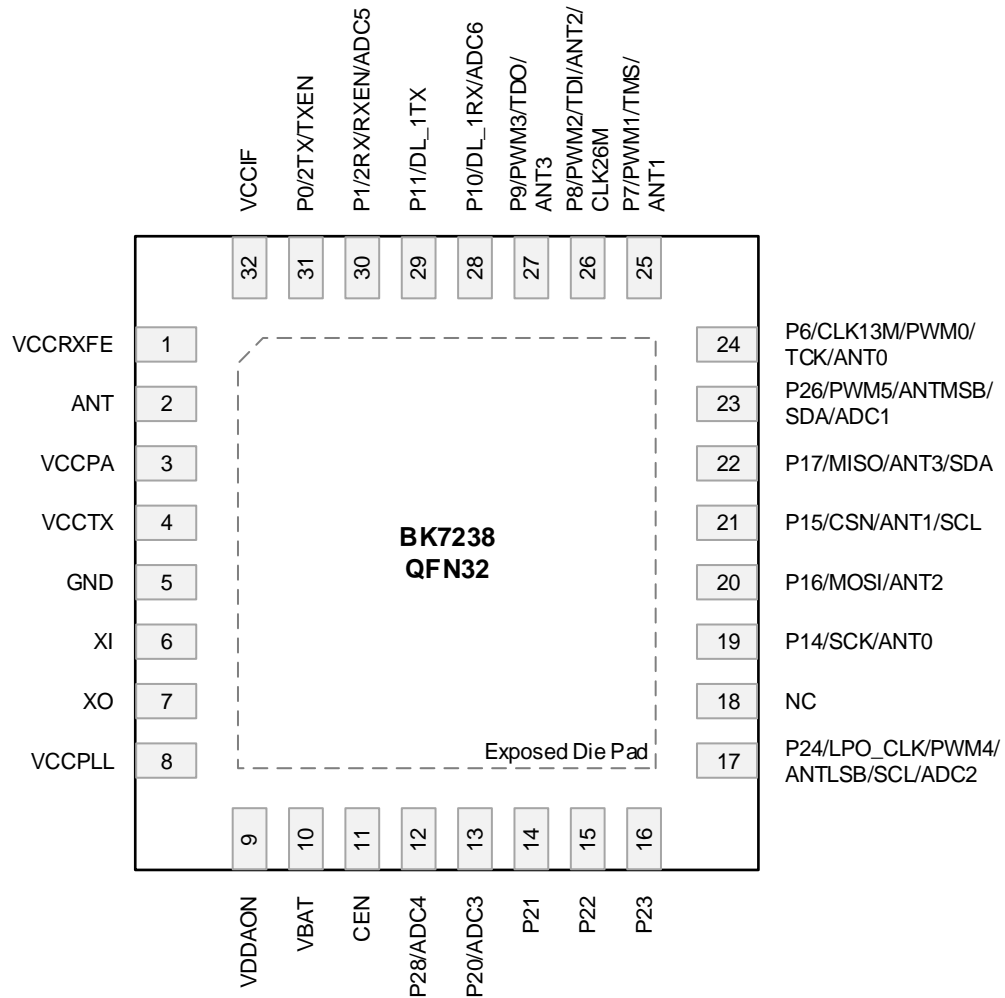
Figure 3-2 QFN32 Pin Assignments


Table 3-2 shows the pin descriptions of the QFN32 package.

Table 3-2 QFN32 Pin Descriptions

Pin #	Name	I/O	Type	Description
1	VCCRFXFE	-	Analog input	RF receiver power supply
2	ANT	-	RF	2.4 GHz RF signal port
3	VCCPA	-	Analog input	RF PA power supply
4	VCCTX	-	Analog input	RF Transmitter power supply
5	GND	-	GND	Ground
6	XI	-	Analog input	26 MHz crystal input
7	XO	-	Analog output	26 MHz crystal output



Pin #	Name	I/O	Type	Description
8	VCCPLL	-	Analog input	RF PLL power supply
9	VDDAON	-	Analog output	Always-on digital LDO output
10	VBAT	-	Analog input	Chip power supply
11	CEN	-	Analog input	Chip enable, active high
12	P28/ADC4	I/O	Digital/Analog	<ul style="list-style-type: none"> GPIO28 ADC4
13	P20/ADC3	I/O	Digital/Analog	<ul style="list-style-type: none"> GPIO20 ADC3
14	P21	I/O	Digital	GPIO21
15	P22	I/O	Digital	GPIO22
16	P23	I/O	Digital	GPIO23
17	P24/LPO_CLK/PWM4/ANTLSB/SCL/ADC2	I/O	Digital/Analog	<ul style="list-style-type: none"> GPIO24 32 kHz clock output PWM4 (differential with PWM5) Bluetooth LE antenna select (LSB) I2C: SCL ADC2
18	NC	-	NC	No connect
19	P14/SCK/ANT0	I/O	Digital	<ul style="list-style-type: none"> GPIO14 SPI: SCK Bluetooth LE antenna select 0
20	P16/MOSI/ANT2	I/O	Digital	<ul style="list-style-type: none"> GPIO16 SPI: MOSI Bluetooth LE antenna select 2
21	P15/CSN/ANT1/SCL	I/O	Digital	<ul style="list-style-type: none"> GPIO15 SPI: CSN Bluetooth LE antenna select 1 I2C: SCL
22	P17/MISO/ANT3/SDA	I/O	Digital	<ul style="list-style-type: none"> GPIO17 SPI: MISO Bluetooth LE antenna select 3 I2C: SDA

Pin #	Name	I/O	Type	Description
23	P26/PWM5/ANTMSB/SDA/ADC1	I/O	Digital/Analog	<ul style="list-style-type: none"> GPIO26 PWM5 (differential with PWM4) Bluetooth LE antenna select (MSB) I2C: SDA ADC1
24	P6/CLK13M/PWM0/TCK/ANT0	I/O	Digital	<ul style="list-style-type: none"> GPIO6 26 MHz clock output (divide by 1/2/4/8) PWM0 (differential with PWM1) JTAG: TCK Bluetooth LE antenna select 0
25	P7/PWM1/TMS/ANT1	I/O	Digital	<ul style="list-style-type: none"> GPIO7 PWM1 (differential with PWM0) JTAG: TMS Bluetooth LE antenna select 1
26	P8/PWM2/TDI/ANT2/CLK26M	I/O	Digital	<ul style="list-style-type: none"> GPIO8 PWM2 (differential with PWM3) JTAG: TDI Bluetooth LE antenna select 2 26 MHz clock output
27	P9/PWM3/TDO/ANT3	I/O	Digital	<ul style="list-style-type: none"> GPIO9 PWM3 (differential with PWM2) JTAG: TDO Bluetooth LE antenna select 3
28	P10/DL_1RX/ADC6	I/O	Digital/Analog	<ul style="list-style-type: none"> GPIO10 UART1: RX (Flash download support) ADC6
29	P11/DL_1TX	I/O	Digital	<ul style="list-style-type: none"> GPIO11 UART1: TX (Flash download support)
30	P1/2RX/RXEN/ADC5	I/O	Digital/Analog	<ul style="list-style-type: none"> GPIO1 UART2: RX RX enable ADC5

Pin #	Name	I/O	Type	Description
31	P0/2TX/TXEN	I/O	Digital	<ul style="list-style-type: none"> GPIO0 UART2: TX TX enable
32	VCCIF	-	Analog input	IF power supply
Die pad	GND_SLUG	-	GND	Ground

3.3 QFN20 Pin Description

Figure 3-3 shows the pin assignments of the 3 x 3 mm, 20-pin QFN package.

Figure 3-3 QFN20 Pin Assignments

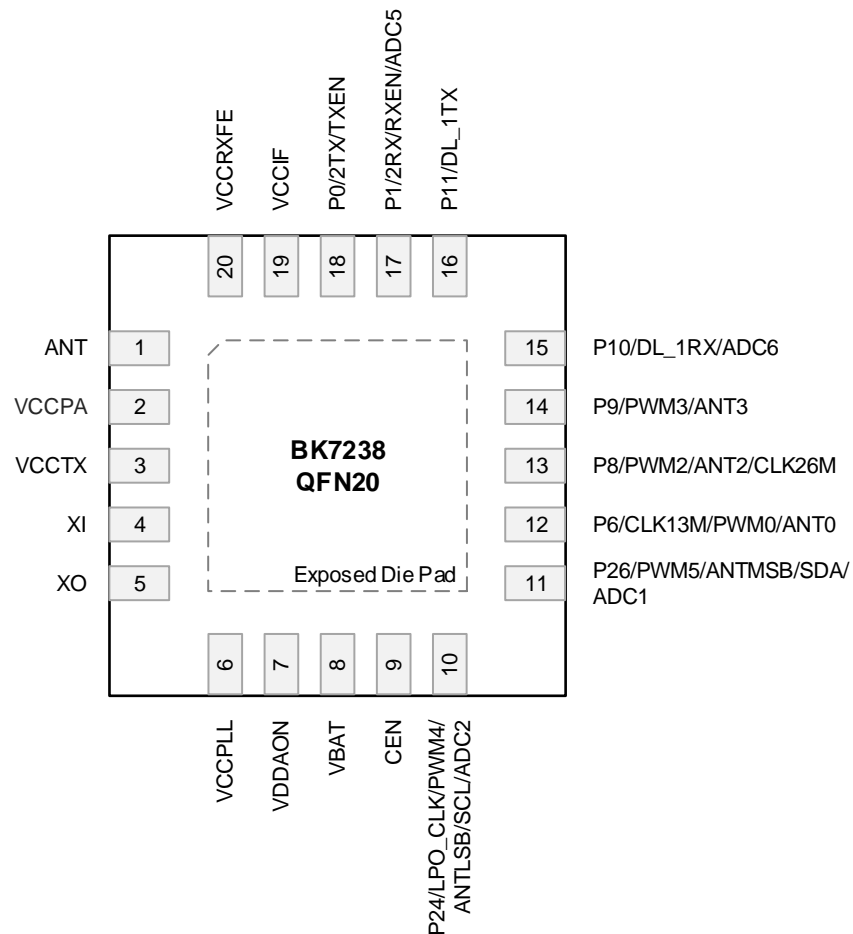


Table 3-3 shows the pin descriptions of the QFN20 package.

Table 3-3 QFN20 Pin Descriptions

Pin #	Name	I/O	Type	Description
1	ANT	-	RF	2.4 GHz RF signal port
2	VCCPA	-	Analog input	RF PA power supply
3	VCCTX	-	Analog input	RF Transmitter power supply
4	XI	-	Analog input	26 MHz crystal input
5	XO	-	Analog output	26 MHz crystal output
6	VCCPLL	-	Analog input	RF PLL power supply
7	VDDAON	-	Analog output	Always-on digital LDO output
8	VBAT	-	Analog input	Chip power supply
9	CEN	-	Analog input	Chip enable, active high
10	P24/LPO_CLK/PWM4/ANTLSB /SCL/ADC2	I/O	Digital/Analog	<ul style="list-style-type: none"> GPIO24 32 kHz clock output PWM4 (differential with PWM5) Bluetooth LE antenna select (LSB) I2C: SCL ADC2
11	P26/PWM5/ANTMSB/SDA/ ADC1	I/O	Digital/Analog	<ul style="list-style-type: none"> GPIO26 PWM5 (differential with PWM4) Bluetooth LE antenna select (MSB) I2C: SDA ADC1
12	P6/CLK13M/PWM0/ANT0	I/O	Digital	<ul style="list-style-type: none"> GPIO6 26 MHz clock output (divided by 1/2/4/8) PWM0 Bluetooth LE antenna select 0
13	P8/PWM2/ANT2/CLK26M	I/O	Digital	<ul style="list-style-type: none"> GPIO8 PWM2 (differential with PWM3) Bluetooth LE antenna select 2 26 MHz clock output
14	P9/PWM3/ANT3	I/O	Digital	<ul style="list-style-type: none"> GPIO9 PWM3 (differential with PWM2)



Pin #	Name	I/O	Type	Description
				<ul style="list-style-type: none">Bluetooth LE antenna select 3
15	P10/DL_1RX/ADC6	I/O	Digital/Analog	<ul style="list-style-type: none">GPIO10UART1: RX (Flash download support)ADC6
16	P11/DL_1TX	I/O	Digital	<ul style="list-style-type: none">GPIO11UART1: TX (Flash download support)
17	P1/2RX/RXEN/ADC5	I/O	Digital/Analog	<ul style="list-style-type: none">GPIO1UART2: RXRX enableADC5
18	P0/2TX/TXEN	I/O	Digital	<ul style="list-style-type: none">GPIO0UART2: TXTX enable
19	VCCIF	-	Analog input	IF power supply
20	VCCRFE	-	Analog input	RF receiver power supply
Die pad	GND_SLUG	-	GND	Ground

4. Functional Description

4.1 WLAN/Bluetooth Transceiver

The BK7238 integrates a high-performance WLAN/Bluetooth transceiver. The incorporated low noise amplifier (LNA) amplifies the single-ended input and converts the amplified signal into a differential output for a better noise and linearity trade-off. On the transmit side, the differential outputs of the power amplifier (PA) are combined and converted to single-ended outputs using the on-chip balun, enabling transmit and receive operations with only one ANT pin connected to the antenna. The communication range can be extended by configuring GPIO0 and GPIO1 as TXEN and RXEN function to control external PA and LNA. The frequency synthesizer is fully integrated, eliminating the need for any external components.

4.2 Power Management

4.2.1 Power Modes

The BK7238 supports four low-power modes except active mode, namely shutdown mode, deep sleep mode, low-voltage sleep mode, and normal sleep mode, where shutdown mode has the lowest power consumption.

Shutdown Mode: All circuits are powered off. A high level on the CEN pin will take the system to active mode.

Deep Sleep Mode: All circuits are powered off except the always-on (AON) logic. A GPIO interrupt or an RTC interrupt can power up the system again. Retention registers can keep their contents.

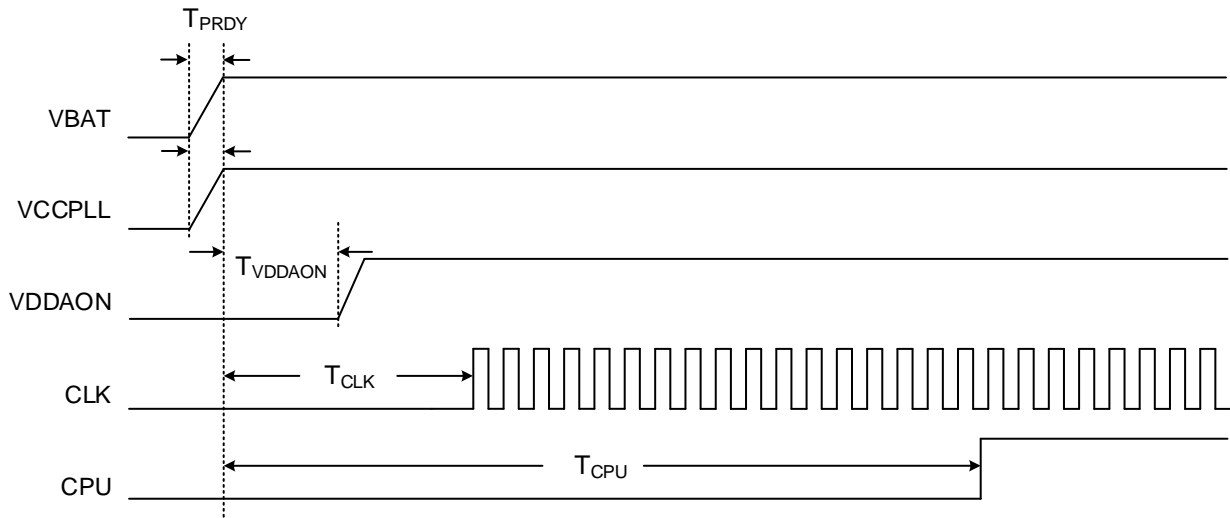
Low-voltage Sleep Mode: The MCU and all digital logic stop their clocks, and their power supply decreases to a much lower retention voltage, which results in a much lower current. A GPIO interrupt or an RTC interrupt can bring the system back to active mode with normal voltage.

Normal Sleep Mode: The MCU stops running, and all peripheral interrupts can resume the MCU.

Active Mode: The MCU is active, and all peripherals are available.

4.2.2 Power-up Sequence

Figure 4-1 shows the power-up sequence of BK7238.

Figure 4-1 BK7238 Power-up Sequence

Table 4-1 Timing Parameters of BK7238 Power-up Sequence

Parameter	Description	Min.	Typ.	Max.	Unit
T_{PRDY}	VBAT ready time	-	0.5	1.5	ms
T_{VDDAON}	Always-on digital LDO output ready time	-	0.5	1.5	ms
T_{CLK}	26 MHz clock stable time	-	3	5	ms
T_{CPU}	Application ready time	60	70	-	ms

4.3 Clock Management

The primary clock sources available in the BK7238 are as follows:

- High-frequency clocks
 - 26 MHz crystal oscillator (XTALH)
 - 26–160 MHz internal digitally controlled oscillator (DCO), about $\pm 2\%$ variation after calibration
 - 480 MHz digital PLL (DPLL)
- Low-frequency clock
 - 32 kHz internal ring oscillator (ROSC), about $\pm 2\%$ variation after calibration

The system generates a low-power clock source LPO_CLK for standby. The LPO_CLK can be selected from the following clocks:

- 32 kHz clock signal derived from 26 MHz crystal oscillator

- 32 kHz internal oscillator ROSC

The clock selection options for MCU and peripherals are listed as follows.

Table 4-2 Clock Selection

MCU and Peripherals	XTALH	DCO	DPLL	LPO_CLK
MCU	√	√	√	√
FLASH controller	√	√	√	
SPI	√	√		
UART1	√	√		
UART2	√	√		
I2C	√	√		
PWM	√	√		√
AUX ADC	√	√		
TIMG1	√			
TIMG2				√
Watchdog timer				√
RTC				√

The BK7238 also has clock output capability to output clock signals to external components. GPIOs can output the following clock signals:

- LPO_CLK: low-power LPO_CLK clock
- CLK13M: clock derived from high-frequency crystal clock (factor 1/2/4/8)
- CLK26M: high-frequency crystal clock, generally 26 MHz

4.4 Reset

A reset can be triggered by the following sources: power-on reset, brown-out reset, watchdog reset, software reset, and wake-up from shutdown mode or deep sleep mode.

System power-on and watchdog resets have the same reset effect on major blocks, except for the always-on logic. Any of these two resets can reset the whole chip to its initial state. The always-on logic has a 32-bit timer and 16-bit retention registers, which can only be reset to initial values by a system power-on reset. The watchdog reset can also reset the 32-bit timer of the always-on logic.

Wake-up from either shutdown mode or deep sleep mode will power on digital from power-down mode, which triggers the whole system reset procedure.

4.5 General-purpose I/Os (GPIO)

The BK7238 has up to 19 GPIOs, which can be configured as either input or output. Most GPIOs are shared with alternate functions.

The main features of GPIOs include:

- Push-pull
- Internal pull-up/down resistors
- Configurable drive strength
- Alternate function
- Interrupt generation:
 - High or low level
 - Rising or falling edge

4.6 SPI Interface (SPI)

The BK7238 integrates an SPI interface that can operate in master or slave mode. The SPI interface allows a clock frequency up to 30 MHz in master mode and 20 MHz in slave mode.

The SPI interface supports the following features:

- 4-wire or 3-wire full-duplex synchronous communication
- Configurable 8-bit or 16-bit data width
- Programmable clock polarity and phase
- Programmable data order with MSB-first or LSB-first shifting
- A 64-depth RX FIFO and a 64-depth TX FIFO with DMA capability

4.7 UART Interface (UART)

The BK7238 includes two universal asynchronous receiver/transmitter (UART) interfaces, which support full-duplex, asynchronous serial communication at a baud rate up to 6 Mbps.

The UART interfaces offer the features below:

- Configurable data length (5, 6, 7, or 8 bits)

- Even, odd, or none parity check
- Programmable stop bits (1 or 2 bits)
- Each UART embeds a 128-byte TX FIFO and a 128-byte RX FIFO. FIFO mode is disabled by default and can be enabled by software.
- Flash download (UART1)

4.8 I2C Interface (I2C)

I2C is a popular inter-IC interface that requires only two bus lines, the serial data line (SDA) and the serial clock line (SCL). The BK7238 embeds an I2C interface, which can operate in master or slave mode.

The features of the I2C interface are listed below:

- Master and slave modes
- Standard mode (up to 100 kbps)
- Fast mode (up to 400 kbps)
- 7-bit and 10-bit addressing
- Bus idle and SCL low timeout condition detection

4.9 GDMA Controller (GDMA)

The BK7238 has a general-purpose DMA controller (GDMA) with six DMA channels to unload CPU activity. The six channels are shared by peripherals that have DMA capabilities.

The GDMA controller can perform single block transfers and repeated block transfers. Data width for destination and source can be configured as 8 bits (byte), 16 bits (half-word), or 32 bits (word). It allows peripheral to memory, memory to memory, and memory to peripheral data transfers at a high speed.

The peripherals with DMA capabilities on the BK7238 includes UART1, UART2, and SPI.

4.10 PWM

The BK7238 has three 32-bit PWM pairs labeled PWM0/1, PWM2/3, and PWM4/5. Each PWM pair consists of two 32-bit up counters driven by an 8-bit programmable prescaler.

Each channel can work independently (arbitrary waveform configuration), or two channels can be paired (waveforms completely opposite, timing aligned).

When any of the six PWM pins, GPIO6, GPIO7, GPIO8, GPIO9, GPIO24, and GPIO28 is configured as PWM output, the output source can be select from any of the six PWM channels.

The PWM features are listed here:

- 32-bit up counter
- The counter increases in one direction and automatically continues counting from 0 when it overflows to the maximum value.
- Fixed PWM base frequency with 8-bit programmable prescaler (factor between 1 and 256)
- Six channels, each supports four modes:
 - PWM mode
 - Timer mode
 - Counter mode
 - Capture mode
- Each channel can be enabled individually, and the mode of each channel can be configured individually.
- Configurable PWM period and duty cycle for each PWM channel
- Capable of continuously counting between two rising edges, two falling edges, or any two edges in Capture mode
- Real-time count value can be read in Timer mode.

4.11 Auxiliary ADC (AUX ADC)

The auxiliary ADC (AUX ADC) is a 10-bit successive approximation analog-to-digital converter. The AUX ADC has multiple external analog input channels and internal dedicated channels. The AUX ADC supports A/D conversion performed in one-shot, software control, or continuous mode.

The AUX ADC has the following features:

- Programmable sample rate from 5 kHz to 26 MHz
- 10-bit resolution
- Up to six external analog input channels: ADC1/2/3/4/5/6
- Four internal dedicated channels:
 - VBAT monitoring channel (VBAT/2), connected to ADC0
 - Internal temperature sensor (TEMP), connected to ADC7
 - TSSIO, connected to ADC8
 - Internal debug channel, connected to ADC9
- Conversion modes:

- One-shot mode
- Software control mode
- Continuous mode

4.12 Timer Group (TIMG)

The BK7238 includes two general-purpose timer groups (TIMG). Each group has three 32-bit timers. Each group consists of three 32-bit counters driven by a 4-bit prescaler.

Each TIMG module has the following features:

- Three timers (Timer0/1/2)
- Three 32-bit up counters
- 4-bit prescaler, factor between 1 and 16
- Capable of reading the real-time value of the counter

4.13 Watchdog Timer (WDT)

The purpose of the watchdog timer is to detect and recover from failures or malfunctions. It triggers a reset on expiry of a specified time period.

The watchdog timer runs on the 32 kHz LPO_CLK clock and has a maximum programmable period of up to 65.536 ($2^{16}/1$ kHz) seconds.

4.14 Real-time counter (RTC)

The real-time counter (RTC) is a 32-bit counter that can be used as a wake-up source to wake up the system from low-voltage sleep or deep sleep mode. The RTC runs on the ROSC, and it can keep running even when the system is in low-voltage sleep or deep sleep mode.

4.15 Temperature Sensor

The BK7238 integrates an on-chip temperature sensor. The temperature sensor can measure on-chip temperature over -40 to +125 °C with an accuracy of ± 5 °C. The digital results can be read by the ADC.

Usually, the software initiates the calibration of a specific module based on the temperature value, narrowing the difference in chip performance at different temperatures. The host can also read the on-chip temperature and decide whether to reduce transmit power or suspend operation at high temperatures.



4.16 True Random Number Generator (TRNG)

The random number generator module generates true, nondeterministic random numbers based on thermal noise for the purpose of creating keys, initialization vectors, and nonces needed for cryptographic operations.

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute-maximum-rated conditions for prolonged periods may affect the reliability of the device.

Parameter	Description	Min.	Max.	Unit
V _{BAT}	Battery regulator supply voltage	-0.3	3.6	V
P _{RX}	RX input power	-	10	dBm
T _{STR}	Storage temperature range	-55	150	°C

5.2 ESD Ratings

Parameter	Description	Test Condition	Value	Unit
ESD HBM	Electrostatic discharge voltage (human body model), per ANSI/ESDA/JEDEC JS-001-2017	ANT pin	±2000	V
		VCCPA/VCCTX/XI pins	±3000	V
		Other pins	±4000	V
ESD CDM	Electrostatic discharge voltage (charge device model), per ANSI/ESDA/JEDEC JS-002-2018	All pins	±1000	V

5.3 Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
V _{BAT}	Battery/regulator supply voltage	2.7	-	3.6	V
V _{CCIF}	Supply voltage for IF	2.2	-	3.6	V
V _{CCR_{XFE}}	Supply voltage for RX	2.2	-	3.6	V
V _{CCPA}	Supply voltage for PA	2.7	-	3.6	V
V _{CC_{TX}}	Supply voltage for TX	2.7	-	3.6	V
V _{CCPLL}	Supply voltage for RF PLL	2.2	-	3.6	V

Parameter	Description	Min.	Typ.	Max.	Unit
VDDAON	Always-on digital LDO output voltage	0.5	0.9	1.0	V
VDD_FLASH	Supply voltage for external Flash	2.7	-	3.6	V

5.4 Digital I/O Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VIH	High-level input voltage	-	0.7 VBAT	-	VBAT + 0.3	V
VIL	Low-level input voltage	-	-0.3	-	0.3 VBAT	V
VOH	High-level output voltage	-	0.9 VBAT	-	-	V
VOL	Low-level output voltage	-	-	-	0.1 VBAT	V
IDRV	I/O output drive strength	-	5	-	20	mA
RPU	Weak pull-up resistor	-	-	48	-	kΩ
RPD	Weak pull-down resistor	-	-	48	-	kΩ

5.5 Digital LDO

Parameter	Description	Min.	Typ.	Max.	Unit
VDDAON	Always-on digital LDO output voltage	0.5	0.9	1.0	V
Load current	-	-	-	50	mA

5.6 26 MHz Crystal Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
F0	Nominal Frequency	-	-	26	-	MHz
ΔF/F0	Frequency tolerance	25 °C	-10	-	+10	ppm
TC	Frequency stability over operating temperature	-40 to 105 °C crystal	-20	-	+20	ppm
		-30 to 85 °C crystal	-10	-	+10	ppm
CL	Load capacitance	-	7	7.3	9	pF
TS	Trim sensitivity	-40 to 105 °C crystal	-	32	-	ppm/pF

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
		-30 to 85 °C crystal	-	17	-	ppm/pF

5.7 Current Consumption

Measured with T = 25 °C, VBAT = 3.0 V unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
Active Mode					
RX current	11 Mbps DSSS	-	30	-	mA
	54 Mbps OFDM	-	33	-	mA
	MCS7, HT20	-	33	-	mA
TX current	11 Mbps DSSS @ 17 dBm	-	265	-	mA
	54 Mbps OFDM @ 15 dBm	-	230	-	mA
	MCS7, HT20 @ 14 dBm	-	220	-	mA
Sleep Mode					
Normal sleep	-	-	300	-	μA
Low-voltage sleep	-	-	75	-	μA
Deep sleep	-	-	10	-	μA
Shutdown Mode					
Shutdown	-	-	0.5	-	μA

5.8 WLAN Receiver RF Characteristics

Measured with T = 25 °C, VBAT = 3.0 V unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
General					
Frequency range	-	2412	-	2484	MHz
Sensitivity					
Sensitivity - IEEE 802.11b (8% PER for 1024 octet PSDU)	1 Mbps DSSS	-	-99	-	dBm
	2 Mbps DSSS	-	-96	-	dBm

Parameter	Condition	Min.	Typ.	Max.	Unit
	5.5 Mbps DSSS	-	-94	-	dBm
	11 Mbps DSSS	-	-90	-	dBm
Sensitivity - IEEE 802.11g (10% PER for 1000 octet PSDU)	6 Mbps OFDM	-	-92	-	dBm
	9 Mbps OFDM	-	-92	-	dBm
	12 Mbps OFDM	-	-91	-	dBm
	18 Mbps OFDM	-	-89	-	dBm
	24 Mbps OFDM	-	-86	-	dBm
	36 Mbps OFDM	-	-82	-	dBm
	48 Mbps OFDM	-	-78	-	dBm
	54 Mbps OFDM	-	-76	-	dBm
Sensitivity - IEEE 802.11n, 20 MHz (10% PER for 4096 octet PSDU)	MCS0	-	-92	-	dBm
	MCS1	-	-90	-	dBm
	MCS2	-	-87	-	dBm
	MCS3	-	-84	-	dBm
	MCS4	-	-81	-	dBm
	MCS5	-	-77	-	dBm
	MCS6	-	-75	-	dBm
	MCS7	-	-74	-	dBm
Maximum Receive Level					
Maximum receive level @ 2.4 GHz	11b: 1, 2 Mbps (8% PER, 1024 octets)	-	-	10	dBm
	11b: 5.5, 11 Mbps (8% PER, 1024 octets)	-	-	10	dBm
	11g: 6–54 Mbps (10% PER, 1000 octets)	-	-	5	dBm
	11n: MCS0–7 (10% PER, 4096 octets)	-	-	2	dBm
Adjacent Channel Rejection					
Adjacent channel (± 30 MHz) rejection - IEEE 802.11b	1 Mbps DSSS	-74 dBm	-	51	dB

Parameter	Condition		Min.	Typ.	Max.	Unit
(8% PER for 1024 octet PSDU with desired signal level as specified in Condition)	2 Mbps DSSS	-74 dBm	-	48	-	dB
Adjacent channel (± 25 MHz) rejection - IEEE 802.11b (8% PER for 1024 octet PSDU with desired signal level as specified in Condition)	5.5 Mbps DSSS	-70 dBm	-	42	-	dB
	11 Mbps DSSS	-70 dBm	-	37	-	dB
Adjacent channel (± 25 MHz) rejection - IEEE 802.11g (10% PER for 1000 octet PSDU with desired signal level as specified in Condition)	6 Mbps OFDM	-79 dBm	-	42	-	dB
	54 Mbps OFDM	-62 dBm	-	30	-	dB
Adjacent channel (± 25 MHz) rejection - IEEE 802.11n (10% PER for 4096 octet PSDU with desired signal level as specified in Condition)	MCS0	-79 dBm	-	42	-	dB
	MCS7	-61 dBm	-	24	-	dB
Spurious Emissions						
Spurious emissions	< 1 GHz		-	-	-60	dBm
	> 1 GHz		-	-	-60	dBm

5.9 WLAN Transmitter RF Characteristics

Measured with $T = 25\text{ }^{\circ}\text{C}$, $V_{BAT} = 3.0\text{ V}$ unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
General					
Frequency range	-	2412	-	2484	MHz
TX power					
TX power - IEEE 802.11b (SEM compliant)	1 Mbps DSSS	-	19	-	dBm
	11 Mbps DSSS	-	19	-	dBm
TX power - IEEE 802.11g (EVM compliant)	6 Mbps OFDM	-	20	-	dBm
	54 Mbps OFDM	-	17	-	dBm
TX power - IEEE 802.11n	MCS0	-	19	-	dBm

Parameter	Condition	Min.	Typ.	Max.	Unit	
(EVM compliant)	MCS7	-	16	-	dBm	
Harmonic Level						
Harmonic level (at maximum output power)	4.8–5.0 GHz	2nd harmonic	-	-	-45	dBm
	7.2–7.5 GHz	3rd harmonic	-	-	-50	dBm
Spurious Emissions						
Spurious emissions (at maximum output power)	< 1 GHz	-	-	-50	dBm	
	> 1 GHz	-	-	-43	dBm	

5.10 Bluetooth LE Receiver RF Characteristics

Measured with T = 25 °C, VBAT = 3.0 V unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
General					
Frequency range	-	2402	-	2480	MHz
Bluetooth LE 1 Mbps					
Sensitivity	30.8% PER	-	-98	-	dBm
Maximum input level	30.8% PER	0	-	-	dBm
C/I co-channel	-	-	8	-	dB
C/I 1 MHz adjacent channel	-	-	0	-	dB
C/I -1 MHz adjacent channel	-	-	-1	-	dB
C/I 2 MHz adjacent channel	-	-	-29	-	dB
C/I -2 MHz adjacent channel	-	-	-30	-	dB
C/I 3 MHz adjacent channel	-	-	-30	-	dB
C/I -3 MHz adjacent channel	-	-	-29	-	dB
C/I > 3 MHz adjacent channel	-	-	-29	-	dB
C/I < -3 MHz adjacent channel	-	-	-30	-	dB
Out-of-band blocking	30–2000 MHz	-	-27	-	dBm
	2003–2399 MHz	-	-33	-	dBm

Parameter	Condition	Min.	Typ.	Max.	Unit
	2484–2997 MHz	-	-32	-	dBm
	3000 MHz–12.75 GHz	-	-10	-	dBm
Intermodulation	-	-	-38	-	dBm
Bluetooth LE 2 Mbps					
Sensitivity	30.8% PER	-	-95	-	dBm
Maximum input level	30.8% PER	0	-	-	dBm
C/I co-channel	-	-	8	-	dB
C/I 2 MHz adjacent channel	-	-	0	-	dB
C/I -2 MHz adjacent channel	-	-	-2	-	dB
C/I 4 MHz adjacent channel	-	-	-29	-	dB
C/I -4 MHz adjacent channel	-	-	-29	-	dB
C/I 6 MHz adjacent channel	-	-	-29	-	dB
C/I -6 MHz adjacent channel	-	-	-29	-	dB
C/I > 6 MHz adjacent channel	-	-	-30	-	dB
C/I < -6 MHz adjacent channel	-	-	-29	-	dB
Out-of-band blocking	30–2000 MHz	-	-28	-	dBm
	2003–2399 MHz	-	-33	-	dBm
	2484–2997 MHz	-	-29	-	dBm
	3000 MHz–12.75 GHz	-	-5	-	dBm
Intermodulation	-	-	-38	-	dBm
Bluetooth LE 125 kbps					
Sensitivity	30.8% PER	-	-104	-	dBm
Maximum input level	30.8% PER	0	-	-	dBm
C/I co-channel	-	-	1	-	dB
C/I 1 MHz adjacent channel	-	-	-3	-	dB
C/I -1 MHz adjacent channel	-	-	-4	-	dB
C/I 2 MHz adjacent channel	-	-	-31	-	dB
C/I -2 MHz adjacent channel	-	-	-34	-	dB

Parameter	Condition	Min.	Typ.	Max.	Unit
C/I 3 MHz adjacent channel	-	-	-34	-	dB
C/I -3 MHz adjacent channel	-	-	-41	-	dB
C/I > 3 MHz adjacent channel	-	-	-41	-	dB
C/I < -3 MHz adjacent channel	-	-	-41	-	dB
Bluetooth LE 500 kbps					
Sensitivity	30.8% PER	-	-101	-	dBm
Maximum input level	30.8% PER	0	-	-	dBm
C/I co-channel	-	-	4	-	dB
C/I 1 MHz adjacent channel	-	-	-2	-	dB
C/I -1 MHz adjacent channel	-	-	-3	-	dB
C/I 2 MHz adjacent channel	-	-	-31	-	dB
C/I -2 MHz adjacent channel	-	-	-33	-	dB
C/I 3 MHz adjacent channel	-	-	-32	-	dB
C/I -3 MHz adjacent channel	-	-	-34	-	dB
C/I > 3 MHz adjacent channel	-	-	-34	-	dB
C/I < -3 MHz adjacent channel	-	-	-34	-	dB

5.11 Bluetooth LE Transmitter RF Characteristics

Measured with T = 25 °C, VBAT = 3.0 V unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
General					
Frequency range	-	2402	-	2480	MHz
TX power	-	6	8	10	dBm
Bluetooth LE 1 Mbps					
In-band emissions	±2 MHz offset	-	-	-49	dBm
	±3 MHz offset	-	-	-50	dBm
	>±3 MHz offset	-	-	-51	dBm

Parameter		Condition	Min.	Typ.	Max.	Unit
Modulation characteristics	Δf_{1avg}	-	-	262	-	kHz
	Δf_{2max}	-	-	250	-	kHz
	$\Delta f_{2avg}/\Delta f_{1avg}$	-	-	0.9	-	-
Carrier frequency offset and drift	Max $ f_n _{n=0,1,2,3\dots k}$	-	-	8	-	kHz
	Max $ f_0 - f_n _{n=2,3,4\dots k}$	-	-	1.5	-	kHz
	$ f_1 - f_0 $	-	-	0.5	-	kHz
	Max $ f_n - f_{n-5} _{n=6,7,8\dots k}$	-	-	1.3	-	kHz/50 μ s
Bluetooth LE 2 Mbps						
In-band emissions	± 4 MHz offset	-	-	-52	-	dBm
	± 5 MHz offset	-	-	-52	-	dBm
	$> \pm 5$ MHz offset	-	-	-53	-	dBm
Modulation characteristics	Δf_{1avg}	-	-	522	-	kHz
	Δf_{2max}	-	-	502	-	kHz
	$\Delta f_{2avg}/\Delta f_{1avg}$	-	-	0.9	-	-
Carrier frequency offset and drift	Max $ f_n _{n=0,1,2,3\dots k}$	-	-	10	-	kHz
	Max $ f_0 - f_n _{n=2,3,4\dots k}$	-	-	1.2	-	kHz
	$ f_1 - f_0 $	-	-	0.5	-	kHz
	Max $ f_n - f_{n-5} _{n=6,7,8\dots k}$	-	-	0.9	-	kHz/50 μ s
Bluetooth LE 125 kbps						
In-band emissions	± 2 MHz offset	-	-	-49	-	dBm
	± 3 MHz offset	-	-	-50	-	dBm
	$> \pm 3$ MHz offset	-	-	-50	-	dBm
Modulation characteristics	Δf_{1avg}	-	-	261	-	kHz
	Δf_{1max}	-	-	245	-	kHz
Carrier frequency offset and drift	Max $ f_n _{n=0,1,2,3\dots k}$	-	-	10	-	kHz
	Max $ f_0 - f_n _{n=1,2,3\dots k}$	-	-	1	-	kHz

Parameter	Condition	Min.	Typ.	Max.	Unit	
	$ f_0 - f_3 $	-	-	1	-	kHz
	$ f_n - f_{n-3} $ n = 7, 8, 9...k	-	-	1	-	kHz/48 μ s
Bluetooth LE 500 kbps						
In-band emissions	± 2 MHz offset	-	-	-47	-	dBm
	± 3 MHz offset	-	-	-48	-	dBm
	$> \pm 3$ MHz offset	-	-	-50	-	dBm

5.12 AUX ADC Characteristics

Parameter	Condition	Min.	Typ.	Max.	Unit
Conversion clock	-	-	-	1.86	MHz
Conversion time	-	14	-	-	Cycle
V_{REF}	Internal	0.8	1.8	-	V
	External	-	V _{BAT} /2	-	V
Input voltage range	-	0	-	$V_{REF} * 2$	V
Input impedance	-	100	-	-	M Ω
Input capacitance (Cs)	-	-	1	-	pF
DNL	-	-1	-	0.5	LSB
INL	-	-2	-	2	LSB
ENOB	-	-	9.2	-	Bit
SNDR	-	-	57	-	dB
SFDR	-	-	61.4	-	dB
$T_{STARTUP}$	-	-	5	-	μ s
Current consumption	-	-	200	-	μ A

6. Package Information

6.1 QFN40 5 x 5 mm Package

Figure 6-1 QFN40 5 x 5 mm Package Outline

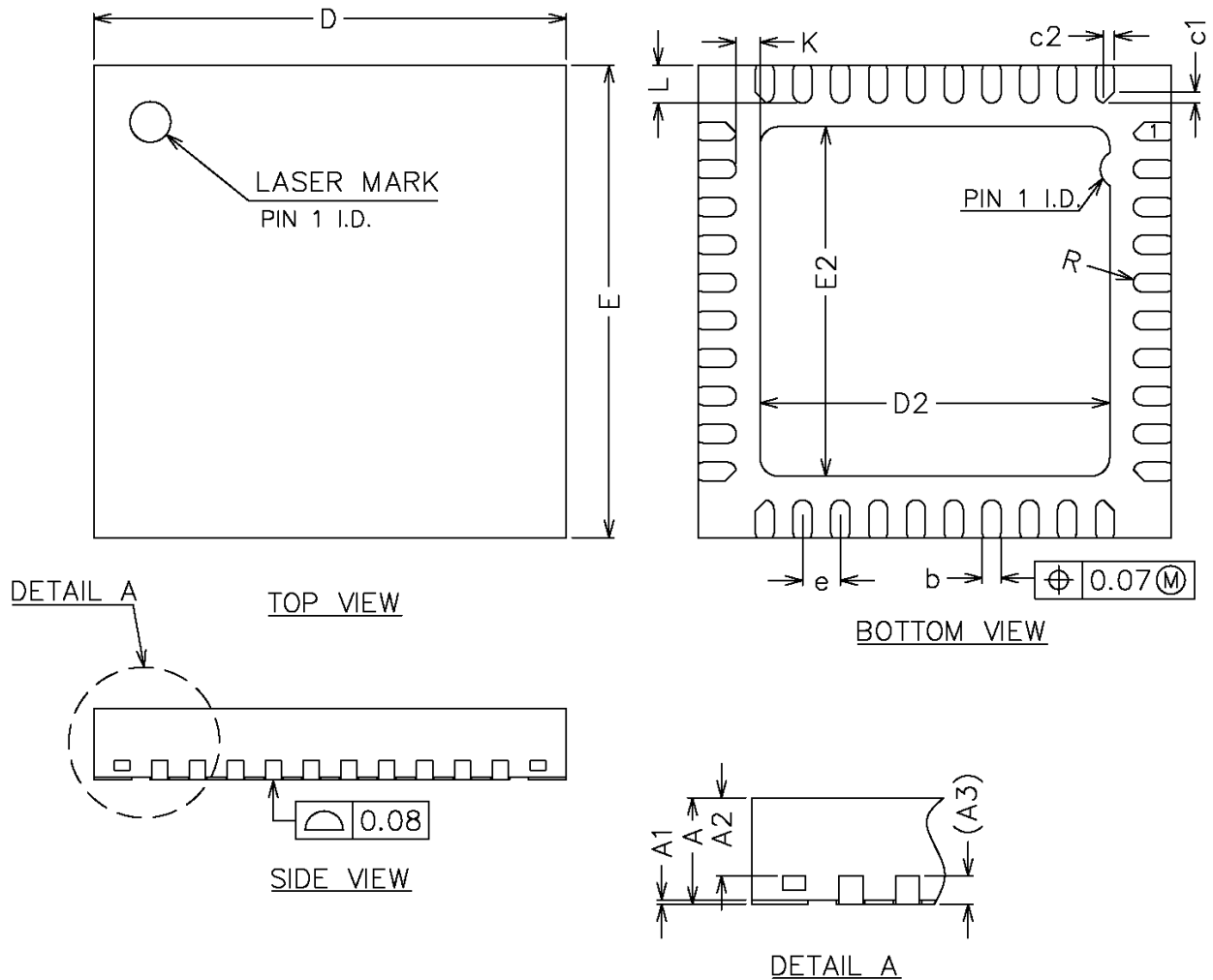


Table 6-1 QFN40 Package Dimensions

Symbol	Dimensions in Millimeters		
	Min.	Nom.	Max.
A	0.70	0.75	0.80



Symbol	Dimensions in Millimeters		
	Min.	Nom.	Max.
A1	0.00	0.02	0.05
A2	0.50	0.55	0.60
A3	0.20 REF		
b	0.15	0.20	0.25
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.60	3.70	3.80
E2	3.60	3.70	3.80
e	0.35	0.40	0.45
K	0.20	-	-
L	0.35	0.40	0.45
R	0.075	-	-
c1	-	0.12	-
c2	-	0.12	-

6.2 QFN32 4 x 4 mm Package

Figure 6-2 QFN32 4 x 4 mm Package Outline

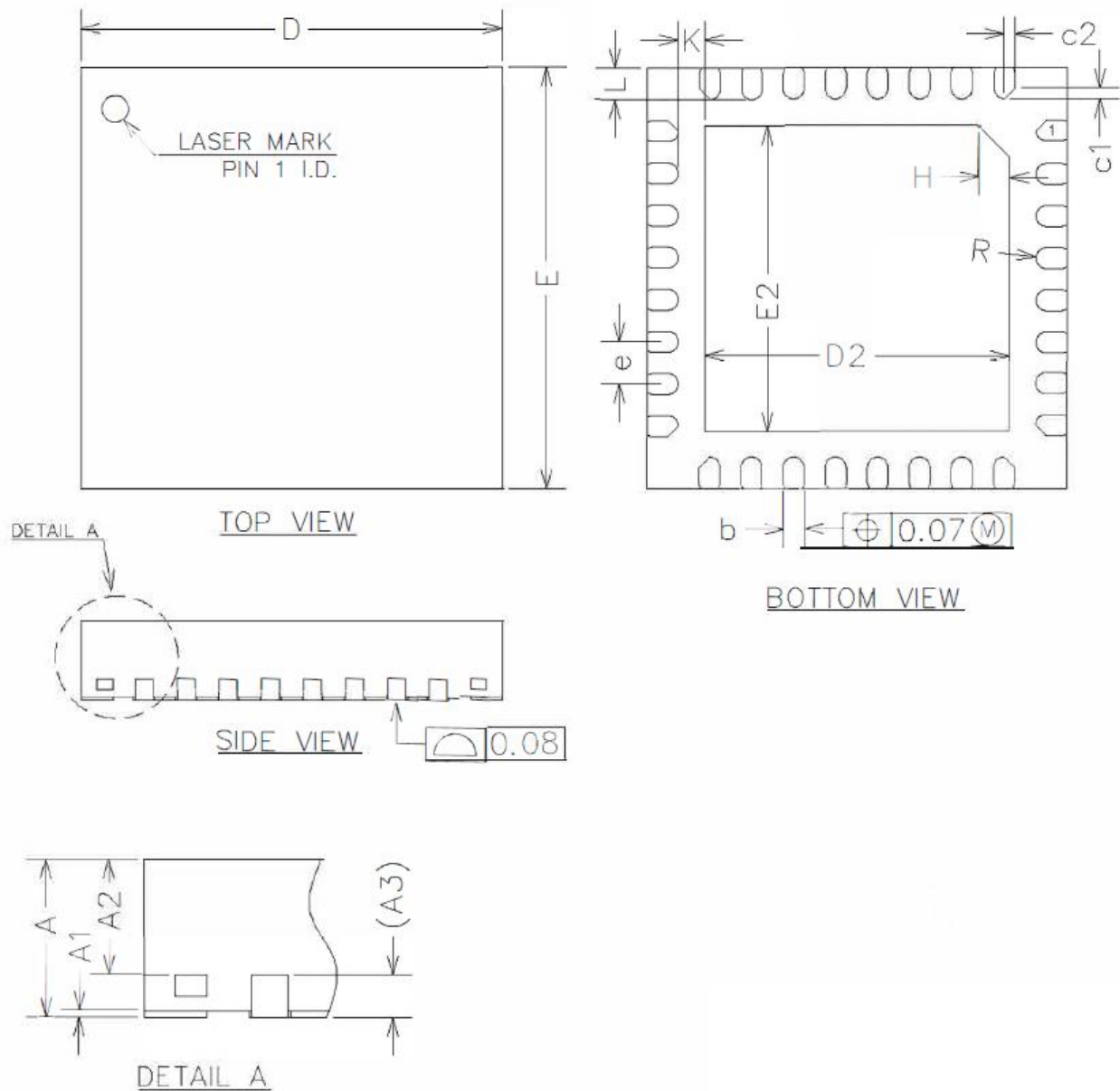


Table 6-2 QFN32 Package Dimensions

Symbol	Dimensions in Millimeters		
	Min.	Nom.	Max.
A	0.70	0.75	0.80



Symbol	Dimensions in Millimeters		
	Min.	Nom.	Max.
A1	0.00	0.02	0.05
A2	0.50	0.55	0.60
A3	0.20 REF		
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.80	2.90	3.00
E2	2.80	2.90	3.00
e	0.30	0.40	0.50
H	0.30 REF		
K	0.25 REF		
L	0.25	0.30	0.35
R	0.09	-	-
c1	-	0.10	-
c2	-	0.10	-

6.3 QFN20 3 x 3 mm Package

Figure 6-3 QFN20 3 x 3 mm Package Outline

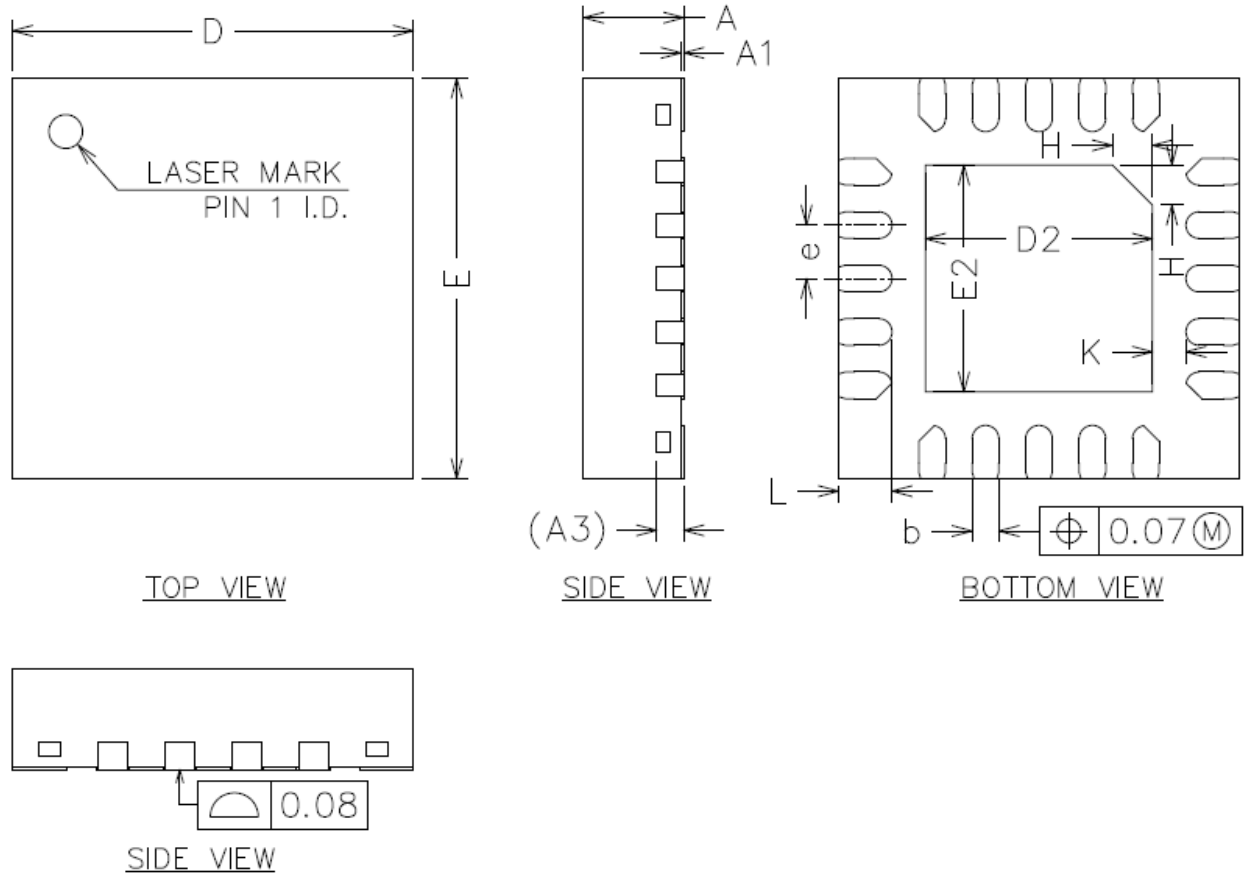


Table 6-3 QFN20 Package Dimensions

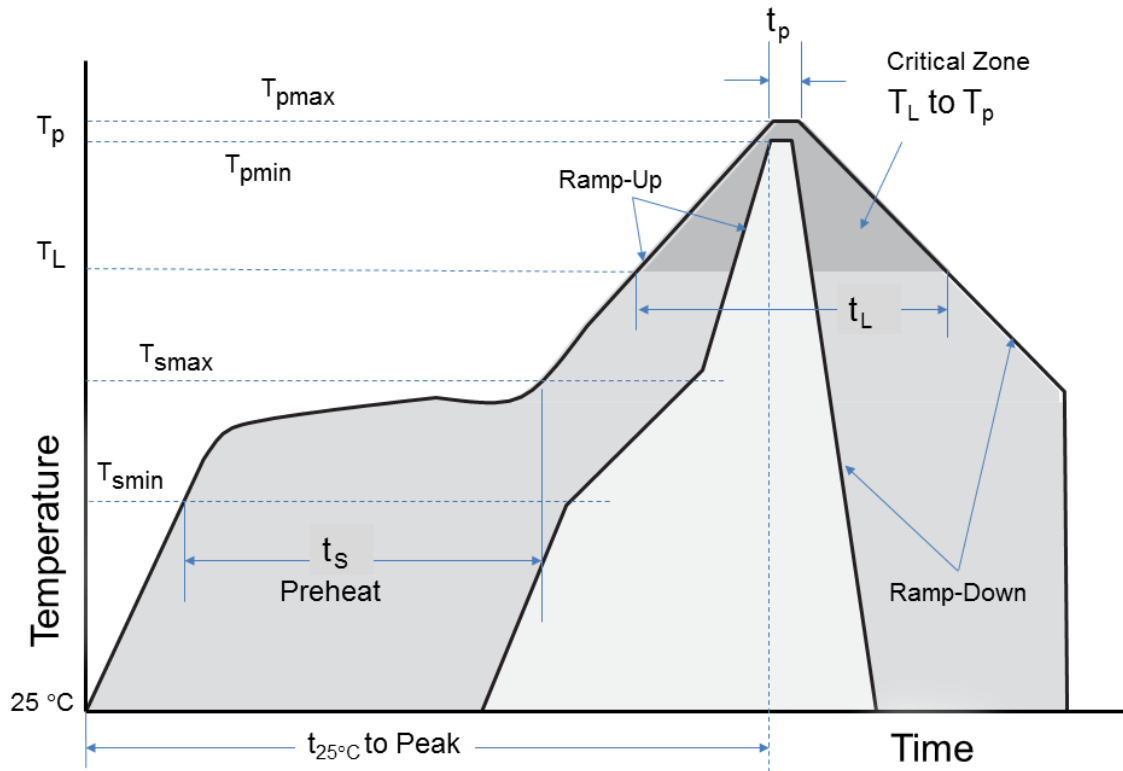
Symbol	Dimensions in Millimeters		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20 REF		
b	0.15	0.20	0.25
D	2.95	3.00	3.05
E	2.95	3.00	3.05
D2	1.65	1.70	1.75



Symbol	Dimensions in Millimeters		
	Min.	Nom.	Max.
E2	1.65	1.70	1.75
e	0.30	0.40	0.50
H	0.30 REF		
K	0.15	-	-
L	0.35	0.40	0.45

7. Reflow Soldering Profile

Figure 7-1 Reflow Soldering Profile



Profile Feature		Specification
Average ramp-up rate (T_{smax} to T_p)		3 $^{\circ}\text{C/s}$ max.
Preheat	Temperature min. (T_{smin})	150 $^{\circ}\text{C}$
	Temperature max. (T_{smax})	200 $^{\circ}\text{C}$
	Time (t_s)	60 s to 180 s
Time maintained above	Temperature (T_L)	217 $^{\circ}\text{C}$
	Time (t_L)	60 s to 150 s
Peak/classification temperature (T_p)		260 $^{\circ}\text{C}$
Time within 5 $^{\circ}\text{C}$ of actual peak temperature (t_p)		20 s to 40 s

Profile Feature	Specification
Ramp-down rate	6 °C/s max.
Time 25 °C to peak temperature	8 minutes max.

RoHS Compliant

The product does not contain lead, mercury, cadmium, hexavalent chromium, PBB&PBDE content in accordance with directive 2002/95/EC (RoHS).

ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electricity. Proper ESD techniques should be used when handling these devices.



Moisture Sensitivity Level

The product is qualified to moisture sensitivity level MSL3 in accordance with IPC/JEDEC J-STD-020.

8. Ordering Information

Figure 8-1 Part Number Scheme

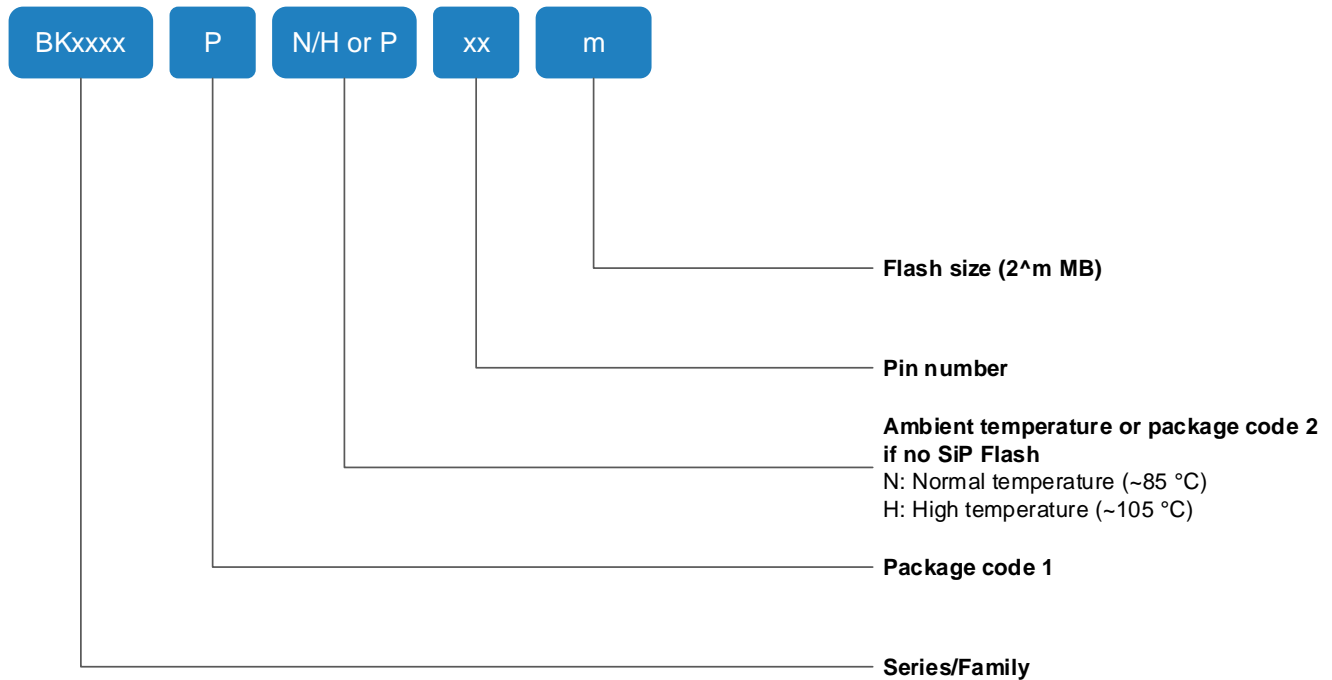


Table 8-1 Ordering Information

Ordering Code	Package	SiP ^a Flash	Ambient Temp	Packing	Minimum Ordering Qty (MOQ)
BK7238QN40	5 mm x 5 mm QFN40	-	-40 to +105 °C	Tape and Reel	3000
BK7238QH320	4 mm x 4 mm QFN32	1 MB	-40 to +105 °C	Tape and Reel	3000
BK7238QH200	3 mm x 3 mm QFN20	1 MB	-40 to +105 °C	Tape and Reel	6000
BK7238QN321	4 mm x 4 mm QFN32	2 MB	-40 to +85 °C	Tape and Reel	3000
BK7238QH321	4 mm x 4 mm QFN32	2 MB	-40 to +105 °C	Tape and Reel	3000
BK7238QN201	3 mm x 3 mm QFN20	2 MB	-40 to +85 °C	Tape and Reel	6000
BK7238QH201	3 mm x 3 mm QFN20	2 MB	-40 to +105 °C	Tape and Reel	6000

a. A system in a package (SiP) refers to Flash enclosed in the package.

Revision History

Version	Date	Description
0.1	2021/11/2	Initial release. First version of the preliminary specification.
0.2	2022/2/18	<p>Added documentation for QFN32 package and general wording update:</p> <ul style="list-style-type: none"> • Added and updated features in Section 1 Features • Updated Figure 2-1 and added Table 2-1 in Section 2 Overview • Added Section 3.2 QFN32 Pin Description • Changed the pin name of pin 7 in Section 3.3 QFN20 Pin Description • Added deep sleep mode to Section 4.2.1 Power Modes • Added clock selection for SPI, I2C to Table 4-2 in Section 4.3 Clock • Updated Section 4.4 Reset • Updated GPIO number in Section 4.5 General-purpose I/Os (GPIO) • Added Section 4.6 SPI Interface (SPI), Section 4.8 I2C Interface (I2C), Section 4.9 GDMA Controller (GDMA) • Updated PWM channel number in Section 4.10 PWM • Updated Section 4.11 Auxiliary ADC (AUX ADC) • Changed the parameter VDDDIG to VDDAON in Section 5.3 Recommended Operating Conditions • Added deep sleep current to Section 5.7 Current Consumption • Added Section 6.2 QFN32 4 x 4 mm Package • Added QFN32 ordering info to Table 8-1 in Section 8 Ordering Information
0.3	2022/7/7	<ul style="list-style-type: none"> • Corrected RAM size and removed Cache in Section 1 Features • Removed Cache from Figure 2-1 in Section 2 Overview • Added documentation for QFN40 package • Updated Operating temperature • Corrected IO mapping for ADC channels in Section 3 Pin Description • Added measurement conditions for RF characteristics and SAR ADC characteristics in Section 5 Electrical Characteristics • Added Section 7 Reflow Soldering Profile
1.0	2022/10/24	<ul style="list-style-type: none"> • Updated Wi-Fi TX power and RX sensitivity in Section 1 Features • Added 2 MB Flash option for QFN32 and QFN20 packages • Replaced low-power timer with real-time counter (RTC) • Added Section 5.2 ESD Ratings • Added active mode TX current and deep sleep current to Section 5.7

Version	Date	Description
		Current Consumption <ul style="list-style-type: none"> Updated and added RF data in Section 5.8 to Section 5.11 Updated SAR ADC characteristics table in Section 5.12 AUX ADC Characteristics
1.1	2023/2/20	<ul style="list-style-type: none"> Updated Table 2-1 for BK7238QN20 in Section 2 Overview Updated pin assignments of QFN20 package (BK7238QN20) Updated storage temperature range in Section 5.1 Absolute Maximum Ratings
1.2	2023/3/6	Added Section 4.2.2 Power-up Sequence
1.3	2023/3/31	Updated Section 8 Ordering Information
1.4	2023/4/28	Updated ESD ratings in Section 5.2 ESD Ratings
1.5	2023/8/10	<ul style="list-style-type: none"> General wording update Removed PTA support from Section 1 Features Renamed standby mode as sleep mode and SAR ADC as AUX ADC throughout document Corrected CLK13M signal description in Section 3 Pin Description Updated wording for Section 4 Functional Description Renamed Section Modes of Operation as Section 4.2.1 Power Modes Organized Section 4.2.1 Power Modes and Section 4.2.2 Power-up Sequence as subsections under Section 4.2 Power Management Removed note “Values currently listed in this section are preliminary measurements and are subject to change.” from Section 5 Electrical Characteristics Updated and added measurement data in Section 5 Electrical Characteristics Updated minimum ordering quantity for QFN20 package in Section 8 Ordering Information
1.6	2023/11/7	Updated minimum recommended operating voltage for VCCIF, VCCRFE, and VCCPLL in Section 5.3 Recommended Operating Conditions

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