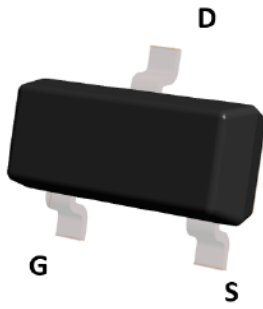
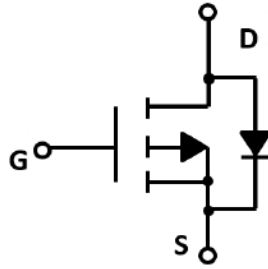
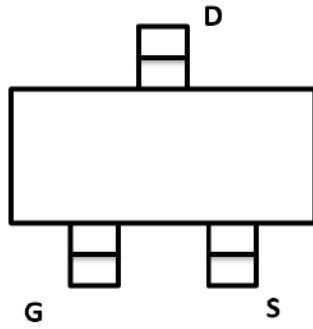


## P-Channel Enhancement Mode Field Effect Transistor



Top View

SOT-23



### Product Summary

- $V_{DS}$  -30V
- $I_D$  -4.1A
- $R_{DS(ON)}$ ( at  $V_{GS}=-10V$ ) <49mohm
- $R_{DS(ON)}$ ( at  $V_{GS}=-4.5V$ ) <65mohm

### General Description

- Trench Power LV MOSFET technology
- High density cell design for Low  $R_{DS(ON)}$
- High Speed switching
- Part no. with suffix "Q" means AEC-Q101 qualified

### Applications

- Battery protection
- Load switch
- Power management

### ■ Absolute Maximum Ratings ( $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-source Voltage	$V_{DS}$	-30	V
Gate-source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current	$I_D$	$T_A=25^\circ\text{C}$	-4.1
		$T_A=70^\circ\text{C}$	-3.2
Pulsed Drain Current <sup>A</sup>	$I_{DM}$	-15	A
Total Power Dissipation	$P_D$	$T_A=25^\circ\text{C}$	1.2
		$T_A=70^\circ\text{C}$	0.8
Thermal Resistance Junction-to-Ambient <sup>B</sup>	$R_{\theta JA}$	105	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55~+150	$^\circ\text{C}$

### ■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJL3407AQ	F2	3407.	3000	30000	120000	7" reel



# YJL3407AQ

## ■ Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =-250μA	-30			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-30V, V <sub>GS</sub> =0V			-1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±10V, V <sub>DS</sub> =0V			±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA	-1	-1.5	-2.4	V
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =-10V, I <sub>D</sub> =-4.1A		36	49	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-3.5A		52	65	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =-4.1A, V <sub>GS</sub> =0V			-1.2	V
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =-15V, V <sub>GS</sub> =0V, f=1MHZ		572		pF
Output Capacitance	C <sub>oss</sub>			82		
Reverse Transfer Capacitance	C <sub>rss</sub>			70		
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-15V, I <sub>D</sub> =-4.1A		11.65		nC
Gate-Source Charge	Q <sub>gs</sub>			2.32		
Gate-Drain Charge	Q <sub>gd</sub>			2.08		
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> =-10A, di/dt=100A/us		0.643		ns
Reverse Recovery Time	t <sub>rr</sub>			15.7		
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-15V, R <sub>L</sub> =15Ω R <sub>GEN</sub> =2.5Ω		3.8		ns
Turn-on Rise Time	t <sub>r</sub>			17.6		
Turn-off Delay Time	t <sub>D(off)</sub>			17.8		
Turn-off fall Time	t <sub>f</sub>			21.8		

A. Pulse Test: Pulse Width ≤ 300us, Duty cycle ≤ 2%.

B. R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>θJC</sub> is guaranteed by design, while R<sub>θJA</sub> is determined by the board design. The maximum rating presented here is based on mounting on a 1 in<sup>2</sup> FR-4 board with 2oz copper.



■ Typical Performance Characteristics

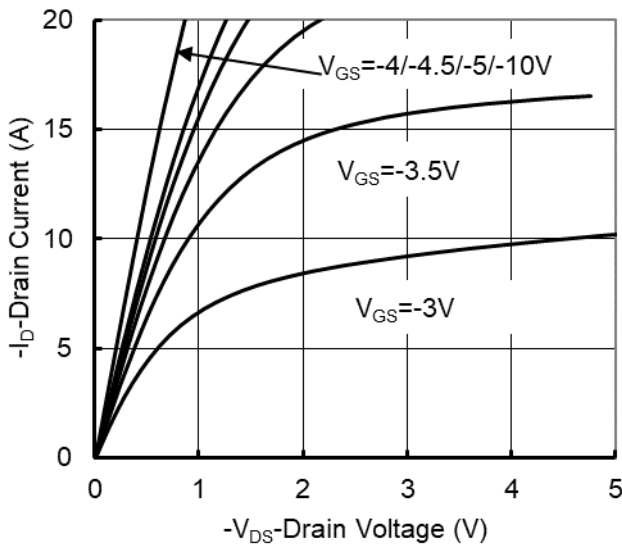


Figure1. Output Characteristics

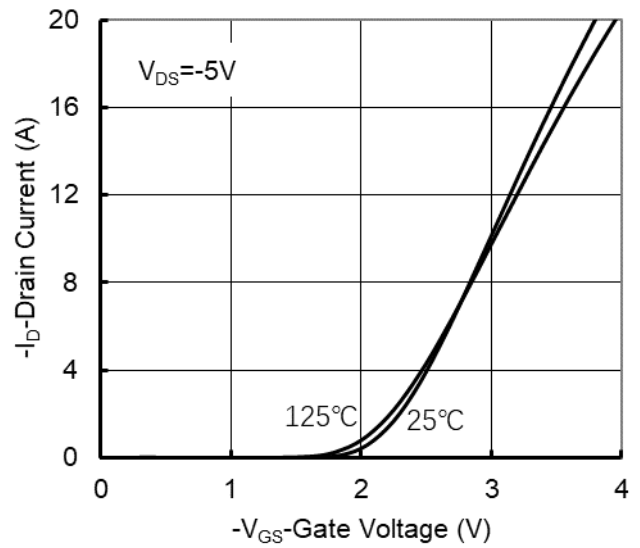


Figure2. Transfer Characteristics

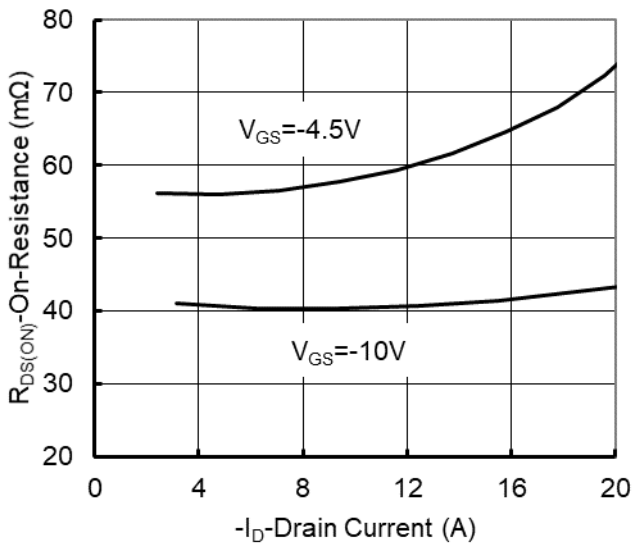


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

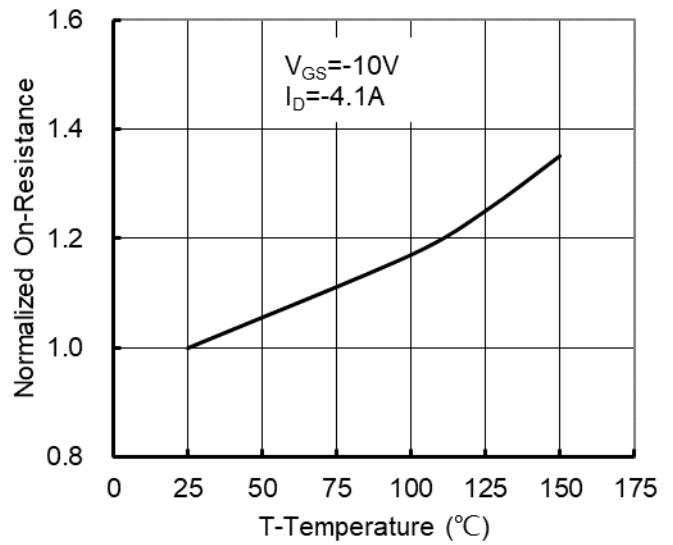


Figure 4: On-Resistance vs. Junction Temperature

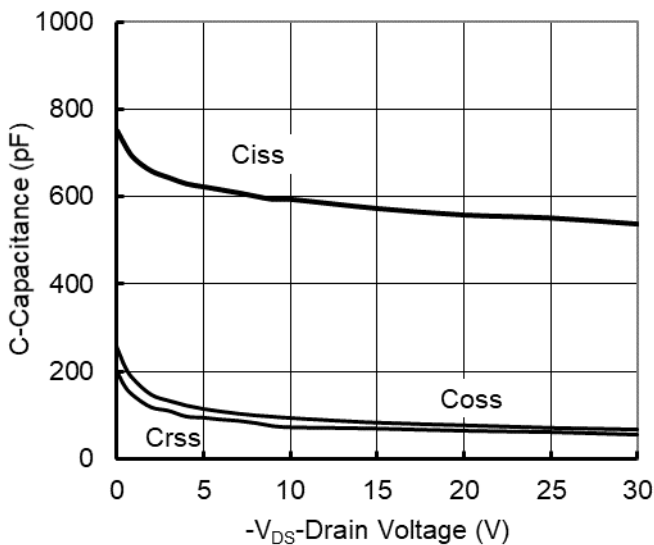


Figure5. Capacitance Characteristics

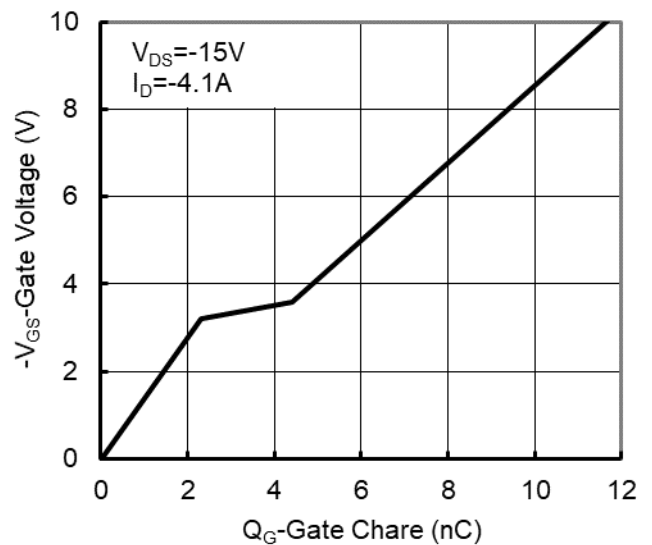


Figure6. Gate Charge

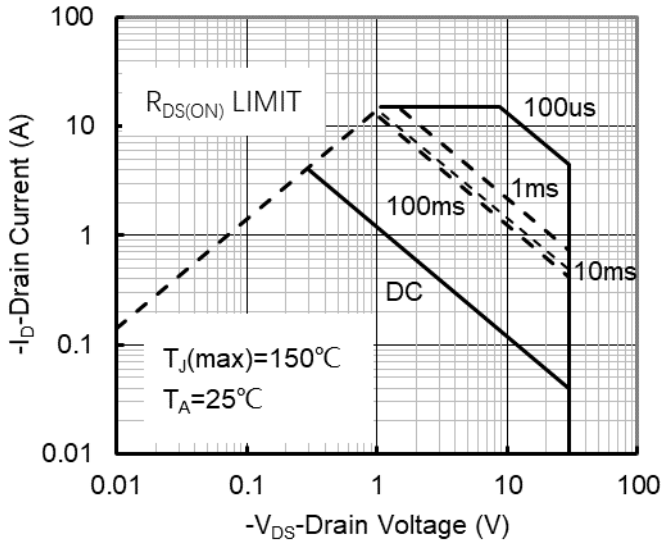


Figure7. Safe Operation Area

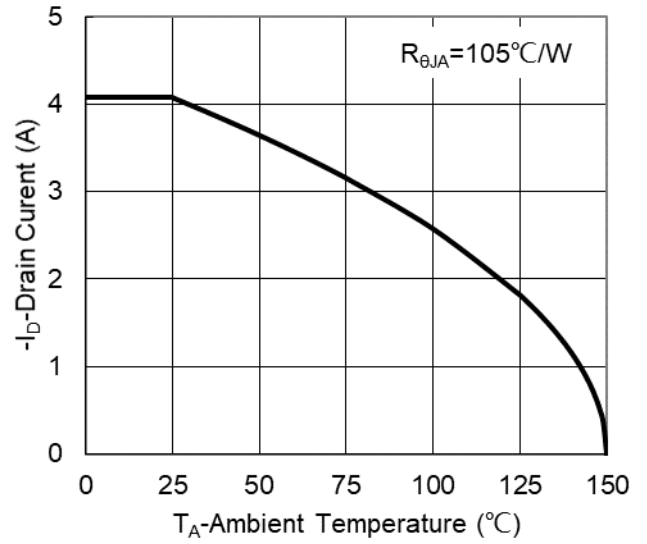


Figure8. Maximum Continuous Drain Current vs Ambient Temperature

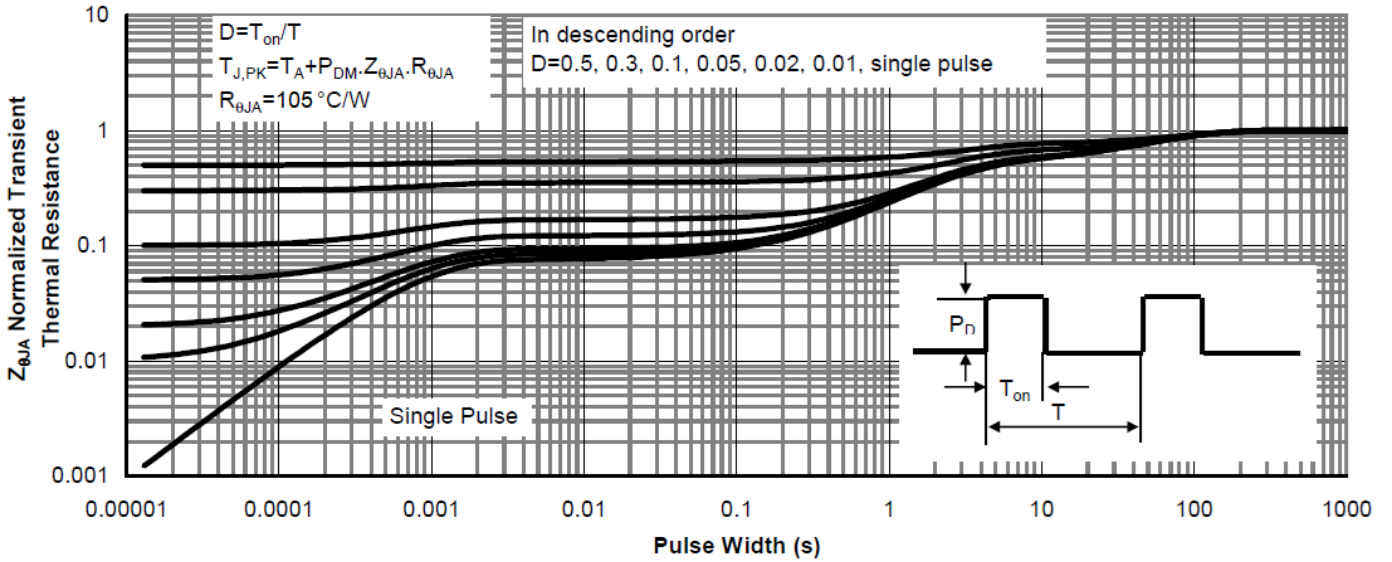
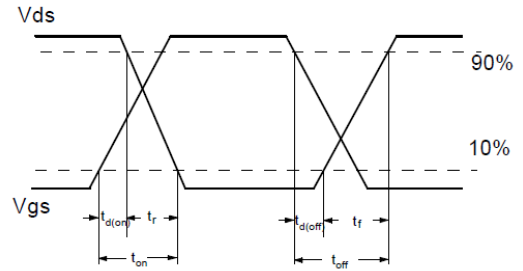
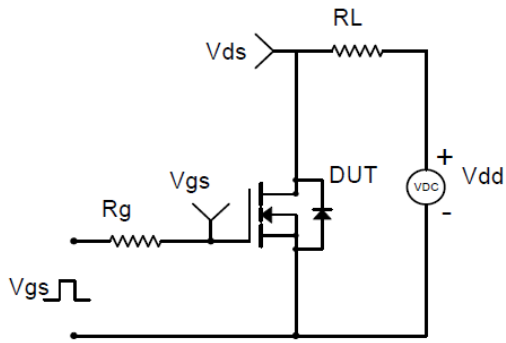
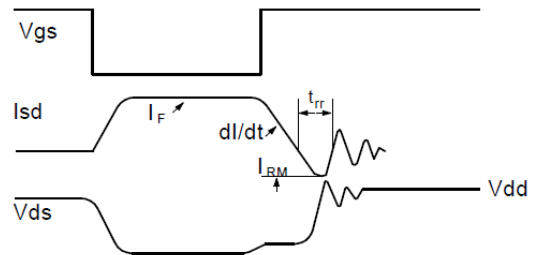
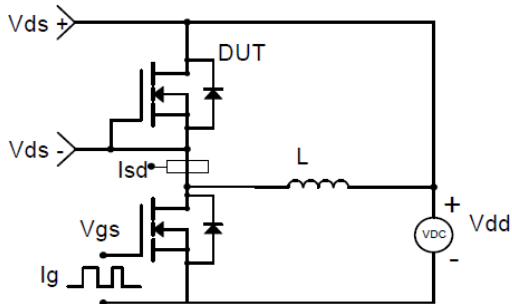


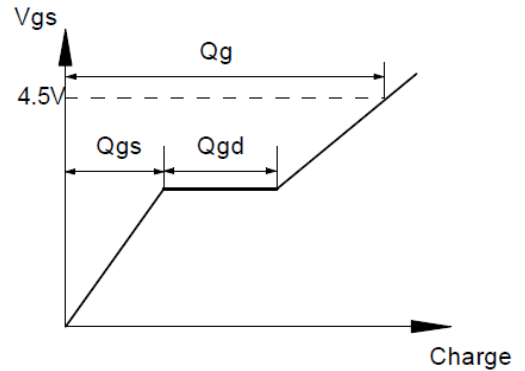
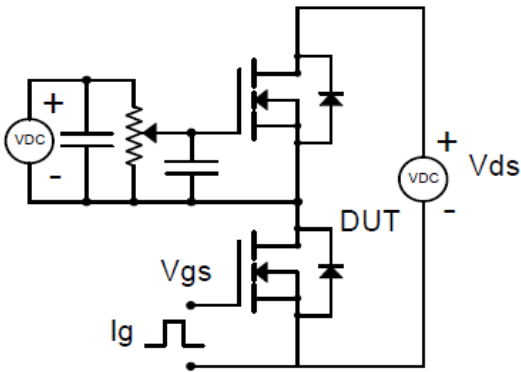
Figure9. Normalized Maximum Transient Thermal Impedance



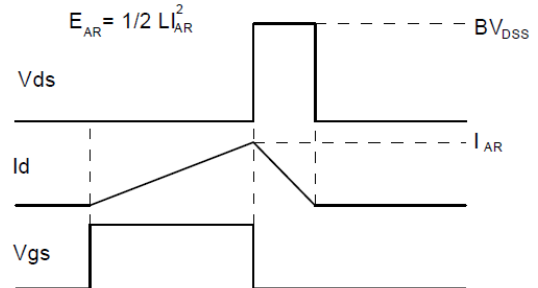
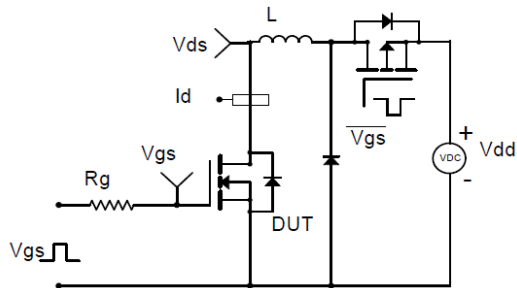
**Resistive Switching Test Circuit & Waveforms**



**Diode Recovery Test Circuit & Waveforms**



**Gate Charge Test Circuit & Waveform**

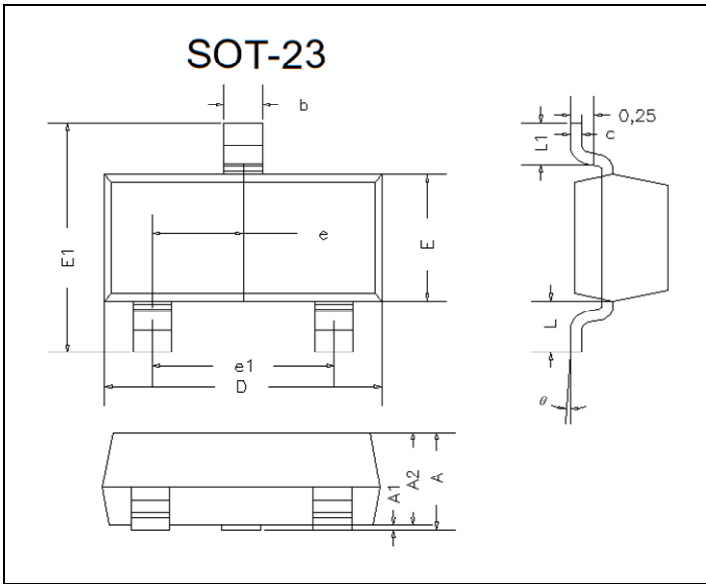


**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**



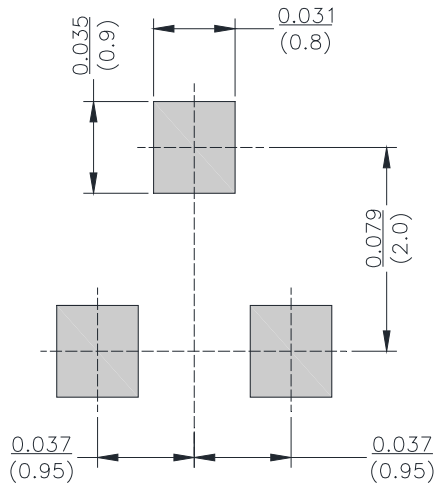
# YJL3407AQ

## ■ SOT-23 Package information



DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	0.035	0.045	0.90	1.15	
A1	0.000	0.004	0.00	0.10	
A2	0.035	0.041	0.90	1.05	
b	0.012	0.020	0.30	0.50	
c	0.004	0.008	0.10	0.20	
D	0.110	0.118	2.80	3.00	
E	0.047	0.055	1.20	1.40	
E1	0.089	0.100	2.25	2.55	
e	0.370TYP		0.95TYP		
e1	0.071	0.079	1.80	2.00	
L	0.220REF		0.55REF		
L1	0.012	0.020	0.30	0.50	
$\theta$	0°	8°	0°	8°	

## ■ SOT-23 Suggested Pad Layout





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