General Description

The WSD30L88DN56 is the highest performance trench Dual P-Ch MOSFET with extreme high cell density,which provide excellent RDSON and gate charge for most of the synchronous buck converter applications .

The WSD30L88DN56 meet the RoHS and Green Product requirement 100% EAS guaranteed with full function reliability approved.

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

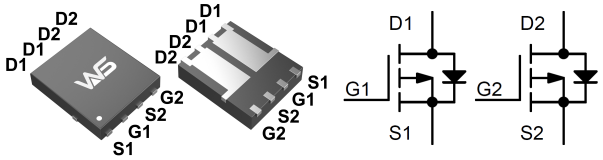
Product Summery

BVDSS	RDSON	ID
-30V	11.5mΩ	-49A

Applications

- High Frequency Point-of-Load Synchronous Buck Converter for MB/NB/UMPC/VGA
- Networking DC-DC Power System
- Load Switch

DFN5X6C-8-EP2 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-30	V
V_{GS}	Gate-Source Voltage	±20	V
I_D@T_C=25℃	Continuous Drain Current, V_{GS} @ -10V[1]	-49	A
I_D@T_C=100℃	Continuous Drain Current, V_{GS} @ -10V[1]	-23	A
I_{DM}	Pulsed Drain Current[2]	-120	A
EAS	Single Pulse Avalanche Energy[3]	68	mJ
P_D@T_C=25℃	Total Power Dissipation[4]	40	W
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient [1]	---	50	℃/W
$R_{\theta JC}$	Thermal Resistance Junction-Case[1]	---	2.4	℃/W

Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=-250uA	-30	---	---	V
$\triangle BV_{DSS}/\triangle T_J$	BVDSS Temperature Coefficient	Reference to 25℃ , I_D=-1mA	---	-0.0332	---	V/℃
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=-10V , I_D=-10A	---	11.5	16	mΩ
		V_{GS}=-4.5V , I_D=-5A	---	16	20	
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =-250uA	-1.2	-1.5	-2.5	V
$\triangle V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	4.4	---	mV/℃
I_{DSS}	Drain-Source Leakage Current	V_{DS}=-24V , V_{GS}=0V , T_J=25℃	---	---	-1	uA
		V_{DS}=-24V , V_{GS}=0V , T_J=55℃	---	---	-5	
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±20V , V_{DS}=0V	---	---	±100	nA
gfs	Forward Transconductance	V_{DS}=-5V , I_D=-10A	35	---	---	S
R_g	Gate Resistance	V_{DS}=0V , V_{GS}=0V , f=1MHz	---	7	---	Ω
Q_g	Total Gate Charge (-4.5V)	V_{DS}=-15V , V_{GS}=-10V , I_D=-5A	---	22	---	nC
Q_{gs}	Gate-Source Charge		---	5.5	---	
Q_{gd}	Gate-Drain Charge		---	5.9	---	
$T_{d(on)}$	Turn-On Delay Time	V_{DD}=-15V , V_{GEN}=-10V , R_G=3Ω, I_D=-1A	---	9	---	ns
T_r	Rise Time		---	13	---	
$T_{d(off)}$	Turn-Off Delay Time		---	48	---	
T_f	Fall Time		---	20	---	
C_{iss}	Input Capacitance	V_{DS}=-15V , V_{GS}=0V , f=1MHz	---	2135	---	pF
C_{oss}	Output Capacitance		---	282	---	
C_{rss}	Reverse Transfer Capacitance		---	255	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current[1,6]	V_G=V_D=0V , Force Current	---	---	-29.5	A
I_{SM}	Pulsed Source Current[2,6]		---	---	-44	A
V_{SD}	Diode Forward Voltage[2]	V_{GS}=0V , I_S=-1A , T_J=25℃	---	---	-1.2	V

Note :
1.The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper,t<10sec.
2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
3.The EAS data shows Max. rating . The test condition is V_{DD}=-15V,V_{GS}=-10V,L=0.1mH,I_{AS}=-36A
4.The power dissipation is limited by 150℃ junction temperature
5.The Min. value is 100% EAS tested guarantee.
6.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

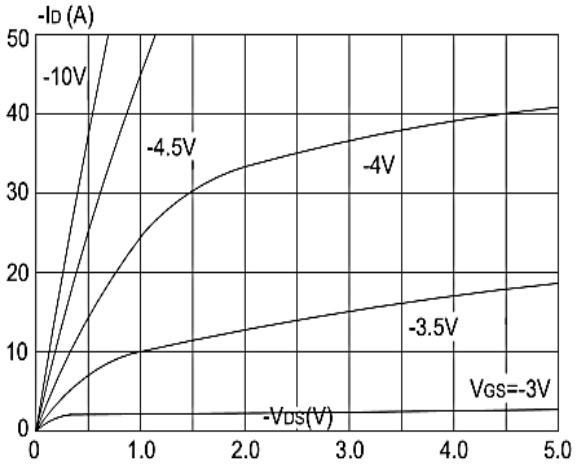


Figure1: Output Characteristics Figure

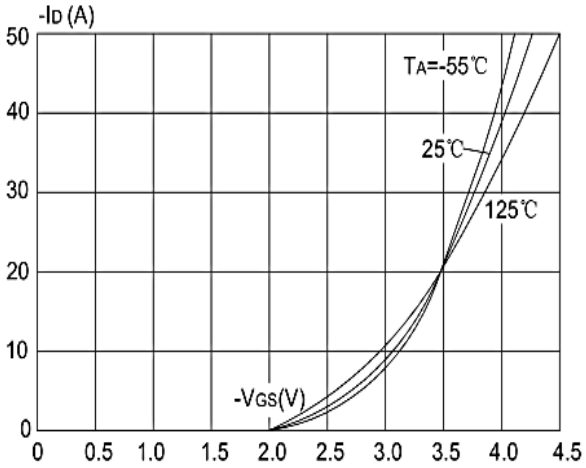


Figure2: Typical Transfer Characteristics

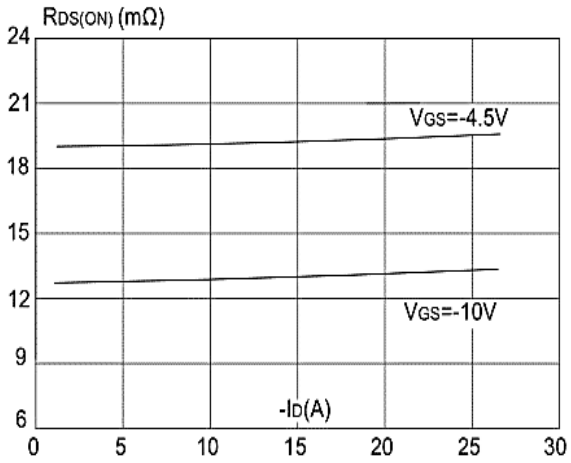


Figure 3:On-resistance vs. Drain Current

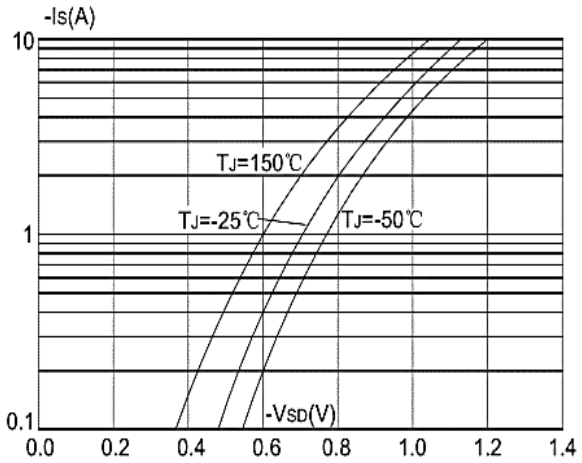


Figure 4: Body Diode Characteristics

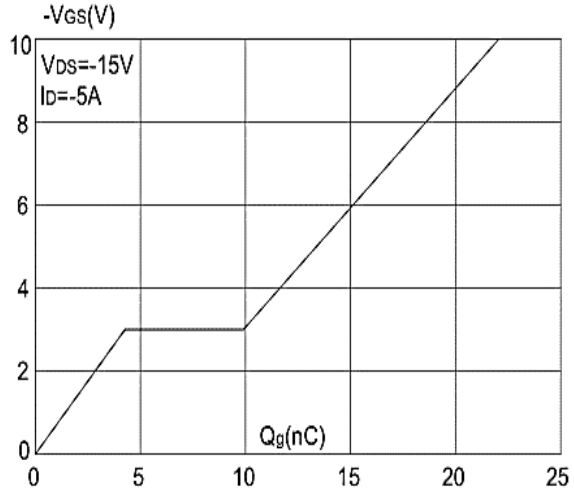


Figure 5: Gate Charge Characteristics

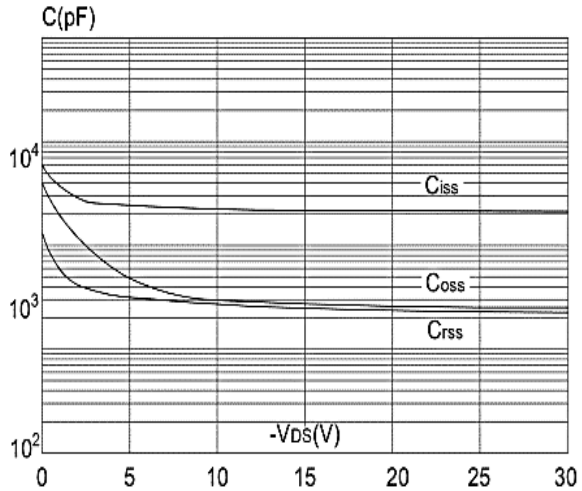


Figure 6: Capacitance Characteristics

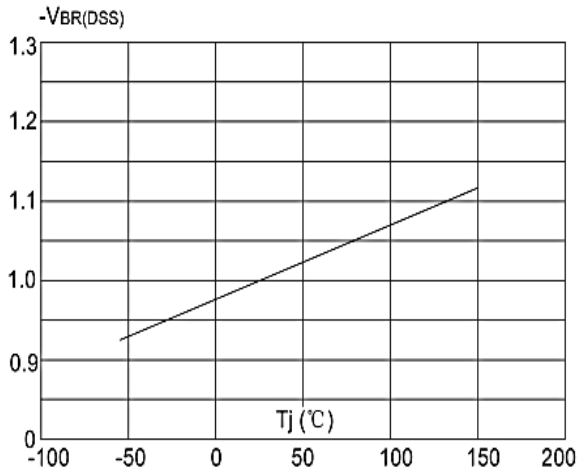


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

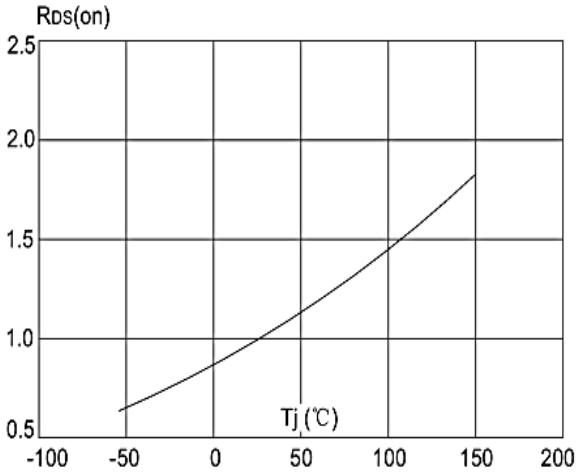


Figure 8: Normalized on Resistance vs. Junction Temperature

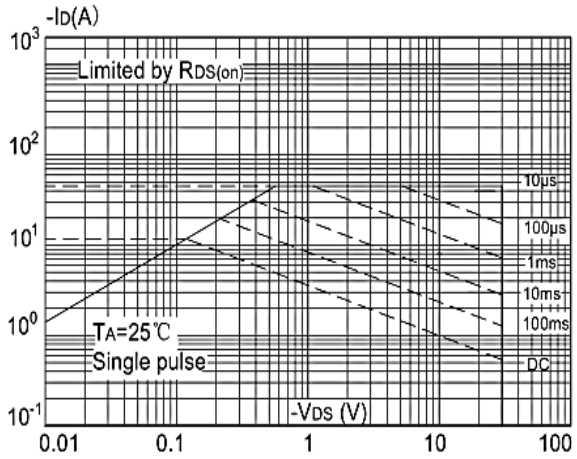


Figure 9: Maximum Safe Operating Area

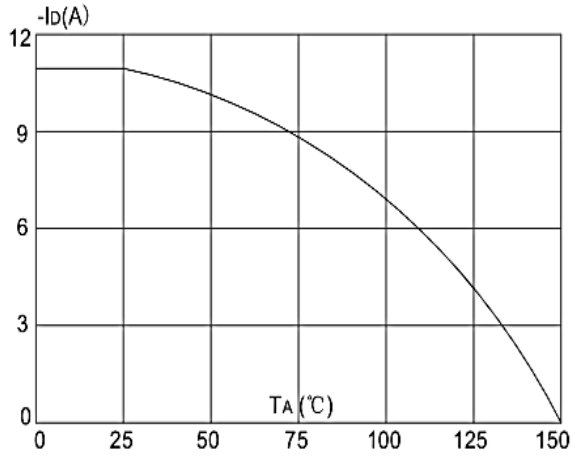


Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature

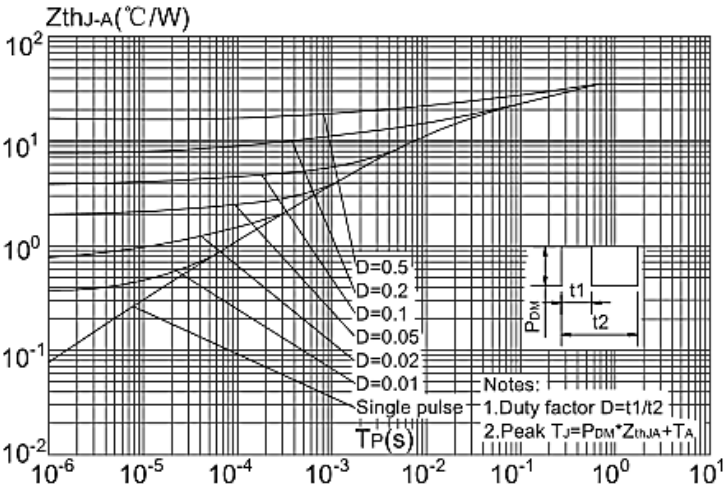


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

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