



# TF0579U

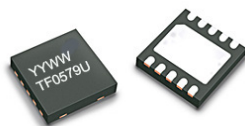
## 100V High Frequency High-Side and Low-Side Gate Driver with Integrated BSD

### Features

- Drives two N-channel MOSFETs in a half bridge configuration
- Integrated bootstrap diode (BSD) included
- Floating high-side driver in bootstrap operation to 100V
- 1.5A source / 2.5A sink output current capability
- Undervoltage lockout for high and low side drivers
- Delay matching a maximum of 10ns
- Propagation delay a typical of 60ns
- Ultra low standby current (<1 $\mu$ A)
- Logic input (HIN, LIN, and EN) 3.3V capability
- Extended temperature range: -40°C to +125°C
- Space saving TDFN-10 3x3mm package

### Applications

- BLDC Motor Drivers
- Battery Powered Hand Tools
- DC/DC converters



TDFN-10

### Description

The TF0579U is a high frequency gate driver capable of driving N-channel MOSFETs in a half bridge configuration. The floating high-side driver can switch to 100V in a bootstrap configuration.

The TF0579U contains an integrated bootstrap diode to greatly ease design and reduce the BOM.

The TF0579U logic inputs are compatible with standard TTL and CMOS levels (down to 3.3V) to interface easily with MCUs. UVLO for high side and low side will protect MOSFET with loss of supply. Also to protect MOSFETs, cross conduction prevention logic prevents the HO and LO to be on at the same time.

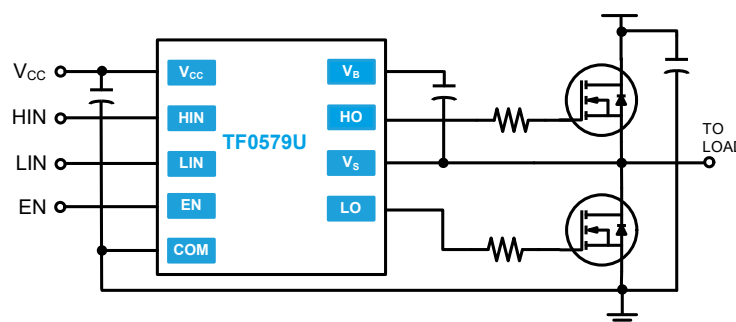
Fast and well matched propagation delays allow a higher switching frequency, enabling a smaller, more compact power switching design using smaller associated components. The TF0579U comes in a space-saving TDFN-10 package and operates over an extended -40 °C to +125 °C temperature range.

### Ordering Information

Year Year Week Week

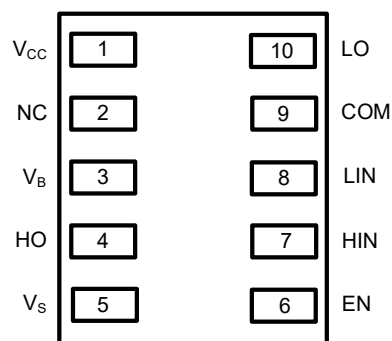
PART NUMBER	PACKAGE	PACK / Qty	MARK
TF0579U-NHS	TDFN-10	Tube / 120	YYWW TF0579U
TF0579U-NHP	TDFN-10	T&R / 3,000	TF0579U

### Typical Application



## Pin Diagrams

### 100V High Frequency High-Side and Low-Side Gate Driver with Integrated BSD

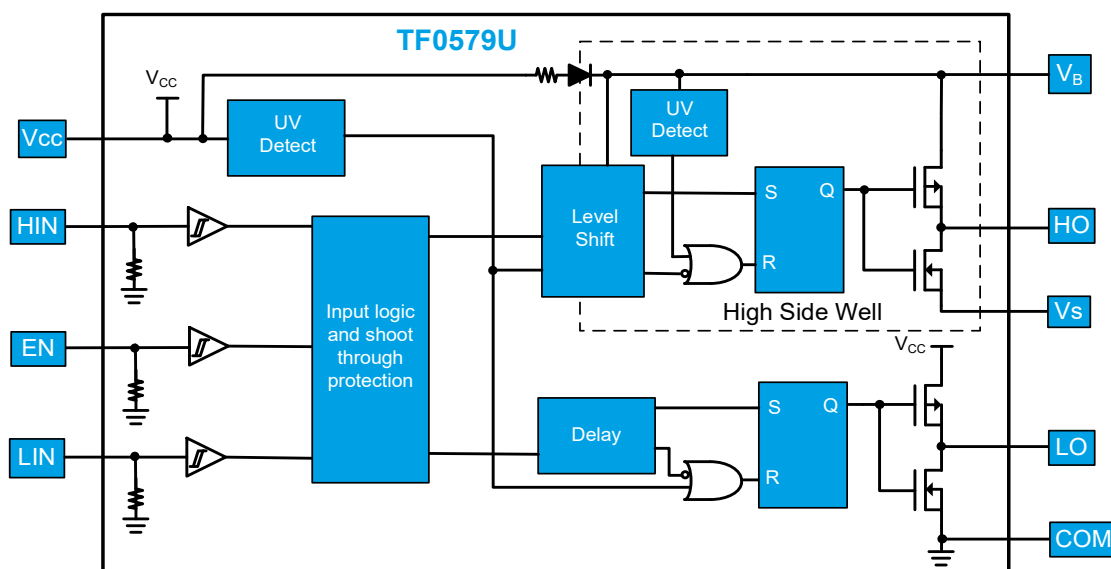


Top View

## Pin Descriptions

PIN NAME	PIN NUMBER	PIN DESCRIPTION
$V_{CC}$	1	Low-side and logic fixed supply
NC	2	No Connect
$V_B$	3	High-side floating supply
HO	4	High-side gate driver output
$V_S$	5	High-side floating supply return
EN	6	Logic input enable, a logic low turns off gate drivers
HIN	7	Logic input for high-side gate driver, in phase with HO
LIN	8	Logic input for low-side gate driver, in phase with LO
COM	9	Low-side and logic return
LO	10	Low-side gate drive output
COM	PAD	Low-side and logic return

## Functional Block Diagram





## 100V High Frequency High-Side and Low-Side Gate Driver with Integrated BSD

### Absolute Maximum Ratings *(NOTE1)*

$V_B$  - High side floating positive supply voltage.....0.3V to 110V  
 $V_S$  - High side floating negative supply voltage.. $V_B$ -20V to  $V_B$ +0.3V  
 $V_{HO}$  - Highside floating output voltage..... $V_S$ -0.3Vto  $V_B$ +0.3V  
 $dV_S/dt$  - Offset supply voltage transient.....50V/ns

$V_{CC}$  - Logic and Low-side fixed supply voltage.....-0.3V to +20V  
 $V_{LO}$  - Low-side output voltage.....-0.3V to  $V_{CC}$ +0.3V  
 $V_{IN}$  - Logic input voltage (HIN, LIN, and EN).....-0.3V to  $V_{CC}$ +0.3V

**NOTE1** Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

$P_D$  - Package power dissipation at  $T_A = 25^\circ\text{C}$   
 TDFN-10.....0.4W

#### TDFN-10 Thermal Resistance *(NOTE2)*

$\theta_{JA}$ .....64°C/W  
 $\theta_{JC}$ ..... 42°C/W

$T_J$  - Junction operating temperature.....-40°C to +150°C  
 $T_L$  - Lead Temperature (soldering, 10 seconds).....+300°C  
 $T_{stg}$  - Storage temperature .....-55°C to 150°C

**NOTE2** When mounted on a standard JEDEC 2-layer FR-4 board.

### Recommended Operating Conditions

Symbol	Parameter	MIN	MAX	Unit
$V_B$	High side floating supply	$V_S + 5.8$	$V_S + 18$	V
$V_S$	High side floating supply offset voltage	<b>NOTE3</b>	100	V
$V_{HO}$	High side floating output voltage	$V_S$	$V_B$	V
$V_{CC}$	Logic and Low side fixed supply voltage	6.5	18	V
$V_{LO}$	Low side output voltage	0	$V_{CC}$	V
$V_{IN}$	Logic input voltage (HIN, LIN and EN)	0	5	V
$T_A$	Ambient temperature	-40	125	°C

**NOTE3** Logic operational for  $V_S$  of -5V to +100V.



## 100V High Frequency High-Side and Low-Side Gate Driver with Integrated BSD

### DC Electrical Characteristics (NOTE4)

$V_{CC} = V_{BS} = 12V$ ,  $COM = V_S = 0V$ ,  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
$V_{IH}$	Logic "1" input voltage	HIN and LIN, <b>NOTES</b>	2.4			V
$V_{IL}$	Logic "0" input voltage					
$V_{EIH}$	Enable logic "1" input voltage	EN	1.5			
$V_{EIL}$	Enable logic "0" input voltage					
$V_{INHYS}$	Input voltage hysteresis			0.7		
$V_{OH}$	High level output voltage, $V_{BIAS} - V_O$	$I_{O+} = 10\text{mA}$		0.05	0.3	
$V_{OL}$	Low level output voltage, $V_O$	$I_{O-} = 10\text{mA}$		0.02	0.1	
$I_{LK}$	Offset supply leakage current	$V_B = V_S = 100V$		0.1	1	$\mu\text{A}$
$I_{CCSD}$	$V_{CC}$ shutdown supply current	$V_{IN} = 0V$ or $5V$ , $V_{EN} = 0V$		0	1	
$I_{CCQ}$	$V_{CC}$ quiescent supply current	$V_{IN} = 0V$ or $5V$		80	150	
$I_{CCOP}$	$V_{CC}$ operating supply current	$f_s = 500\text{kHz}$ , $C_L = 1\text{nF}$		8.2		$\text{mA}$
$I_{BSQ}$	$V_{BS}$ quiescent supply current	$V_{IN} = 0V$ or $5V$		50	100	$\mu\text{A}$
$I_{BSOP}$	$V_{BS}$ operating supply current	$f_s = 500\text{kHz}$ , $C_L = 1\text{nF}$		8.0		$\text{mA}$
$I_{IN+}$	Logic "1" input bias current	$V_{IN} = 5V$			50	$\mu\text{A}$
$I_{IN-}$	Logic "0" input bias current	$V_{IN} = 0V$			5	
$V_{BSUV+}$	$V_{BS}$ supply under-voltage positive going threshold		3.8	4.9	5.8	V
$V_{BSUV-}$	$V_{BS}$ supply under-voltage negative going threshold		3.3	4.5	5.3	
$V_{CCUV+}$	$V_{CC}$ supply under-voltage positive going threshold		4.0	5.2	6.0	
$V_{CCUV-}$	$V_{CC}$ supply under-voltage negative going threshold		3.5	4.7	5.5	
$I_{O+}$	Output high short circuit pulsed current	$V_O = 0V$ , $PW \leq 10\text{ }\mu\text{s}$	1.0	1.5		A
$I_{O-}$	Output low short circuit pulsed current	$V_O = 12V$ , $PW \leq 10\text{ }\mu\text{s}$	1.5	2.5		
$V_{F1}$	Forward voltage of bootstrap diode	$I_F = 100\text{ }\mu\text{A}$		0.6	0.75	V
$V_{F2}$	Forward voltage of bootstrap diode	$I_F = 100\text{mA}$		1.4	1.75	

**NOTE4** The  $V_{IN}$  and  $I_{IN}$  parameters are applicable to the logic input pins: HIN, LIN, and EN. The  $V_O$  and  $I_O$  parameters are applicable to the respective output pins: HO and LO

**NOTE5** For optimal operation, it is recommended that the input pulse (to HIN, LIN, and EN) should have an amplitude of 2.4V minimum with a pulse width of 140ns minimum.



## 100V High Frequency High-Side and Low-Side Gate Driver with Integrated BSD

### AC Electrical Characteristics

$V_{CC} = V_{BS} = 12V$ ,  $COM = V_S = 0V$ ,  $C_L = 1000pF$ ,  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
$t_{on}$	Turn-on propagation delay			65		ns
$t_{off}$	Turn-off propagation delay	$V_S = 100V$		58		
$t_{DM}$	Delay matching, HS & LS turn-on			1	10	
$t_r$	Turn-on rise time			27		
$t_f$	Turn-off fall time			20		



# Timing Waveforms

## 100V High Frequency High-Side and Low-Side Gate Driver with Integrated BSD

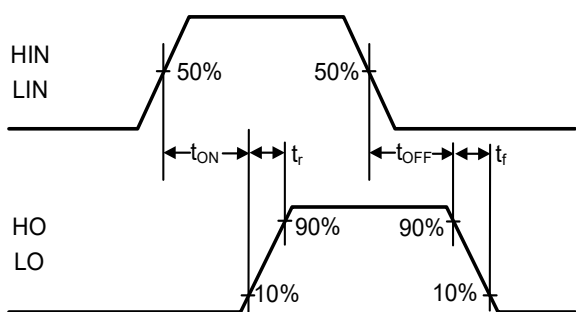


Figure 1. Switching Time Waveform Definitions

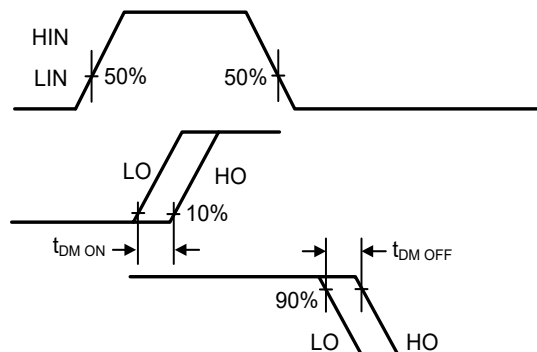


Figure 2. Delay Matching Waveform Definitions

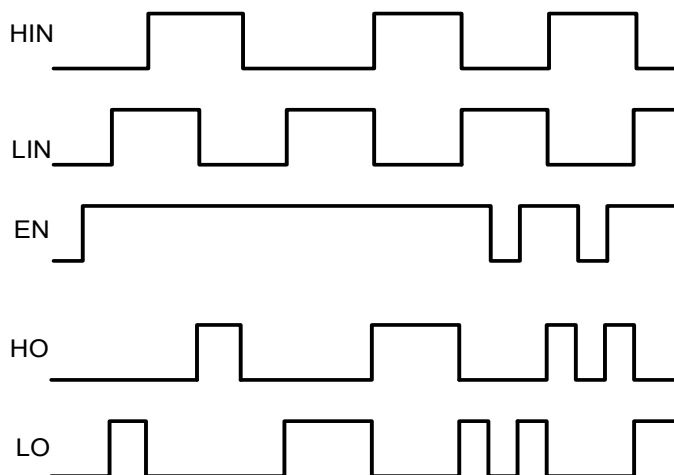
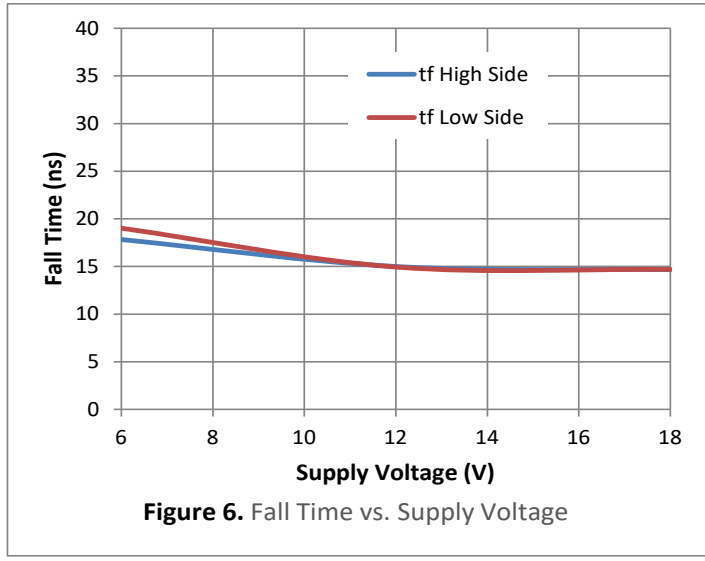
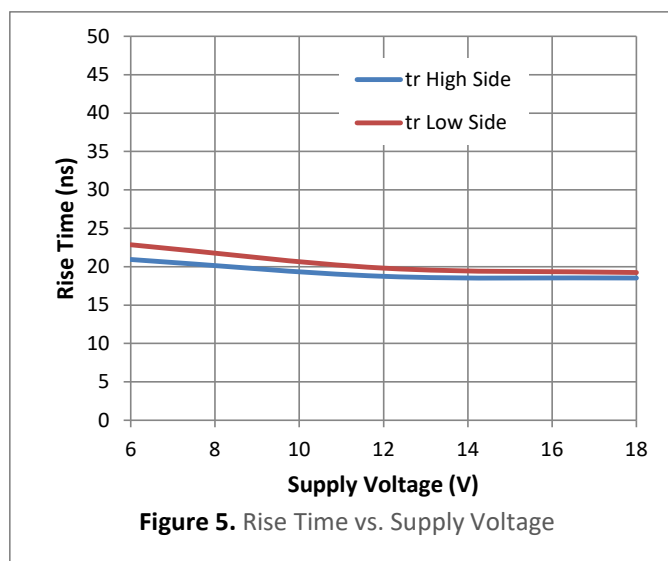
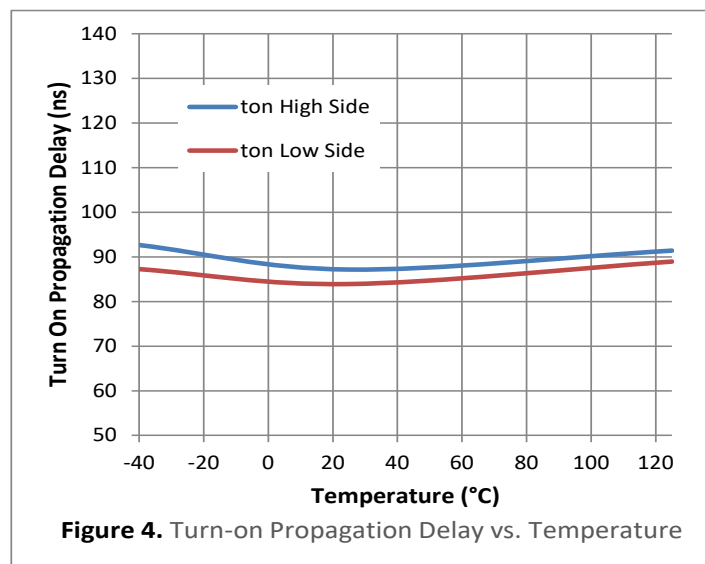
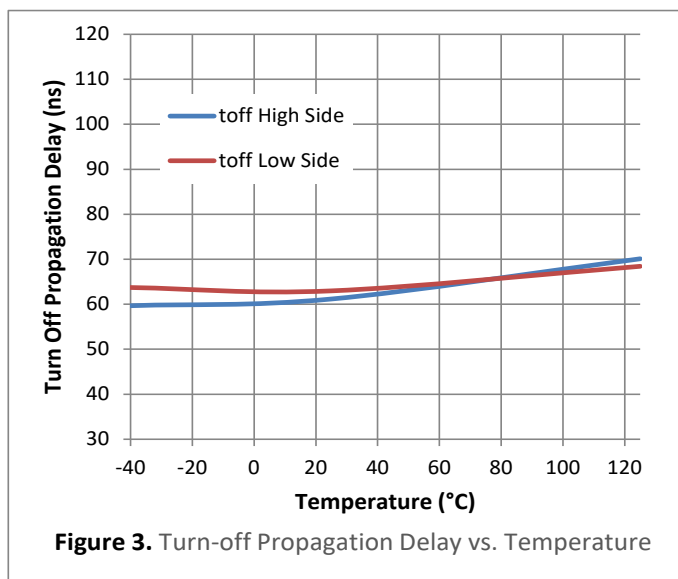
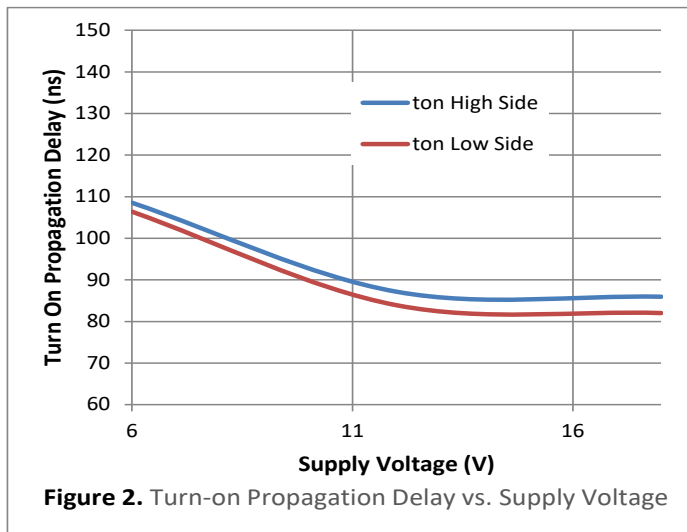
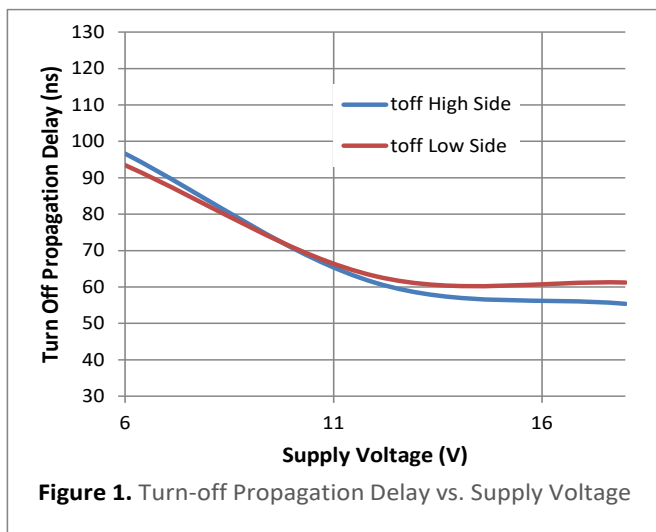


Figure 3. Input / Output Timing Diagram



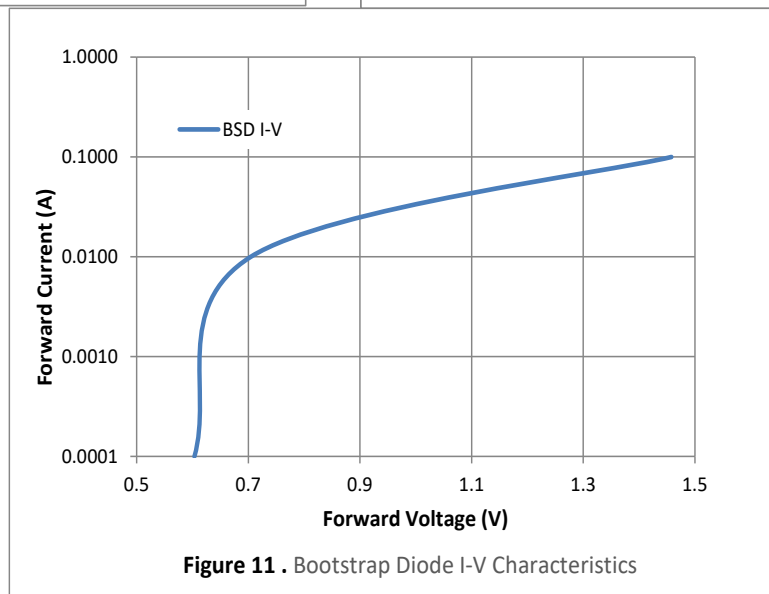
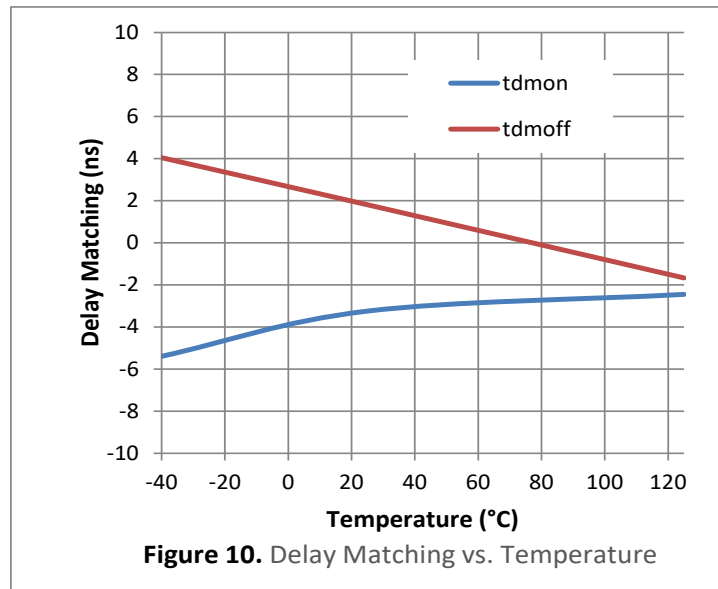
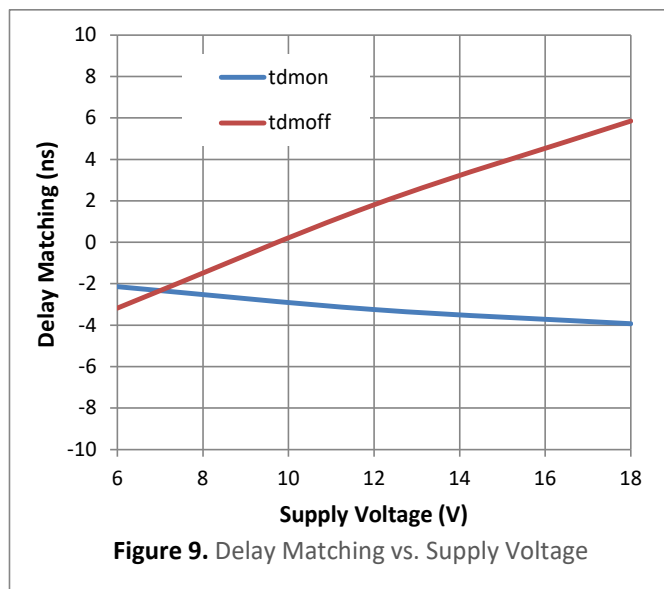
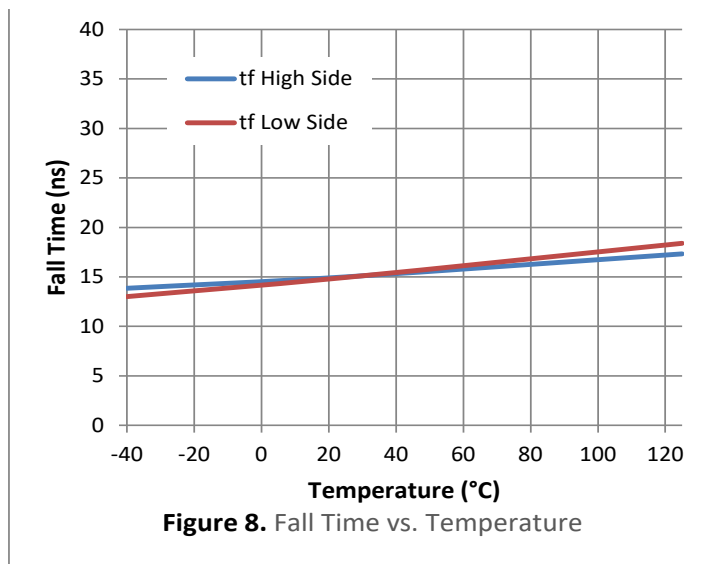
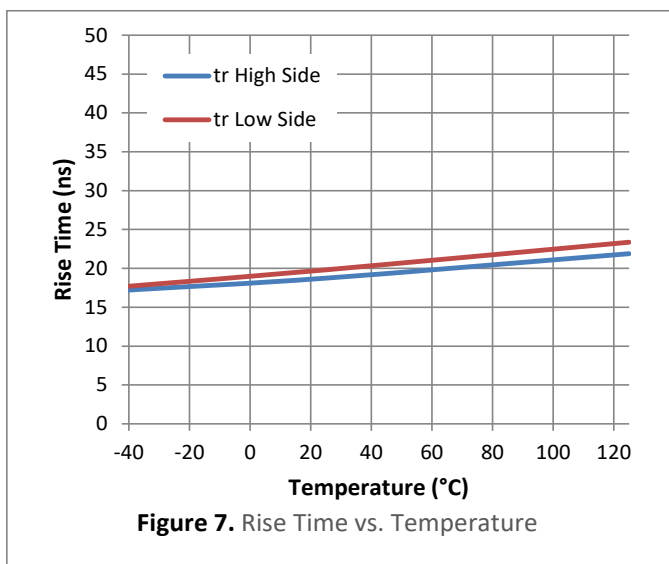
100V High Frequency High-Side and Low-Side Gate Driver with Integrated BSD

Typical Characteristics





100V High Frequency High-Side and Low-Side Gate Driver with Integrated BSD



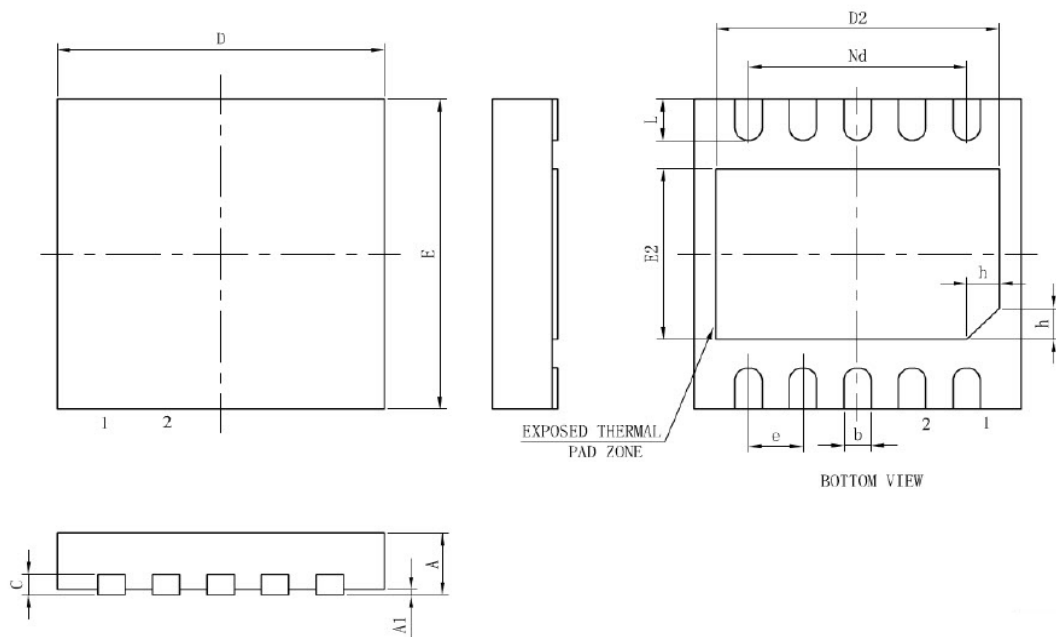




**100V High Frequency High-Side and Low-Side Gate Driver with Integrated BSD**

**Package Dimensions (TDFN-10)**

Please contact support@tfsemi.com for package availability.



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	2.90	3.00	3.10
D2	2.40	2.50	2.60
c	0.50BSC		
Nd	2.00BSC		
E	2.90	3.00	3.10
E2	1.45	1.55	1.65
L	0.30	0.40	0.50
h	0.20	0.25	0.30



## 100V High Frequency High-Side and Low-Side Gate Driver with Integrated BSD

### Revision History

Rev.	Change	Owner	Date
1.0	First release	Keith Spaulding	4/14/2020
1.1	Add Enable logic input threshold specification	Keith Spaulding	6/10/2020
1.2	Electrical specs changed to match early production data, and some graphs added.	Keith Spaulding	8/1/2020

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