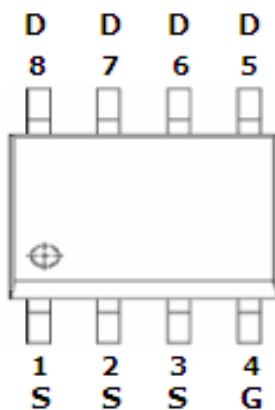
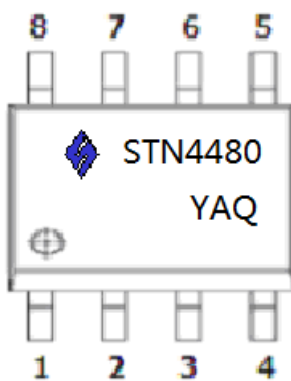


DESCRIPTION

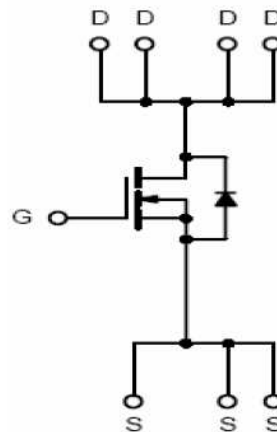
STN4480 is the N-Channel logic enhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as power management and other battery powered circuits where high-side switching.

**PIN CONFIGURATION
SOP-8**

FEATURE


- 40V/14.0A, $R_{DS(ON)} = 13m\Omega$ (Typ.) @ $V_{GS} = 10V$
- 40V/5.0A, $R_{DS(ON)} = 15m\Omega$ @ $V_{GS} = 4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOP-8 package design

PART MARKING


Y: Year Code
A: week Code
Q: Process Code





STN4480 

N Channel Enhancement Mode MOSFET

14.0A

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	VDSS	40	V
Gate-Source Voltage	VGSS	±20	V
Continuous Drain Current (TJ=150°C)	ID	TA=25°C 14.0	A
		TA=70°C 10.0	
Pulsed Drain Current	IDM	70	A
Continuous Source Current (Diode Conduction)	IS	4.0	A
Power Dissipation	PD	TA=25°C 3.1	W
		TA=70°C 2.0	
Operation Junction Temperature	TJ	150	°C
Storage Temperature Range	TSTG	-55/150	°C
Thermal Resistance-Junction to Ambient	RθJA	59	°C/W

ELECTRICAL CHARACTERISTICS (Ta = 25°C Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	40			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0		3.0	V
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=32V, V_{GS}=0V$			1	uA
		$V_{DS}=32V, V_{GS}=0V$ $T_J=55^\circ C$			5	
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=14A$ $V_{GS}=4.5V, I_D=8A$		13 15	15.5 18.0	mΩ
Forward Transconductance	g_{fs}	$V_{DS}=15V, I_D=6.2AV$		50		S
Diode Forward Voltage	V_{SD}	$I_S=2.3A, V_{GS}=0V$			1.0	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=20V, V_{GS}=10V$ $I_D=14A$		22		nC
Gate-Source Charge	Q_{gs}			10.5		
Gate-Drain Charge	Q_{gd}			4.8		
Input Capacitance	C_{iss}	$V_{DS}=20V, V_{GS}=0V$ $F=1MHz$		1600		pF
Output Capacitance	C_{oss}			320		
Reverse Transfer Capacitance	C_{rss}			102		
Turn-On Time	$t_{d(on)}$ t_r	$V_{DS}=20V, V_{GS}=10V$ $R_L=1.5\Omega$ $I_D=5.0A, V_{GEN}=3V$		3.5		nS
Turn-Off Time	$t_{d(off)}$ t_f			6		
				13.2		
				3.5		

TYPICAL CHARACTERISTICS

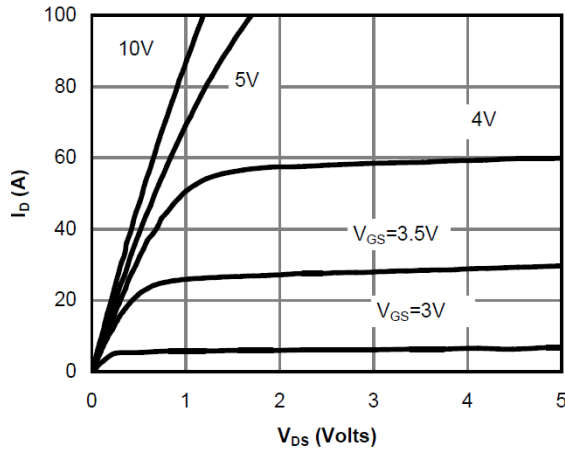


Figure 1: On-Region Characteristics

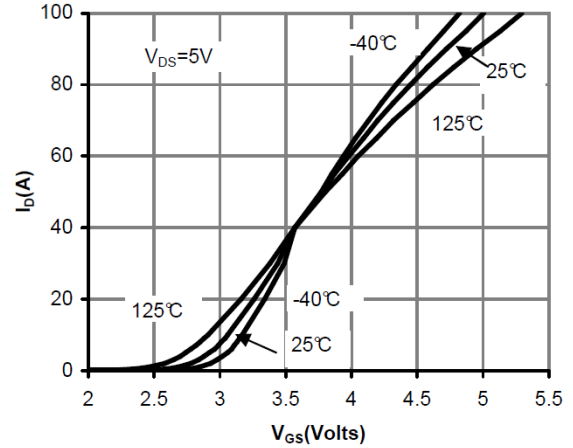


Figure 2: Transfer Characteristics

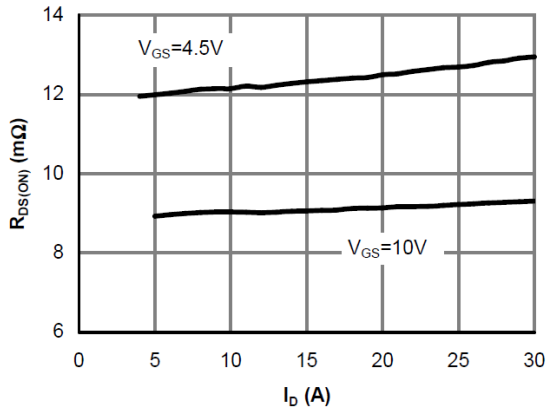


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

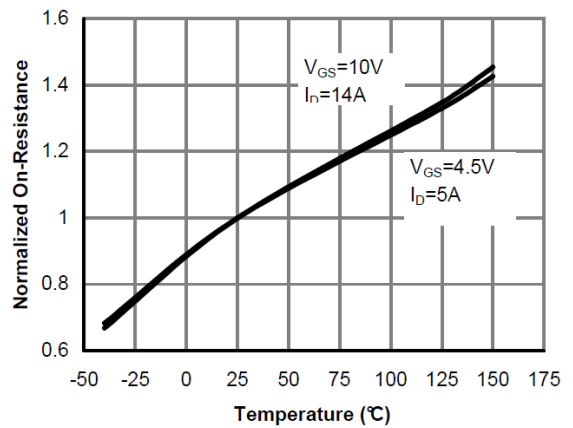


Figure 4: On-Resistance vs. Junction Temperature

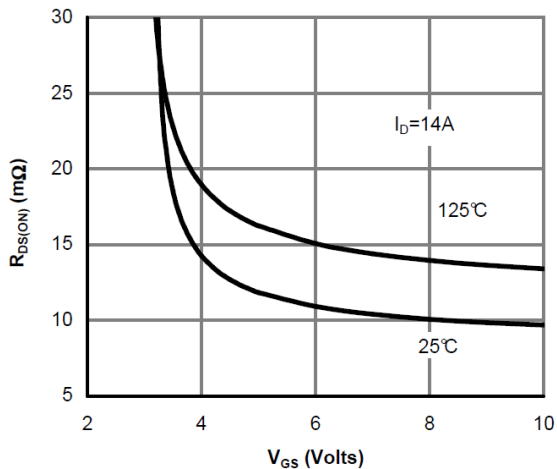


Figure 5: On-Resistance vs. Gate-Source Voltage

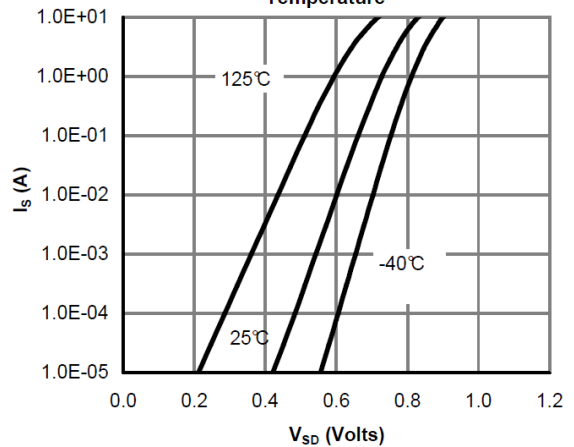


Figure 6: Body-Diode Characteristics

TYPICAL CHARACTERISTICS

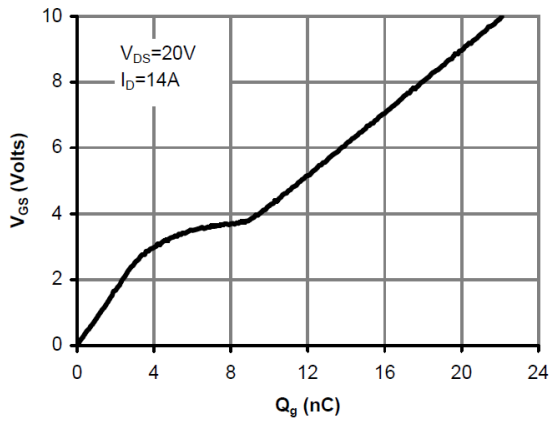


Figure 7: Gate-Charge Characteristics

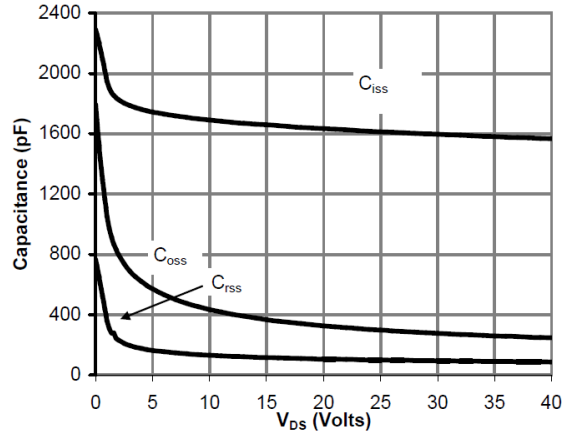


Figure 8: Capacitance Characteristics

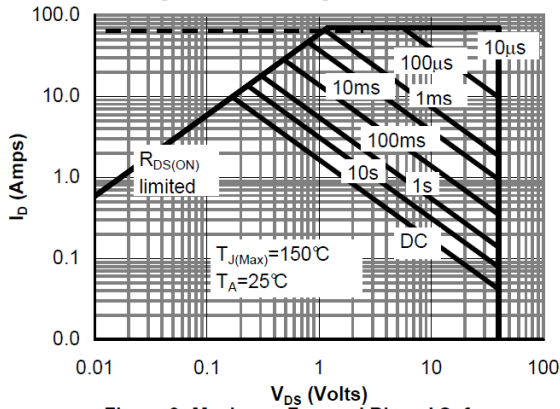


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

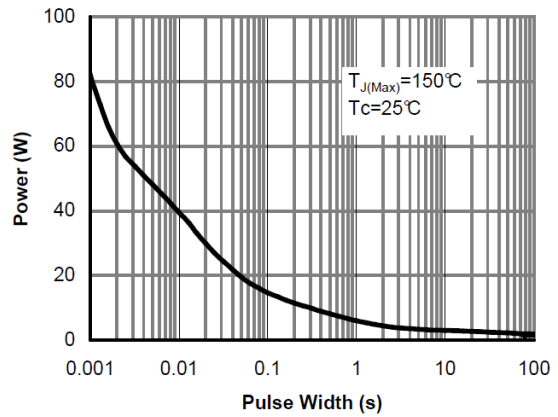


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

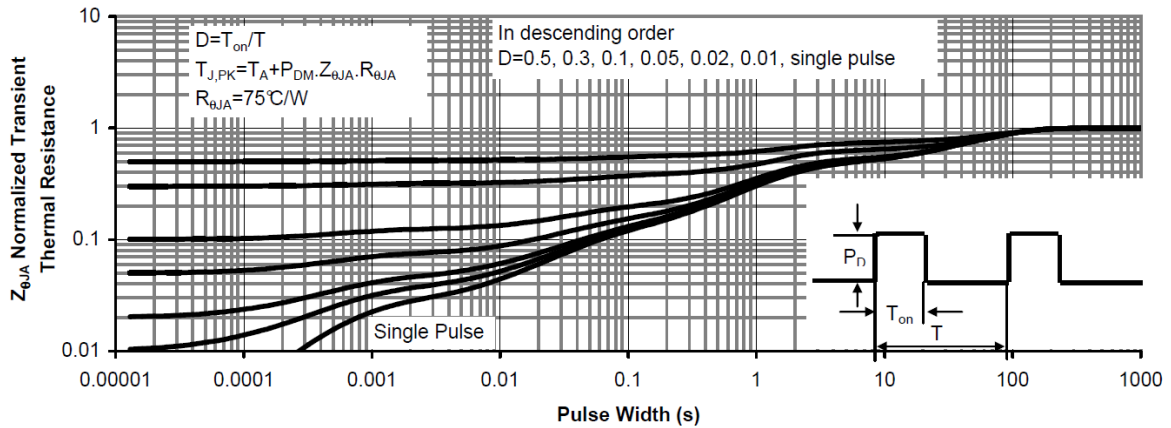
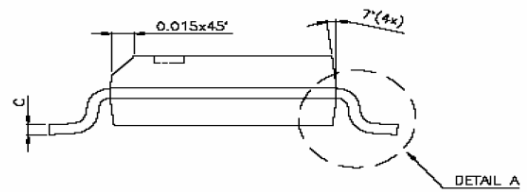
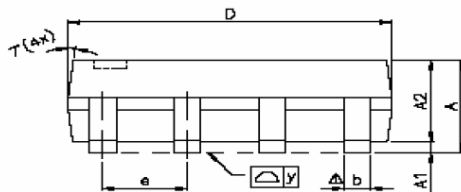
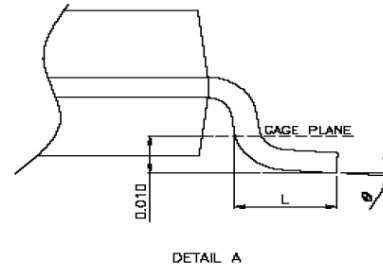
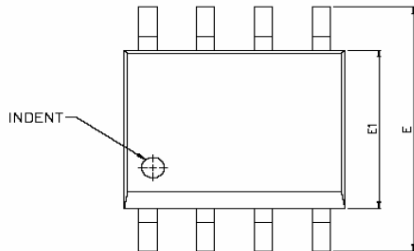


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

PACKAGE OUTLINE SOP-8P


SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	—	0.25	0.004	—	0.010
A2	—	1.45	—	—	0.057	—
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	—	1.27	—	—	0.050	—
L	0.38	0.71	1.27	0.015	0.028	0.050
Δ y	—	—	0.076	—	—	0.003
\varnothing	0°	—	8°	0°	—	8°