

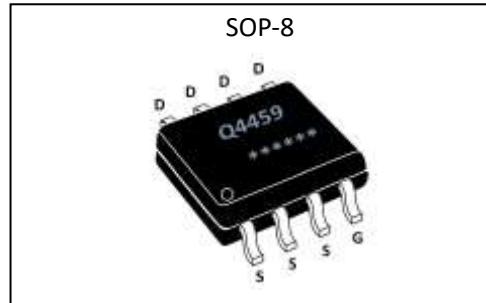
GL Silicon P-Channel Power MOSFET**General Description:**

The Q4459 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications. The package form is SOP-8, which accords with the RoHS standard.

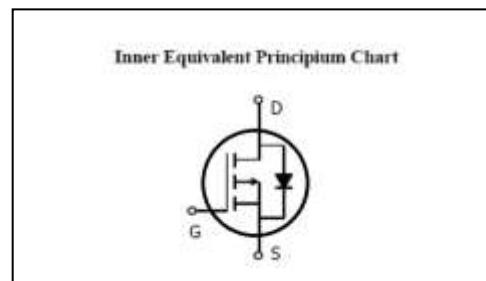
V_{DSS}	-30	V
I_D	-9.1	A
P_D	3.1	W
$R_{DS(ON)}\text{type}$	25	$\text{m}\Omega$

Features:

- $R_{DS(ON)} < 35\text{m}\Omega$ @ $V_{GS}=10\text{V}$ (Typ25mΩ)
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation

**Applications:**

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

**Absolute (T_c= 25°C unless otherwise specified):**

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	-30	V
I_D	Continuous Drain Current	-9	A
I_{DM}	Pulsed Drain Current	-45	A
V_{GS}	Gate-to-Source Voltage	± 20	V
P_D	Power Dissipation	3.1	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	155, -55 to 155	°C

GL Silicon P-Channel Power MOSFET
Electrical Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified):

OFF Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu\text{A}$	-30	--	--	V
I_{DSS}	Drain to Source Leakage Current	$V_{DS}=-30V, V_{GS}=0V, T_a=25^\circ\text{C}$	--	--	-1.0	μA
$I_{GSS(F)}$	Gate to Source Forward Leakage	$V_{GS}=+20V$	--	--	0.1	μA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	$V_{GS}=-20V$	--	--	-0.1	μA

ON Characteristics ^{a3}						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$	Drain-to-Source On-Resistance	$V_{GS}=-10V, I_D=-6.5A$	--	25	35	$\text{m}\Omega$
		$V_{GS}=-4.5V, I_D=-5.0A$		35	50	$\text{m}\Omega$
$V_{GS(\text{TH})}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu\text{A}$	-1.0	--	-3.0	V
Pulse width $t_p \leq 380\mu\text{s}, \delta \leq 2\%$						

Dynamic Characteristics ^{a4}						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
g_{fs}	Forward Transconductance	$V_{DS}=-15V, I_D=-6.5A$	10	--	--	S
C_{iss}	Input Capacitance	$V_{GS}=0V, V_{DS}=-15V$	--	1600	--	pF
C_{oss}	Output Capacitance	$f=1.0\text{MHz}$	--	350	--	
C_{rss}	Reverse Transfer Capacitance		--	300	--	

Resistive Switching Characteristics ^{a4}						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(\text{ON})}$	Turn-on Delay Time	$V_{DD}=-15V, I_D=-1A$	--	10	--	ns
t_r	Rise Time		--	15	--	
$t_{d(\text{OFF})}$	Turn-Off Delay Time		--	110	--	
t_f	Fall Time		--	70	--	
Q_g	Total Gate Charge	$V_{DD}=-15V, I_D=-9.1A$	--	30	--	nC
Q_{gs}	Gate to Source Charge		--	5.5	--	
Q_{gd}	Gate to Drain ("Miller")Charge		--	8	--	

**Q4459**

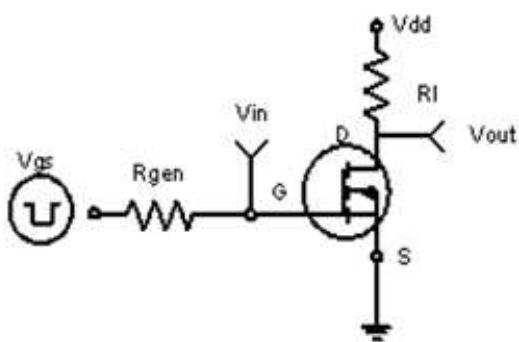
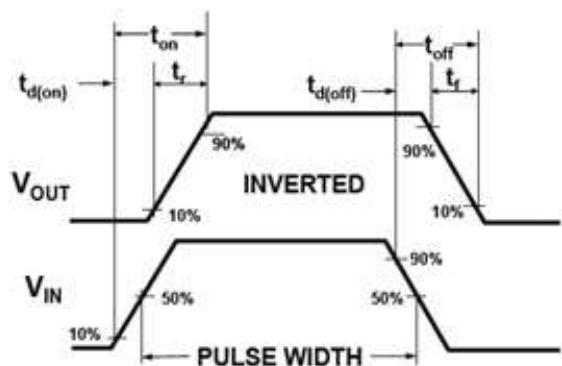
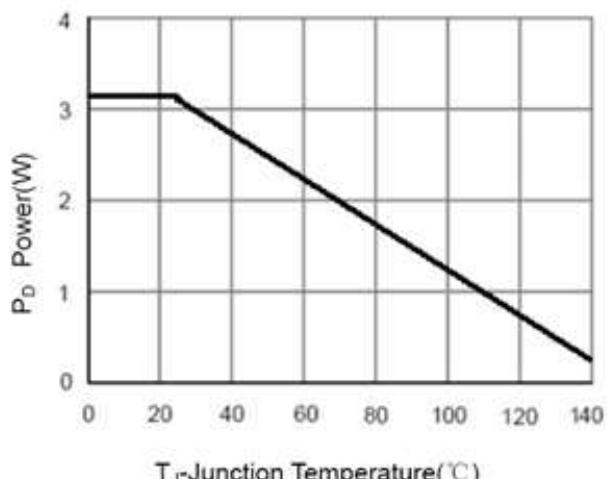
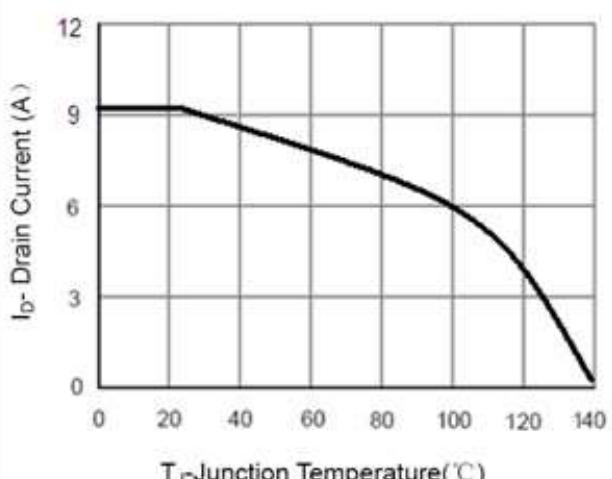
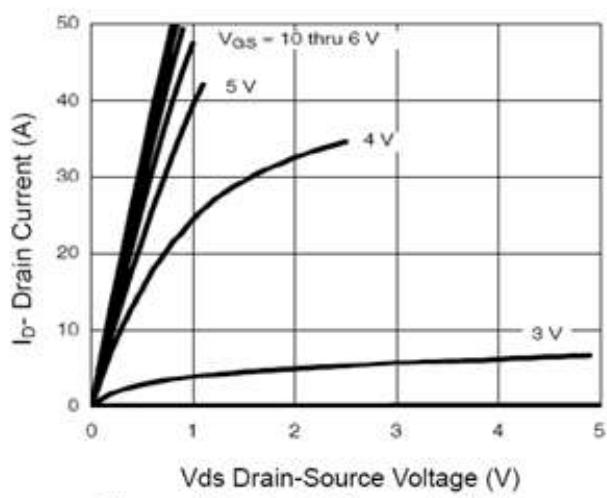
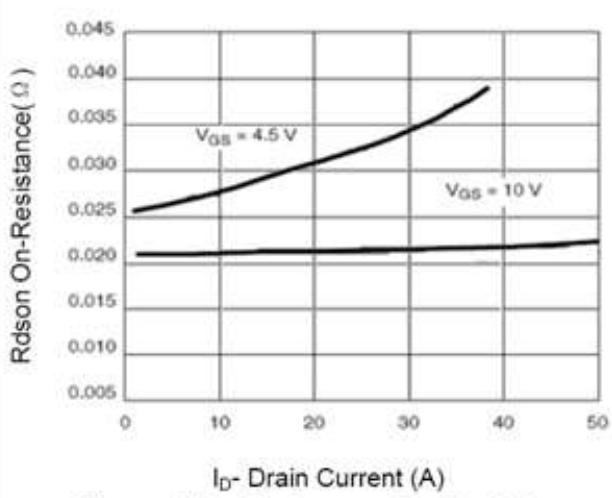
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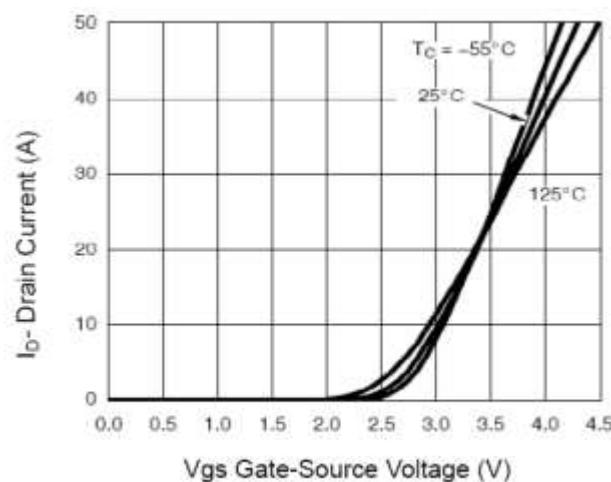
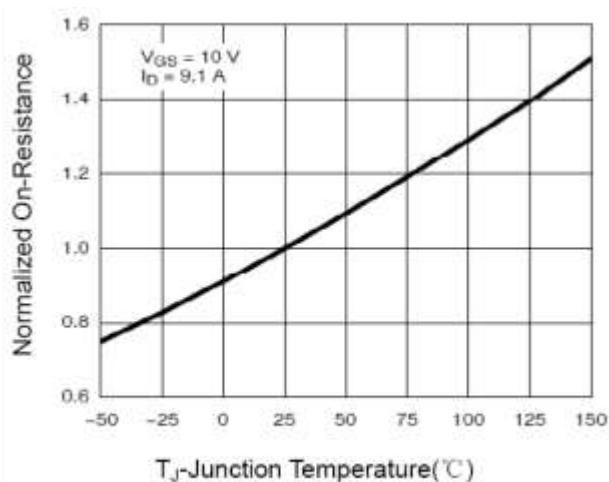
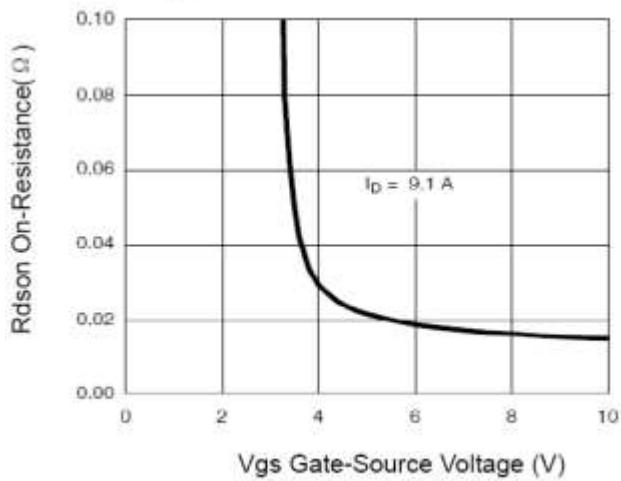
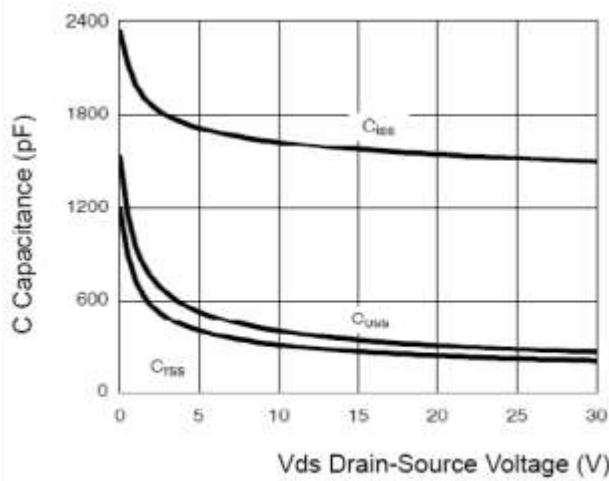
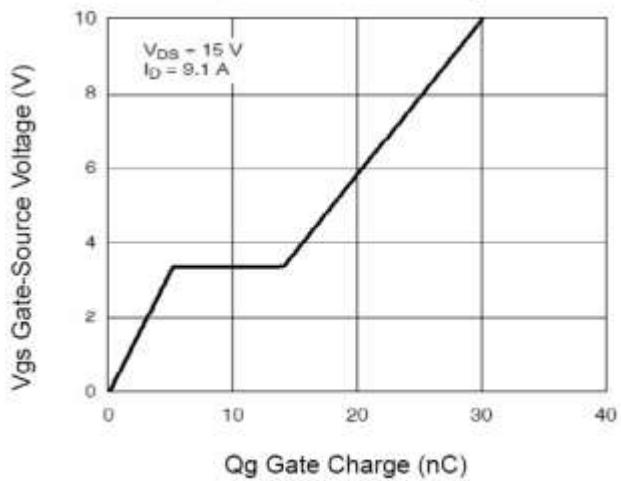
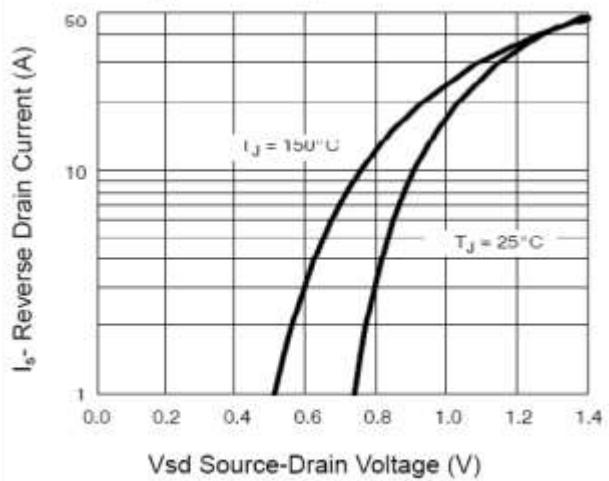
GL Silicon P-Channel Power MOSFET**Source-Drain Diode Characteristics**

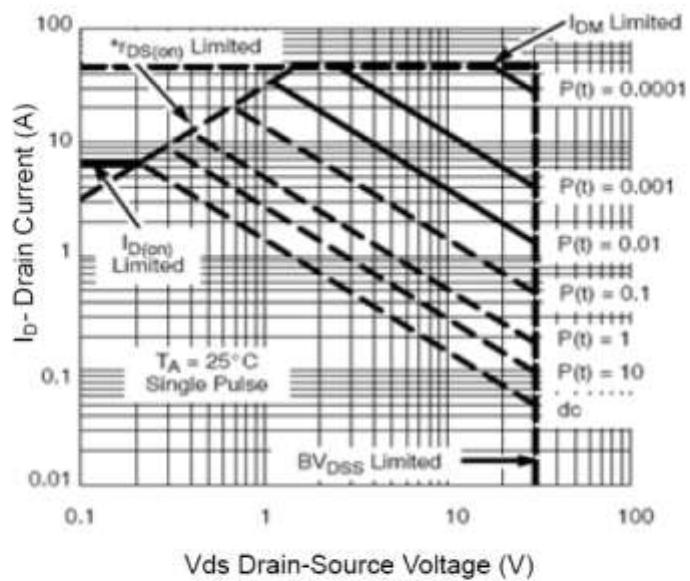
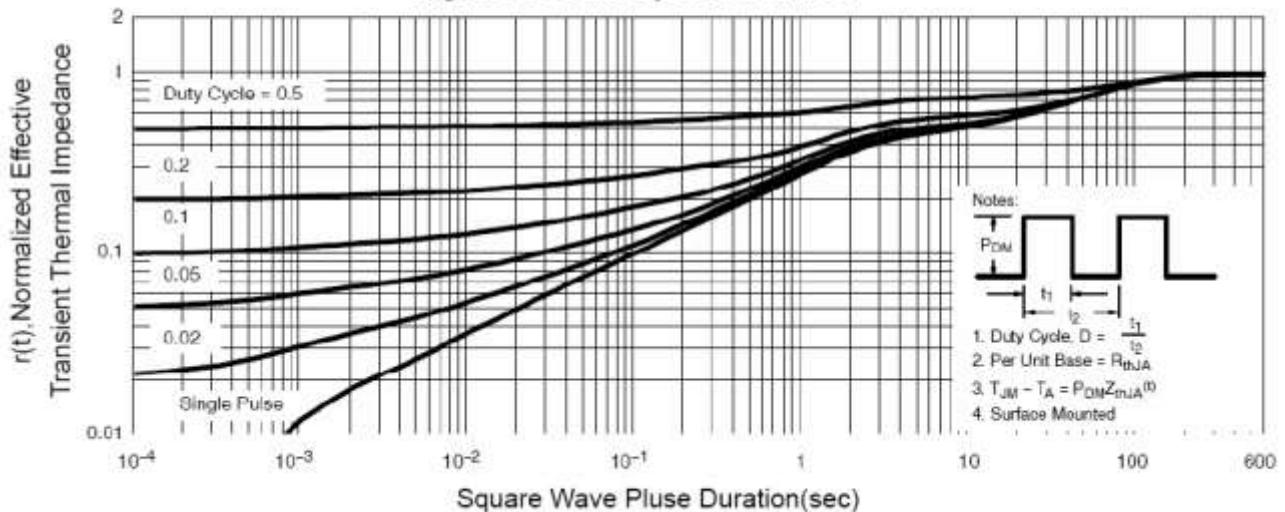
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_S	Continuous Source Current ^{a2} (Body Diode)		--	--	-9.1	A
V_{SD}	Diode Forward Voltage ^{a3}	$I_S = -2.1A, V_{GS} = 0V$	--	--	-1.2	V

Symbol	Parameter	Typ.	Units
$R_{\theta JC}$	Junction-to-Case ^{a2}	40	°C/W

^{a1}: Repetitive Rating: Pulse width limited by maximum junction temperature.^{a2}: Surface Mounted on FR4 Board, $t \leq 10\text{sec}$.^{a3}: Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.^{a4}: Guaranteed by design, not subject to production

GL Silicon P-Channel Power MOSFET
Test circuit & Thermal Characteristics

Figure 1:Switching Test Circuit

Figure 2:Switching Waveforms

Figure 3 Power Dissipation

Figure 4 Drain Current

Figure 5 Output Characteristics

Figure 6 Drain-Source On-Resistance

GL Silicon P-Channel Power MOSFET

Figure 7 Transfer Characteristics

Figure 8 Drain-Source On-Resistance

Figure 9 $R_{DS(on)}$ vs V_{GS}

Figure 10 Capacitance vs V_{DS}

Figure 11 Gate Charge

Figure 12 Source-Drain Diode Forward

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Figure 13 Safe Operation Area

Figure 14 Normalized Maximum Transient Thermal Impedance

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