ZD24C64B

I2C-Compatible (2-wire) Serial EEPROM
64-Kbit (8,192 x 8)
WL-CSP Datasheet

Features

- Low Voltage Operation
  - V_{CC} = 1.7V to 5.5V
- Internally Organized as 8,192 x 8 (64Kb)
- Additional Write lockable page
- 128-Bit Unique ID for each device[1]
- I^2C-compatible (2-wire) Serial Interface and high speed
  - 1MHz high speed, 1.7V to 5.5V
- Schmitt Trigger Filtered Inputs for Noise Suppression
- Bidirectional Data Transfer Protocol
- 32-byte Page Write Mode
  - Partial Page Writes Allowed
- Random and Sequential Read Modes
- Self-timed Write Cycle Within 5ms Max
- High Reliability
  - Endurance: 1,000,000 Write Cycles
  - Data Retention: 100 Years
- WL-CSP Features
  - Software Write Protection
  - Configurable Device Address

Note：

1. This feature is available on special order. Please contact Zetta for details.

Description

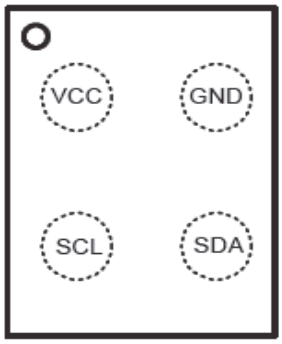
The ZD24C64B provides 65,536 bits of serial electrically erasable and programmable read-only memory (EEPROM) organized as 8,192 words of 8 bits each, with 32-byte Identification Page. The device's cascadable feature allows up to 8 devices to share a common 2-wire bus. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operations are essential.
This supplement contains information on the ZD24C64B in WL-CSP package. Please refer to the ZD24C64A datasheet for full specifications.

1. Pin Descriptions and Pinouts

Table 1-1.Pin Descriptions

Pin Symbol	Pin Name and Functional Description	Asserted State	Pin Type
GND	**Ground:** The ground reference for the power supply. GND should be connected to the system ground.	—	Power
SDA	**Serial Data:** The SDA pin is an open-drain bidirectional input/output pin used to serially transfer data to and from the device. The SDA pin must be pulled-high using an external pull-up resistor (not to exceed 10KΩ in value) and may be wire-ORed with any number of other open-drain or open-collector pins from other devices on the same bus.	—	Input/ Output
SCL	**Serial Clock:** The SCL pin is used to provide a clock to the device and to control the flow of data to and from the device. Command and input data present on the SDA pin is always latched in on the rising edge of SCL, while output data on the SDA pin is clocked out on the falling edge of SCL. The SCL pin must either be forced high when the serial bus is idle or pulled-high using an external pull-up resistor.	—	Input
V_{CC}	**Device Power Supply:** The V_{CC} pin is used to supply the source voltage to the device. Operations at invalid V_{CC} voltages may produce spurious results and should not be attempted.	—	Power

Thin 4-ball WLCSP(CT)



(TOP VIEW)

Ball pitch 400*400um

2. Memory Organization

ZD24C64B, 64K SERIAL EEPROM: Internally organized with 256 pages of 32 bytes each, the 64K requires a 13-bit data word address for random word addressing.

Identification Page： The ZD24C64B offers 32-byte Identification Page which can be written and (later) permanently locked in Read-only mode. This memory may be used by the system manufacturers to store security and other important information separately from the main memory array.

128 bits Unique: The ZD24C64B offers 128-bit Unique ID which can only be read.

Configurable Device Address: When power-on, the device will load the device address Configurations automatically. The CDA contains C0/C1/C2/CX four NVM bits. When CX is set to '1b', the device responds to all device address. Otherwise, the device only responds to the same device address as how C2/C1/C0 is set. The CDA factory default value is '0000b' for CT package.

CDA WREN: ZD24C64B offers a volatile register to protect CDA from unexpected write operation. Before writing CDA, the 'CDA WREN' register must be previously set to 1. Because the register will be automatically set to 0 after any read or write operation, the following command must be a 'Write CDA' command. The default value of 'CDA WREN' register after power-on is 0b.

Device ADDR	Page ADDR	Byte Number		
		32	……	0
1010	0	Data Memory (256P X 32Byte)		
	1			
	2			
	…..			
	255			
1011	xxxx x00x xxxx xxxx[1]	Identification Page(32byte)		
1011	xxxx x01x xxxx xxxx[2]	128 Bits Unique ID		
1011	xxxx x10x xxxx xxxx[3]	1 Bit Lock Bit		
1011	xx00 0110 1100 1010[4]	Configurable Device Address		
1011	xx11 1111 0011 0101[5]	CDA WREN		

Note：

1. Address bits ADDR<10:9> must be 00b, ADDR<4:0> define byte address, other bits are don't care.
2. Address bits ADDR<10:9> must be 01b, ADDR<3:0> define byte address, other bits are don't care.

3. Address bits ADDR<10:9> must be 10b, other bits are don't care.
4. Address bits ADDR<13:0> must be 00011011001010b, other bits are don't care.
5. Address bits ADDR<13:0> must be 11111100110101b, other bits are don't care.

3. CSP Configurations (CC)

Since there are no A0, A1, A2 and WP pins, ZD24C64B with WL-CSP package provides the CSP Configurations for users to implement Software Write Protection and Configurable Device Address features. When power-on, the device will load CSP Configurations automatically.

4. Configurable Device Address (CDA)

When power-on, the device will load the device address Configurations automatically. The CDA contains C0/C1/C2/CX four NVM bits. When CX is set to "1b", the device responds to all device address. Otherwise, the device only responds to the same device address as how C2/C1/C0 is set. The CDA factory default value is "0000b" for CT package.

5. CDA WREN

ZD24C64B offers a volatile register to protect CDA from unexpected write operation. Before writing CDA, the "CDA WREN" register must be previously set to 1. Because the register will be automatically set to 0 after any read or write operation, the following command must be a "Write CDA" command. The default value of "CDA WREN" register after power-on is 0b.

6. Software Write Protection (SWP)

If precautions are not taken, inadvertent writes may occur during transitions of the host system. ZD24C64B with WL-CSP package has provided SWP feature that will protect the memory against inadvertent writes. When SWP enabled, the memory will be read-only except SWP NVM bit. The SWP feature may be enabled (SWP=1'b) or disabled (SWP=0'b) by the user. The ZD24C64B WL-CSP package is shipped with SWP disabled.

7. Device Addressing

Data Memory/ Identification Page Access:

As shown in the Table 1 below, only A2/A1/A0 bits in device address were replaced by C2/C1/C0 respectively, the definitions of other bits in device address are the same with ZD24C64A full datasheet.

When CX is set to "0b", the 64K EEPROM uses the three device address bits C2, C1, C0 to allow as many as eight devices on the same bus. These bits must compare to C0/C1/C2 bits in Configurable Device Address. When CX is set to '1b', the device responds to any device address, thus only one device is allowed on each bus.

CC Access:

Access to this memory location is obtained by beginning the device address word with a '1011b' (Bh) sequence (refer to Table 1). The behavior of the next three bits (C2, C1 and C0) remains the same as during a standard memory addressing sequence.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

For more details on accessing this special feature, See Write Operations and Read Operations.

Table 1．Device Address

Access Area	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Data Memory	1	0	1	0	C2	C1	C0	R/W
Identification Page	1	0	1	1	C2	C1	C0	R/W
Identification Page Lock	1	0	1	1	C2	C1	C0	R/W
Unique ID Number	1	0	1	1	C2	C1	C0	1
CSP configurations	1	0	1	1	C2	C1	C0	R/W
CC WREN	1	0	1	1	C2	C1	C0	0

Table 2．First Word Address

Access Area	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Data Memory	X	X	X	A12	A11	A10	A9	A8
Identification Page	X	X	X	X	X	0	0	X
Identification Page Lock	X	X	X	X	X	1	0	X
Unique ID Number	X	X	X	X	X	0	1	X
CSP configurations	X	X	0	0	0	1	1	0
CC WREN	X	X	1	1	1	1	1	1

Notes:

1) X = Don`t care bit.

Table 3．Second Word Address

Access Area	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Data Memory	A7	A6	A5	A4	A3	A2	A1	A0
Identification Page	X	X	X	A4	A3	A2	A1	A0
Identification Page Lock	X	X	X	X	X	X	X	X
Unique ID Number	X	X	X	X	0	0	0	0
CSP configurations	1	1	0	0	1	0	1	0
CC WREN	0	0	1	1	0	1	0	1

Notes:

1) X = Don`t care bit.

8. Write Operations

WRITE CC

Before writing CC, a previously 'Write CC WREN' command must be performed. Write CC operation is similar to the byte write but requires use of device address, and specific word address. The word address bits ADDR<13:0> must be '00, 0110, 1100, 1010b' (see Table 2~3.), all other word address bits are don't care. The data byte must be equal to the binary value 'C2C1C0CXxxSWPx' (see Table 4 and Figure 1).

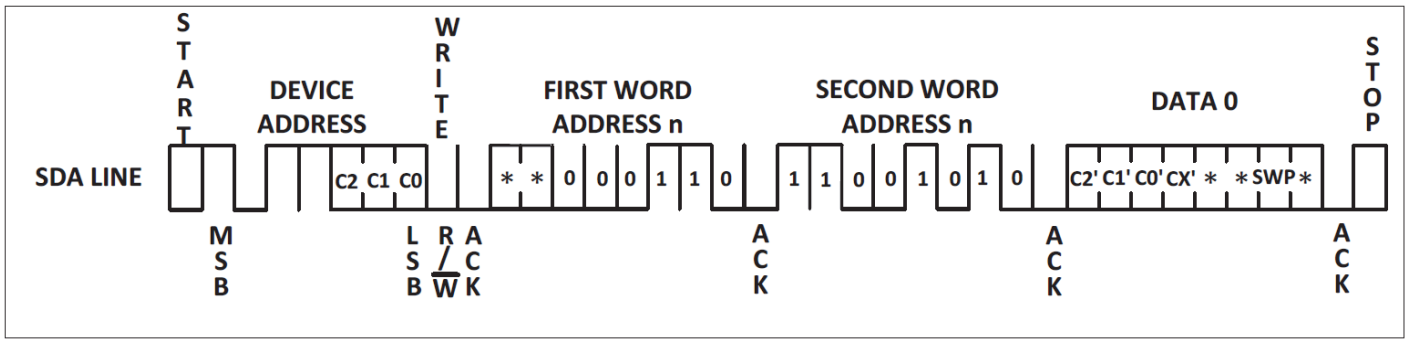
Table 4 . CDA and SWP Bits

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Write	C2	C1	C0	CX	X	X	SWP	X
Read	C2	C1	C0	CX	X	X	SWP	X

Notes:

1)X = Don`t care bit.

Figure 1. Write CC



C2/C1/C0 replace the traditional device address A2/A1/A0, CDA and SWP Bit defined as Table 4.

The factory default value of CDA is "0000b" for CT package and SWP bit is "0b" (SWP disabled). CDA could be configured when SWP is disabled. If SWP is disabled, CDA and SWP could be re- configured in the same write operations. Once CDA re-configured, the following command with device address bits must be in accordance with the modified CDA, otherwise the device will return to standby state. If SWP is enabled, CDA is protected by SWP. CDA can't be modified even during the SWP disable operation, the value of CDA (C2/C1/C0/ CX) in DATA0 of write CC command sequence is ignored.

Notes :

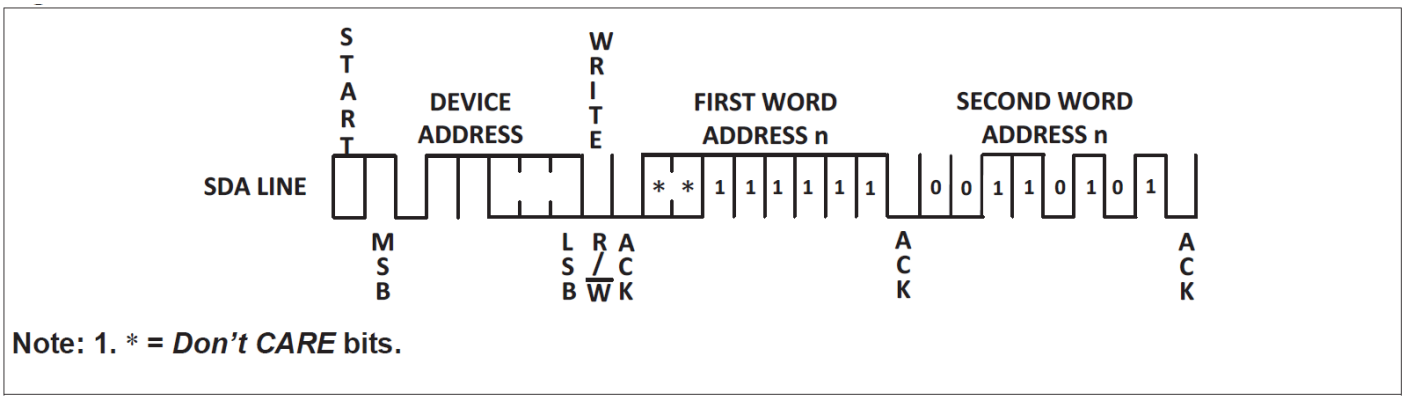
1) The CDA status could be checked by Ack polling. There will be an Ack when CDA value is the same as C2/C1/C0 in the device addresses of command sequence, otherwise NoAck.

2) Write CC operation support Ack polling to check whether the internal write cycle has completed.

WRITE CDA WREN

Write the 'CDA WREN' register is similar to the page write but requires use of device address, and the special word address seen in Table 1. The word address bits ADDR<13:0> must be 11111100110101b, all other word address bits are don't care. After the word address bytes, the register will be set and will be cleared after next command. That is, a following WRITE CDA command should be performed. For CDA WREN is a volatile register, no write cycle time or acknowledge polling is needed in this command (see Figure 2).

Figure 2. Write CC WREN



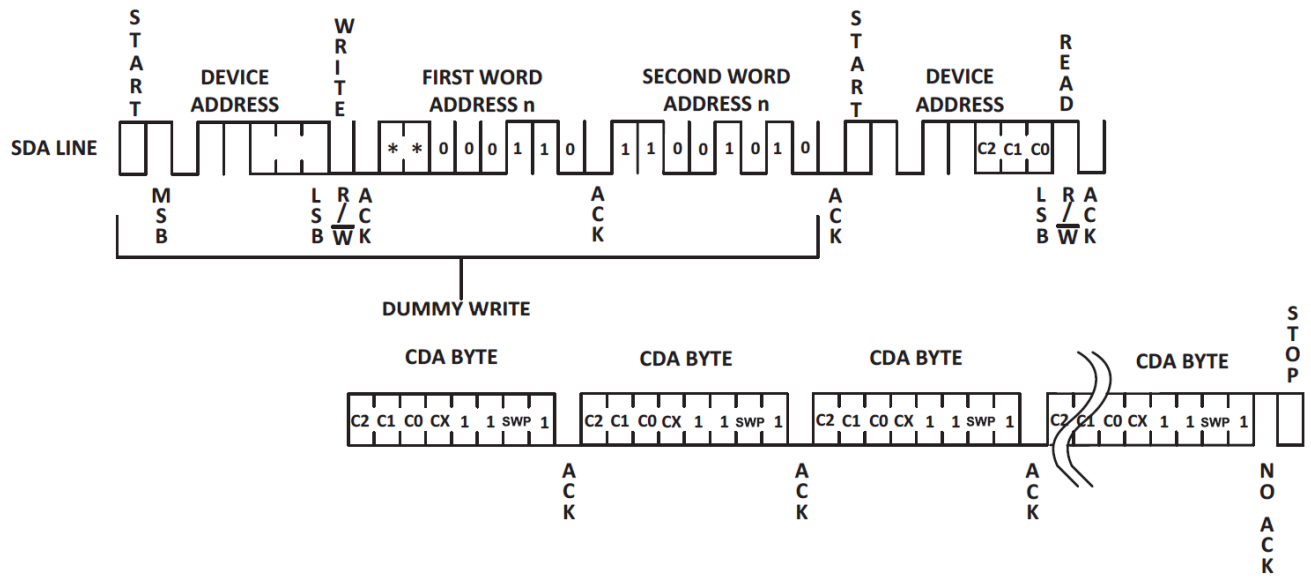
Note: 1. * = *Don't CARE* bits.

9. Read Operations

READ CC

Read CC operation is similar to the random read but requires use of device address, a dummy write, and specific word address. The word address bits ADDR<13:0> must be '00, 0110, 1100, 1010b' (see Table2~3), all other word address bits are don't care. The CDA is the BIT7~BIT4 of the byte read on SDA, and SWP is the BIT1, other bits are '1b'. The internal byte address is not automatically incremented, so the same data is shifted out repeatedly until the microcontroller does not respond with a zero but does generate a following stop condition (see Figure 3).

Figure 3. Read CC



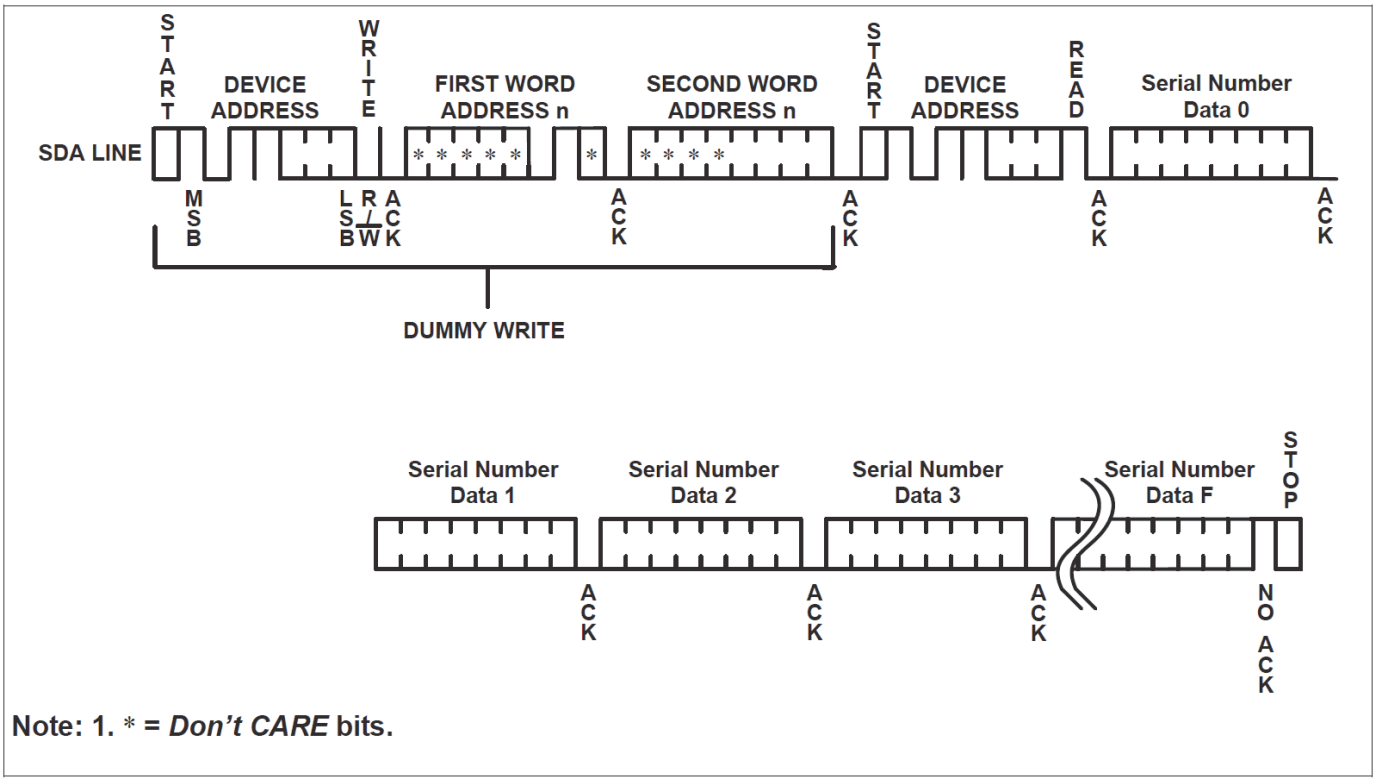
Note: 1. * = *Don't CARE* bits.

UNIQUE ID READ:

Reading the serial number is similar to the sequential read but requires use of the device address, a dummy write, and the use of specific word address seen in Table 1. The higher address bits ADDR<12:4> are don't care except for address bits ADDR<10:9> , which must be equal to '01b'. Lower address bits ADDR<3:0> define the byte address inside the UID. If the application desires to read the first byte of the UID, the lower address bits ADDR<3:0> would need to be '0000b'.

When the end of the 128-bit UID number is reached (16 bytes of data), the data word address will roll-over back to the beginning of the 128-bit UID number. The Unique ID Read operation is terminated when the microcontroller does not respond with a zero (ACK) and instead issues a Stop condition (see Figure 4).

Figure 4. Read Unique ID



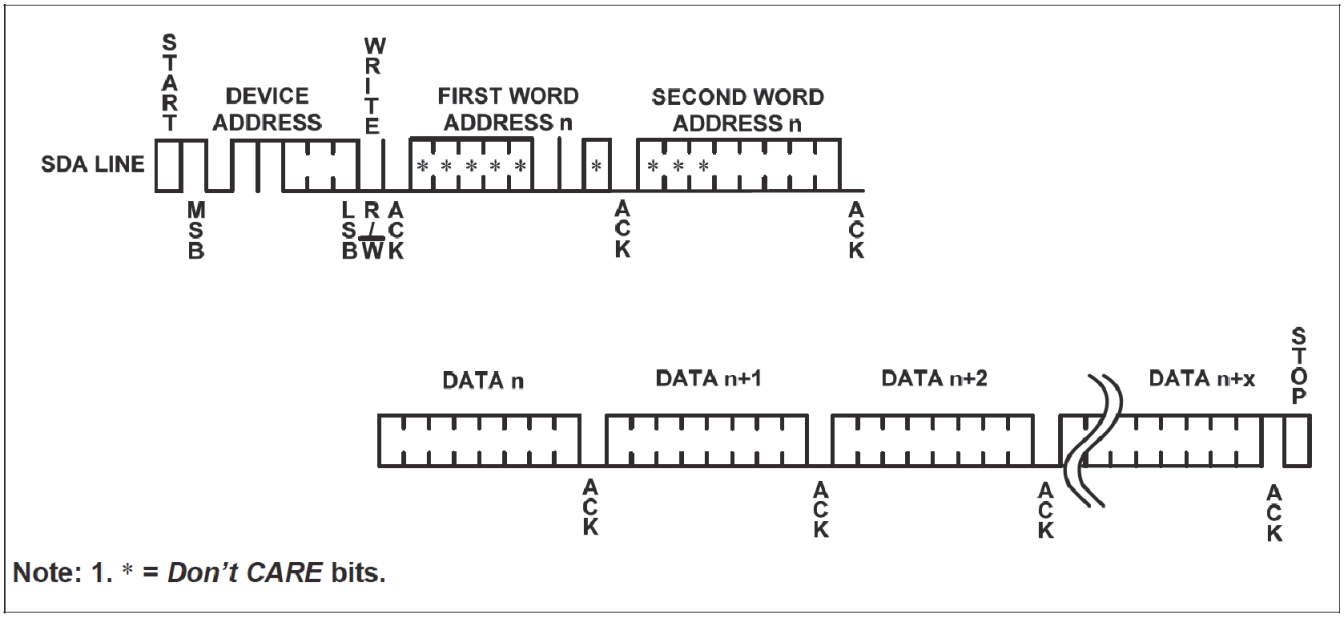
10. Identification Page

Write Identification Page

Write the Identification Page is similar to the page write but requires use of device address, and the special word address seen in Table 1 to Table 3. The higher address bits ADDR<12:5> are don't care except for address bits ADDR<10:9>，which must be equal to ' 00b'. Lower address bits ADDR<4:0> define the byte address inside the Security Sector (see Figure 5).

If the Identification Page is locked, the data bytes transferred during the Write Security Sector operation are not acknowledged (NoAck).

Figure 5. Write the Identification Page

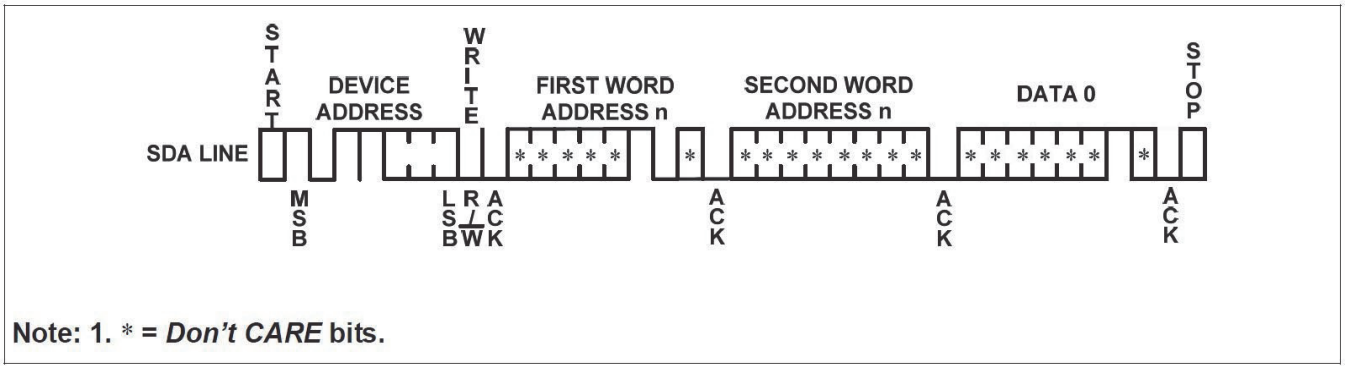


Identification Page Lock

Lock the Identification Page is similar to the byte write but requires use of device address, and special word address seen in Table 1 to Table 3. The word address bits ADDR<10:9> must be '10b', all other word address bits are don't care. The data byte must be equal to the binary value xxxx xx1x(see Figure 6).

If the Identification Page is locked, the data bytes transferred during the Identification Page Lock operation are not acknowledged (NoAck).

Figure 6. Identification Page Lock



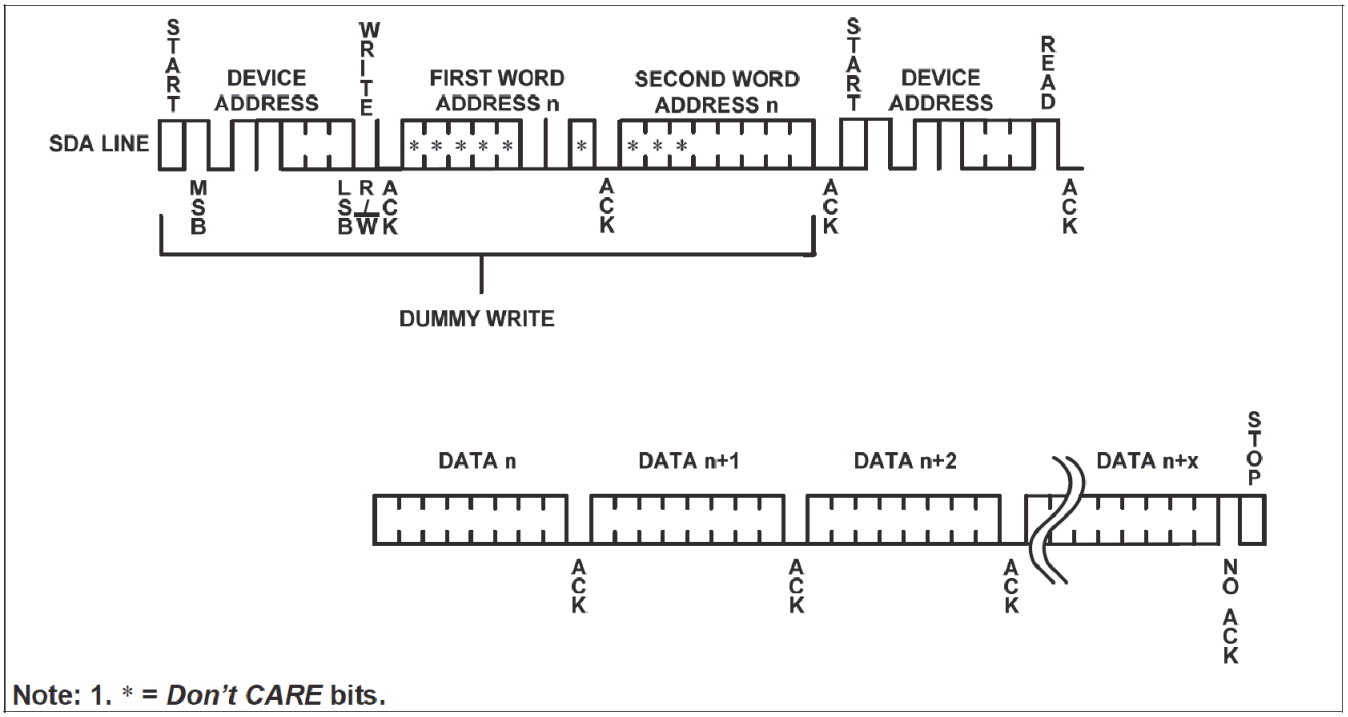
Read Identification Page

Read the Identification Page is similar to the random read but requires use of device address, a dummy write, and the use of specific word address seen in Table 2 and Table 3. The higher address bits ADDR<12:5> are don't care

except for address bits ADDR<10:9> , which must be equal to '00b'. The lower address bits ADDR<4:0> define the byte address inside the Identification Page.

The internal byte address is automatically incremented to the next byte address after each byte of data is clocked out. When the last byte (1Fh) is reached, it will roll over to 00h, the first byte of the Security Sector, and continue to increment. (see Figure 7).

Figure 7. Read Identification Page



Note: 1. * = *Don't CARE* bits.

Read Lock Status

There are two ways to check the lock status of the Identification Page.

1. The first way is initiated by an Identification Page Write, the EEPROM will acknowledge if the Security Sector is unlocked, while it will not acknowledge if the Identification Page is locked.

Once the acknowledge bit is read, it is recommended to generate a Start condition followed by a Stop condition, so that:

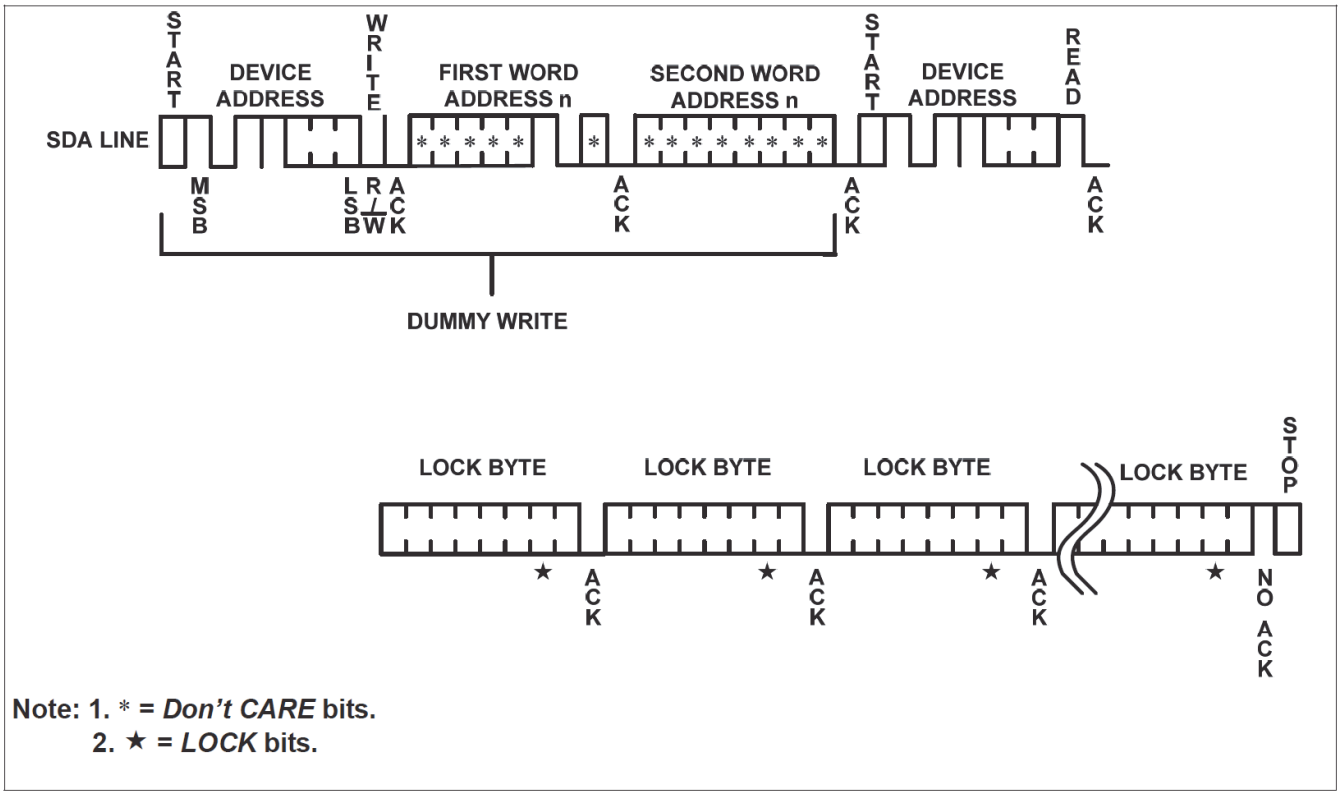
Start: the truncated command is not executed because the Start condition resets the device internal logic

Stop: the device is then set back into Standby mode by the Stop condition.

2. The second way is initiated by a Lock Status Read. Lock Status Read is similar to the random read but requires use of device address seen in Table 1, a dummy write, and the use of specific word address. The address bits ADDR<10:9> must be '10b', all other address bits are Don't Care. The Lock bit is the BIT1 of the byte read on SDA. It is at "1" when the lock is active and at "0" when the lock is not active.

The same data is shifted out repeatedly until the microcontroller does not respond with a zero but does generate a following stop condition (see Figure 8).

Figure 8. Read Lock Status



11. Pin Capacitance

SYMBOL	PARAMETER	CONDITIONS	Max	Units
C_{IN}[1]	Input Capacitance	VIN = 0V, f = 1MHz	6	pF
C_{OUT}[1]	Output Capacitance	VOUT = 0V, f = 1MHz	8	pF

Note: 1. This parameter is characterized and is not 100% tested.

12. DC Characteristics

Applicable over recommended operating range from: TA= -40°C to +85°C, VCC = +1.7V to +5.5V, (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC}	Supply Voltage		1.7		5.5	V
I_{CC1}	Supply Current	V_{CC} = 1.8V, Read at 400kHz		0.08	0.3	mA
		V_{CC} = 5.5V, Read at 1MHz		0.15	0.5	mA
I_{CC2}	Supply Current	VCC = 5.0V, Write at 1MHz		0.2	1	mA
I_{SB1}	Standby Current	VCC = 1.7V, VIN = VCC/GND		0.2	1	uA
I_{SB2}	Standby Current	VCC = 5.5V, VIN = VCC/GND		0.5	1	uA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}		0.1	3	uA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}		0.05	3	uA
V_{IL}[1]	Input Low Level		-0.6		VCCx0.3	V
V_{IH}[1]	Input High Level		VCCx0.7		VCC+0.5	V
V_{OL2}	Output Low Level	V_{CC} = 5.5V, I_{OL} = 2.1mA			0.4	V
V_{OL1}	Output Low Level	V_{CC} = 1.8V, I_{OL} = 0.15mA			0.2	V

Notes:
1. This parameter is characterized but is not 100% tested in production.

13. AC Characteristics

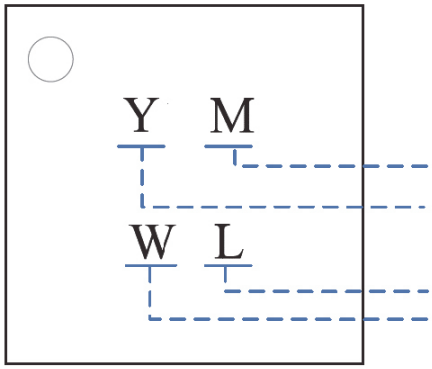
Recommended operating conditions: TA = -40°C to +85°C, VCC = +1.7V to +5.5V, CL = 100 pF (unless otherwise noted). Test conditions are listed in Note 2.

Symbol	Parameter	400KHz		1MHz		Units
		Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL		400		1000	KHz
t_{LOW}	Clock Pulse Width Low	1300		500		ns
t_{HIGH}	Clock Pulse Width High	600		400		
t_{I}[1]	Input Filter Spike Suppression		100		100	ns
t_{AA}	Clock Low to Data Out Valid		900		450	ns
t_{BUF}[1]	Bus Free Time between Stop and Start	1300		500		ns
$t_{HD.STA}$	Start Condition Hold Time	600		250		ns
$t_{SU.STA}$	Start Condition Set-up Time	600		250		ns
$t_{HD.DAT}$	Data In Hold Time	0		0		ns
$t_{SU.DAT}$	Data In Set-up Time	100		100		ns
t_{R}	Inputs Rise Time		300		100	ns

t_F	Inputs Fall Time		300		100	ns
$t_{SU.STO}$	Stop Condition Set-up Time	600		400		ns
t_{DH}	Data Out Hold Time	50		50		ns
t_{WR}	Write Cycle Time		5		5	ms

Notes: 1. This parameter is characterized and is not 100% tested.

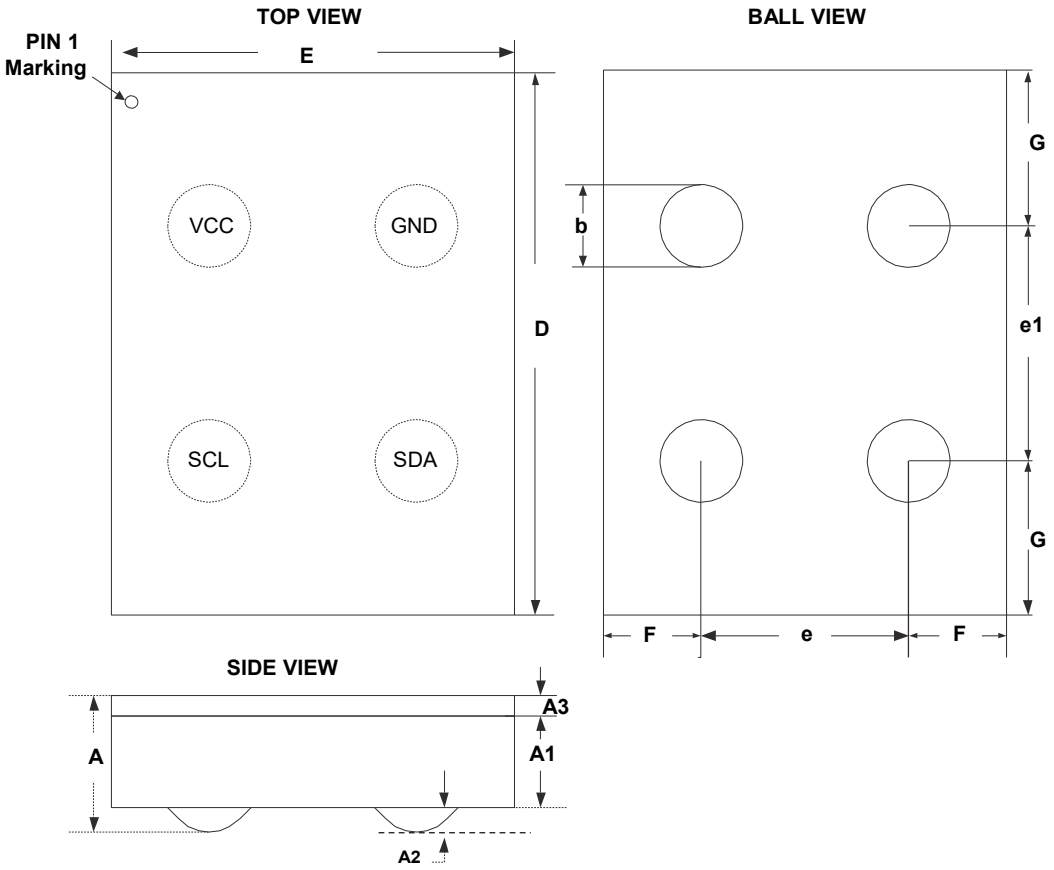
14. Part Marking Scheme



The month (hexadecimal digit) in which the product was molded.
The last one digit of the year In which the products was sealed / molded (just with 0~9)
Lot Number (just with a ~ z, A~Z, 0~9)
Product Density & Assembly's Code

15. Packaging Information

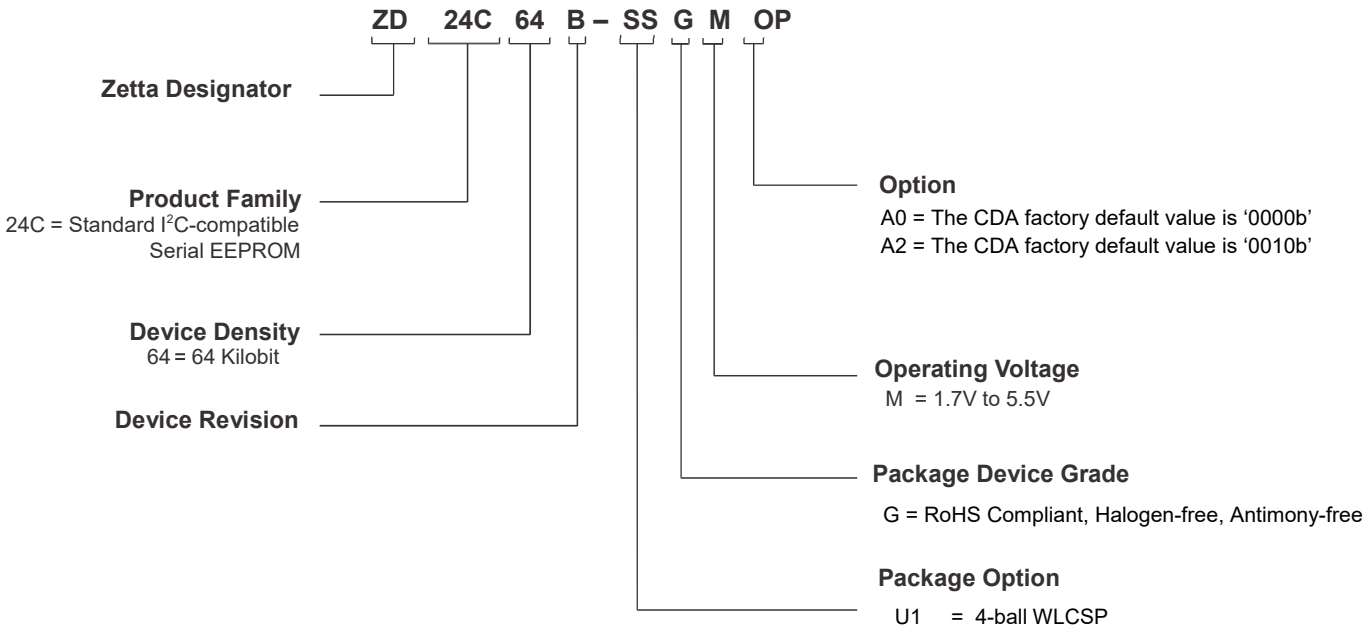
Thin 4-ball WLCSP



Symbol	Millimeters		
	Min	Typ	Max
A	0.260	0.280	0.300
b	-	0.160	-
A1	0.1875	0.200	0.2125
A2	0.0425	0.055	0.0575
A3	0.02	0.025	0.03
D	0.670	0.690	0.710
E	0.626	0.646	0.666
e	-	0.400	-
e1	-	0.400	-
F	-	0.116	-
G	-	0.139	-

NOTE: Dimensions are in Millimeters.

16. Ordering Information



17. Revision History

Version	Date	Comments
Preliminary	June. 2018	Initial document Release.
V1.1	Mar. 2019	Update package size(package D & E).