聯陽半導體
ITE Tech. Inc.

IT986x

Application Processor SoC

Preliminary Specification V0.1.0

ITE TECH. INC.

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Revision History

The contents below indicate the change between this version and the previous version only. The revision history shown in the previous version will not remain in the following table.

Date	Revision
2020/3/24	• Revise Video Input Interface Spec
2020/6/24	• Modify page ii, iii • Modify 1.Features : Audio Format, SARADC • Modify 2.2.6 add MIPI I/F • Modify 3.1 • Modify Table 5-1 • Modify Figure 5-6, Figure 5-9 • Remove 5.1.7 • Modify 6. DC Characteristics : -40 degree C • Remove 5.1.1 General Description: LCD common timing generator, LVDS interface
2020/7/1	• Add 5.1.7 MIPI Output Interface • Add 5.1.8 LVDS Interface
2020/7/16	• Modify Table 4-10 • Modify Table 4-11 • Modify 5.3.3.1 • Modify 5.3.3.2 • Modify Table 4-8
2020/9/30	• Modify 5.3.3.2
2020/11/30	• Modify Page12 VDD33_RTC pin number • Modify Figure 7-2 • Modify Table 7-2 • Modify 5.2 • Modify Page3 1.Features
2021/01/27	• Modify Features Display Interface Description • Modify Features CANBUS Controller • Add IT9866-C Part Number
2021/06/11	• Modify Features ADC and SPI • Modify Chapter 6 DC Electrical Characteristics • Add IT9868-AT Part Number
2021/08/04	• Remove IT9868-AT Part Number, to be included in a separate datasheet. • Modify Features of Stacked Memory Size • Modify 3.1 • Modify Ordering Information
2021/10/20	• Modify Features PWM • Modify 3. Block Diagram • Modify Table 4-10
2022/01/20	• Remove IT9866-C Part Number • CAN BUS support CAN 2.0 Only

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CONTENTS

FIGURES

TABLES

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1. Features

■ **Host Processor**
- 800MHz 32-bit ARM9 CPU1
- 32KB instruction cache
- 32KB data cache
- 400MHz 32-bit ARM9 CPU2
- 16KB instruction cache
- 16KB data cache

■ **Audio Format**
- Supports audio CODEC
- MP3

■ **Micro Controller**
- 324MHz 32-bit RISC CPU
- 16KB SRAM for instruction/data access

■ **Display Interface**
- 2160x1080 16/18/24 bpp (RGB565/RGB666/RGB888)
- Supports 16/18/24 bits RGB I/F and 8/9/16/18 bits CPU I/F
- Hardware 180°, mirror and flip rotate
- Supports CCIR601/CCIR656 interface
- Support LVDS interface (Maximum resolution: 1920X1080 pixel)
  - Maximum CLK rate of 140MHz
- Support MIPI interface (Maximum resolution:2160X1080 pixel)
  - D-PHY specification, Version 1.0, 1Gbps/lane

■ **2D Graphics Acceleration**
- Bit Block Transfer (BitBlt) with ROP3 operation
- Supports mask plan with 1bpp, 2bpp, 4bpp and 8bpp format.
- Supports color expansion with 1bpp, 2bpp, 4bpp and 8bpp format
- Coordinates transform
- Line draw with dash style
- One clipping window

■ **USB Host/Device**
- Provides one host/device controller
- Compliant with USB specification version 2.0
- Compatible with EHCI 1.0
- Supports point-to-point communications with one HS/FS/LS device
- Both host and device support isochronous/interrupt/control/bulk transfers
- Compatible with EHCI data structures

■ **SD/SDIO 3.0 Controller**
- Two MMC/SD/SDIO controller
- Fully compliant with MMCA v4.3
- 8 bits data of MMCA v4.3
- Compliant with SD/SDHC/SDXC
- FAT16/FAT32 boot loader

■ **NOR Flash Controller**
- Dedicated high speed SPI NAND/NOR controller.
- Supports SPI NAND/NOR flash
- Supports SPI serial mode, dual mode and quad mode
- Support maximum operating frequency at 80Mhz without pin share

■ **Ethernet MAC**
- Compliant with full IEEE 802.3-2002 specifications
- Supports IEEE 802.1Q VLAN tag detection for reception frames
- Supports CSMA/CD Protocol for Half-Duplex operation
- Supports IEEE 802.3x flow-control for Full-Duplex operation
- Supports IEEE 1588-2002 Time stamping on the transmit and received frames
- IEEE 802.3 compliant RMII PHY interface

■ **Audio Input/Output Interface**
- Record Five I2S interface
- Playback One I2S interface
- One embedded ADDA device:
  sample rates: 8~96KHz
  sample sizes: 16~24 bits

■ **Video Input Interface**
- Supports BT601:16/20-bit YCbCr 4:2:2
- Supports BT656:8/10/12-bit YCbCr 4:2:2
- Supports HD BT1120 interface
- Resolution: 1080p@ 60 fps(1920X1080)

■ **Video Signal Processor**
- Image and video scaling engine
- 4-Tap scalin**g** filter
- Configurable filter coefficients
- 2D deinterlace filter
- 3D deinterlace filter
- Support 2 layer High color OSD

■ **JPEG Encoder/Decoder**
- Fully compliant with Baseline JPEG standard ISO/IEC 10918
- Supports up to 256 million pixel (16376 * 16376)
- Supports 422, 420, 444 decode
- Supports 422, 420 encode
- Supports downloadable Quantization and Huffman table
- Supports motion JPEG for 720p@30fps (1280x720)

■ **Video Decoder**
- Support H.264/AVC decoding 1080p30@40Mbps
- Support error detection and concealment

■ **Cypher Engine**
- Compliant with the Publication 197 from NIST (AES) encryption/decryption with 128-bit key size
- Supports ECB, CBC, CFB, CTR and OFB operation mode

■ **Compress Engine**
- BriefLZ encode/decode
- UCL decode

■ **DMA**
- Provides 8 configurable DMA channels
- Supports chain transfer
- Memory-to-memory, memory-to-peripheral, and peripheral-to-peripheral transfer
- Group round-robin arbitration scheme with 4 priority levels
- Supports 8-, 16-, 32 and 64-bit wide data transaction
- Supports big-endian and little-endian

■ **Power Management**
- Flexible clock divider to slow down clock
- Dynamic gating clock
- Separate clock source to disable unused peripherals
- Wakeup from external event

■ **GPIO**
- Independent input, output and output enable buses for bi-directional I/O pins
- Each port can separately trigger the GPIO interrupt when it is programmed as input pin.
- Each port interrupt generation can be triggered by rising edge, falling edge, both edges, or high/low level when the interrupt option is set.

■ **IIC**
- Provides Four IIC interfaces
- All with fully mux GPIO output
- Supports standard (100kHz), and fast mode (400kHz) through programming the clock division register
- Supports 7-bit, 10-bit and general call addressing mode
- Glitch suppression throughout the de-bounce circuit
- Programmable slave address
- Master-transmit, Master-receive, Slave-transmit and Slave-receive modes provided
- Configurable multi-master mode supported
- Slave mode general call address detection

■ **UART/IrDA**
- Six UART interfaces
- All with fully MUX GPIO output
- Baud rate up to 6.25M bps
- Firmware compatible with high-speed NS 16C550A UART
- IrDA 1.3 SIR with up to 115.2kbps data rate
- SIR pulse width programmable as 1.6us or 3/16 of the baud-rate pulse width
- Supports IrDA 1.3 FIR
- Multi-frame transmission and reception in FIR mode

■ **Interrupt Controller**
- Provides both edge and level-triggered interrupt sources with positive and negative directions
- Provides de-bounce circuit for interrupt source

■ **PWM**
- Provides 8 independent 32-bit timers with PWM
- All with fully MUX GPIO output
- Programmable duty cycle and frequency
- Supports external clock source
- It can merge two timers into a 64-bit timer.
- Supports incrementing and decrementing mode

■ **SPI**
- Supports TI SSP, Motorola SPI, National Semiconductor Microwire, and SPIDIF interface
- Supports master and slave modes
- Internally or externally controlled serial bit clock
- Internally or externally controlled frame/sync
- Programmable frame/sync polarity
- Programmable serial bit clock polarity, phase, and frequency
- Programmable serial bit data sequence (MSB or LSB first)
- Programmable threshold interrupt of transmit/receive FIFO
- Supports 2 independent SPI interface

■ **RTC**
- Separated second, minute, hour, and day counter
- Programmable auto second, minute, hour or day alarm
- Generates power on signal when alarm occurs

■ **Remote in/out Controller**
- Hardware programmable to receive remote controller signal.
- Transfer data to remote signal
- Remote in signal with fully mux gpio input

■ **Wiegand in/out Controller**
- Provides two Wiegand in/out interface
- Support Wiegand 26/34/37 mode
- Supports up to maximum 128-bit code length
- Auto detects wiegand in code length

■ **Watch Dog**
- During timeout, outputs are system reset or interrupt.
- 32-bit down counter
- A variable time-out period of reset

■ **CANBUS Controller**
- Provides 2 independent CANBUS controller
- All with fully MUX GPIO output
- Supports CAN 2.0B
- Defines Data rates up to 1Mbit/s
- Single Shot Transmission Mode and Transceiver Standby Mode
- Time-stamping : ISO 11898-4 Time-Triggered CAN and CiA 603 time-stamping

■ **Booting**
- Configurable booting media select
- SD/MMC/eMMC(4-bit) booting
- SPI-NAND booting
- NOR booting

■ **SARADC**
- Configurable 8 channels input share the ADC
- 12-bits raw data per sample
- 1 MHz sample rate shared by 8 channels
- Single / Continuous / Group scan mode
- Software timer trigger start

■ **Stacked Memory Size**
- IT9862 Stacked 128Mb DDR2 Memory
- IT9866 Stacked 512Mb DDR2 Memory
- IT9868 Stacked 1Gb DDR3 Memory

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2. General Description

2.1 Introduction

The IT986x family is high performance HD display and high integrated SoC. (The IT986x family includes IT9862, IT9866 and IT9868 package.) It equips 2D Graphics Accelerator allowing for some special user interface designing, JPEG/H.264 HD decoding engine allowing users to have smooth experience while they are watching images and clips, audio engines allowing users to have joyful feeling while they are watching images and surely some other useful interfaces for users to have more flexible usage with their platform.

2.2 Multimedia Processor

2.2.1 High Performance 2D Graphics Accelerator

This engine supports bitblt, blending, rotation, scale and perspective transform function.

2.2.2 Powerful H.264 and JPEG Engine

The engines in the IT986x family offer users the ability to play those clips by video stream. The H.264 decode engine can perform up to 1920x1080p@30fps size clip decoding. Except for H.264 decode, IT986x family have JPEG engine inside. The JPEG engine can perform up to 256M-pixel still JPEG decoding and perform up to 1280x720p@30fps motion JPEG clip decoding. There is a video scaling engine for scaling up or down to the target display size.

2.2.3 Powerful Audio Solution

IT986x family embeds a 32-bit CPU and audio AD/DA. It can support MPEG-1 and MPEG-2 layer 2 audio decoder, MP3 decoder. Besides, it provides IIS as well and users can freely choose to whether to adopt another high performance IIS interface DAC or not when the performance and cost factors are taken into consideration.

2.2.4 High performance USB2.0 I/F

IT986x family supports a USB2.0 host or a USB2.0 device I/F, through which users can experience a high-speed data transfer.

2.2.5 Flexible SPI-NAND/NOR flash controller and flash card I/Fs

IT986x family have various external cards, I/F, SPI-NAND flash I/F and NOR flash I/F. About external cards I/F, IT986x family build in SD3.0/MMC card controllers. If users want some other external cards I/F, IT986x family provide a USB host I/F allowing for an external card bus chip.IT986x family provide SPI-NAND and NOR flash I/F. Besides SPI-NAND, NOR and SD are the other solutions for users to choose as a booting code storage space.

2.2.6 Display Interface

IT986x family supports various LCD I/Fs, such as RGB I/F, LVDS I/F, MIPI I/F and can support resolution up to 1920x1080 in the true color mode based on all of them. With the flexible display I/F, it will be easier to select the appreciate LCM required for users' platforms.

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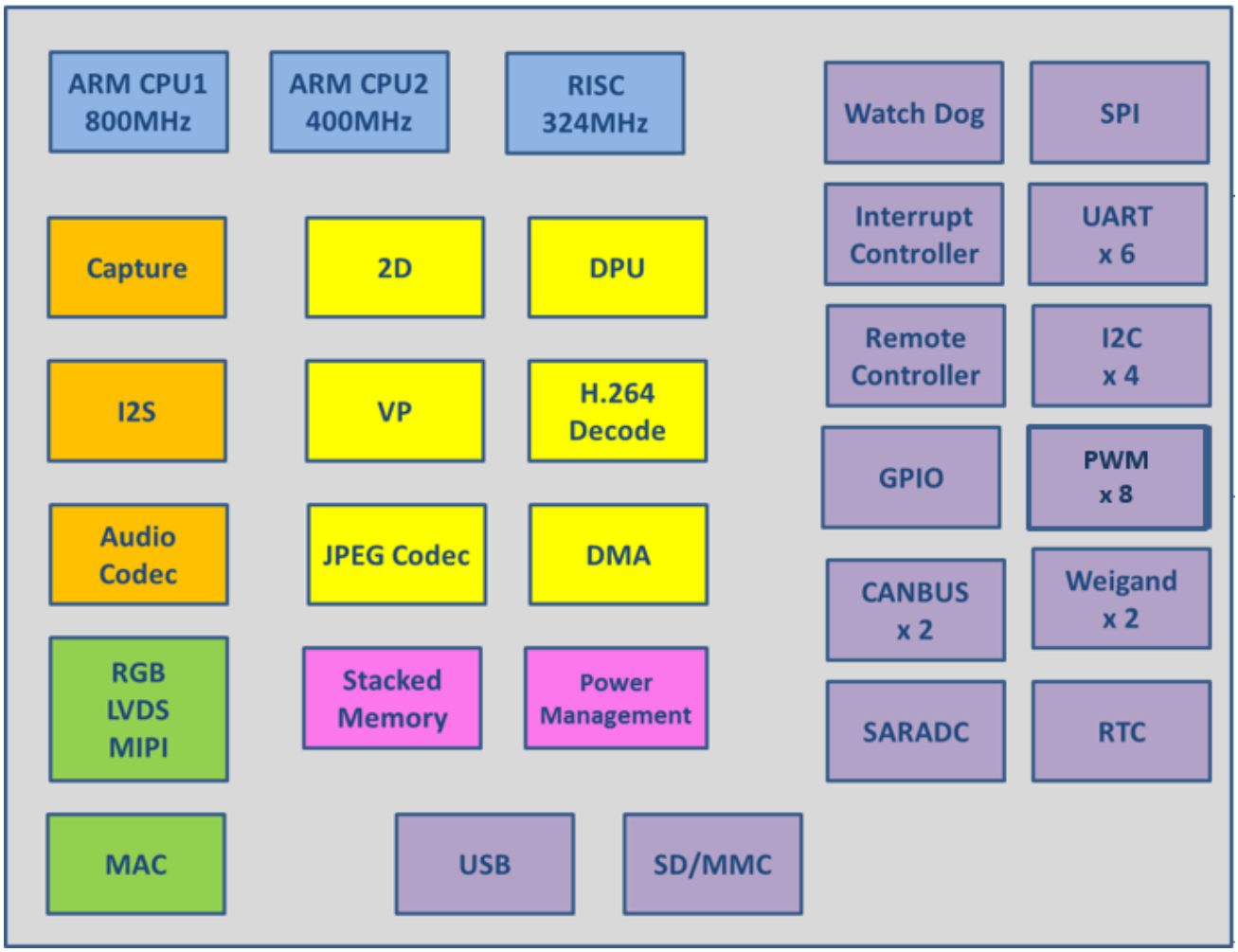
3. Block Diagram



3.1 Recommended Applications Function Configuration

	IT9862	IT9866	IT9868
Memory	128Mb DDR2	512Mb DDR2	1Gb DDR3
CPU	Dual ARM9 800M + 400MHz	Dual ARM9 800M + 400MHz	Dual ARM9 800M + 400MHz
Video Function	-	720p H.264 DECODER	1080p H.264 DECODER
Panel Interface	RGB, MIPI, LVDS	RGB, MIPI, LVDS	RGB, MIPI, LVDS
Panel Resolution	800*480	1280*800	2160*1080
Application	Home Appliances, Automotive Smart Display	Home Appliances, Automotive Smart Display, Smart Home	Home Appliances, Automotive Smart Display, Smart Home
Package	LQFP 128 pins (pin to pin)		

4. IT986x Family IC Description

4.1 IT986x

4.1.1 Pin Location

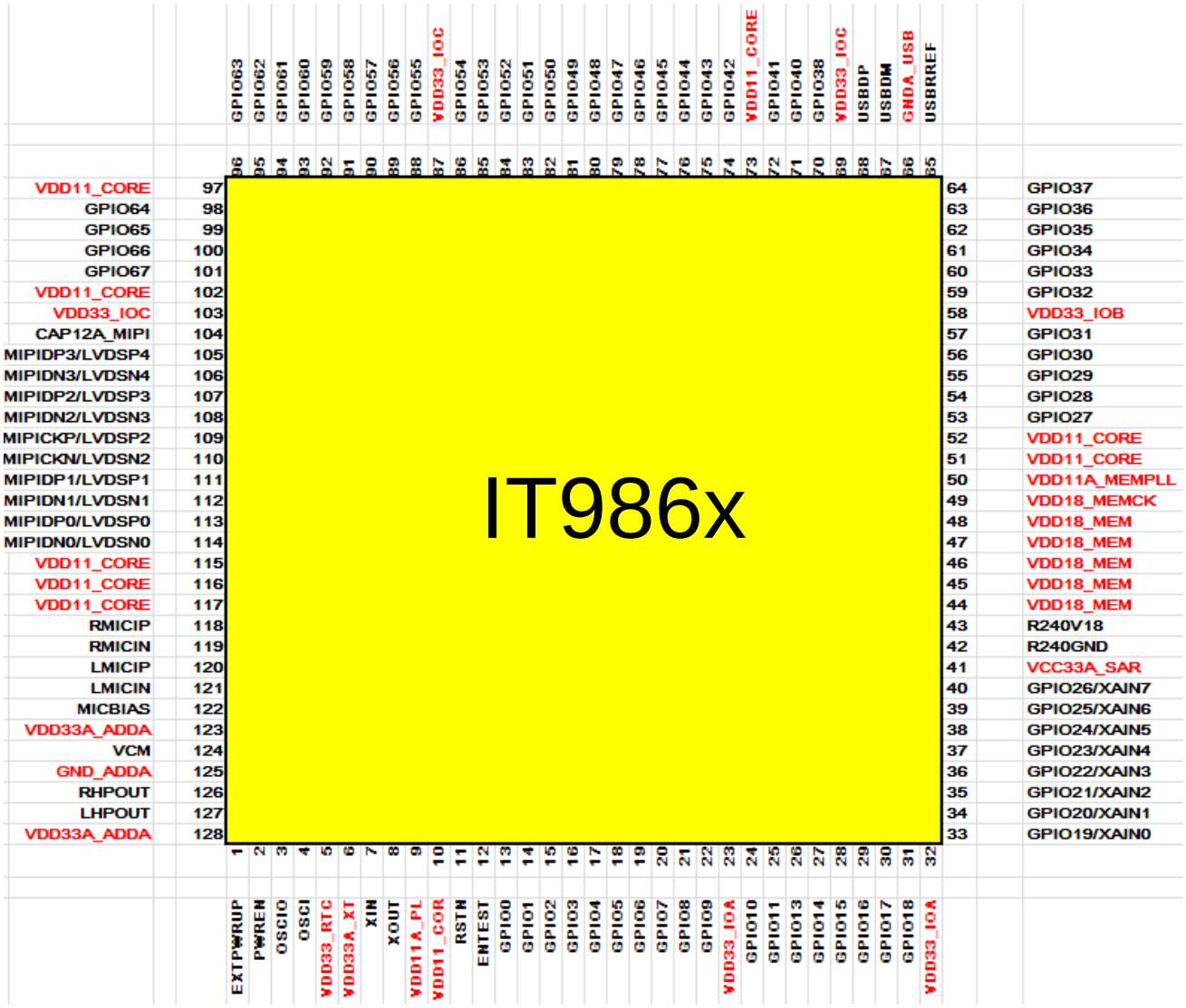


Table 4-1. IT986x Pins Listed in Numeric Order

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	EXTPWRUP	33	GPIO19/XAIN0	65	USBRREF	97	VDD11_CORE
2	PWREN	34	GPIO20/XAIN1	66	GNDA_USB	98	GPIO64
3	OSCIO	35	GPIO21/XAIN2	67	USBDM	99	GPIO65
4	OSCI	36	GPIO22/XAIN3	68	USBDP	100	GPIO66
5	VDD33_RTC	37	GPIO23/XAIN4	69	VDD33_IO	101	GPIO67
6	VDD33A_XTL	38	GPIO24/XAIN5	70	GPIO38	102	VDD11_CORE
7	XIN	39	GPIO25/XAIN6	71	GPIO40	103	VDD33_IO
8	XOUT	40	GPIO26/XAIN7	72	GPIO41	104	CAP12A_MIPI
9	VDD11A_PLL	41	VDD33A_SAR	73	VDD11_CORE	105	MIPIDP3/LVDSP4
10	VDD11_CORE	42	R240GND	74	GPIO42	106	MIPIDN3/LVDSN4
11	RSTN	43	R240V18	75	GPIO43	107	MIPIDP2/LVDSP3
12	ENTEST	44	VDD18_MEM	76	GPIO44	108	MIPIDN2/LVDSN3
13	GPIO0	45	VDD18_MEM	77	GPIO45	109	MIPICKP/LVDSP2
14	GPIO1	46	VDD18_MEM	78	GPIO46	110	MIPICKN/LVDSN2
15	GPIO2	47	VDD18_MEM	79	GPIO47	111	MIPIDP1/LVDSP1
16	GPIO3	48	VDD18_MEM	80	GPIO48	112	MIPIDN1/LVDSN1
17	GPIO4	49	VDD18_MEMCK	81	GPIO49	113	MIPIDP0/LVDSP0
18	GPIO5	50	VDD11A_MEMPLL	82	GPIO50	114	MIPIDN0/LVDSN0
19	GPIO6	51	VDD11_CORE	83	GPIO51	115	VDD11_CORE
20	GPIO7	52	VDD11_CORE	84	GPIO52	116	VDD11_CORE
21	GPIO8	53	GPIO27	85	GPIO53	117	VDD11_CORE
22	GPIO9	54	GPIO28	86	GPIO54	118	RMICIP
23	VDD33_IO	55	GPIO29	87	VDD33_IO	119	RMICIN
24	GPIO10	56	GPIO30	88	GPIO55	120	LMICIP
25	GPIO11	57	GPIO31	89	GPIO56	121	LMICIN
26	GPIO13	58	VDD33_IO	90	GPIO57	122	MICBIAS
27	GPIO14	59	GPIO32	91	GPIO58	123	VDD33A_ADDA
28	GPIO15	60	GPIO33	92	GPIO59	124	VCM
29	GPIO16	61	GPIO34	93	GPIO60	125	GND_ADDA
30	GPIO17	62	GPIO35	94	GPIO61	126	RHPOUT
31	GPIO18	63	GPIO36	95	GPIO62	127	LHPOUT
32	VDD33_IO	64	GPIO37	96	GPIO63	128	VDD33A_ADDA

Table 4-2. IT986x Pins Listed in Alphabetical Order

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
CAP12A_MIPI	104	GPIO34	61	GPIO64	98	USBRREF	65
ENTEST	12	GPIO35	62	GPIO65	99	VCM	124
EXTPWRUP	1	GPIO36	63	GPIO66	100	VDD11_CORE	10
GND_ADDA	125	GPIO37	64	GPIO67	101	VDD11_CORE	51
GNDA_USB	66	GPIO38	70	GPIO7	20	VDD11_CORE	52
GPIO0	13	GPIO4	17	GPIO8	21	VDD11_CORE	73
GPIO1	14	GPIO40	71	GPIO9	22	VDD11_CORE	97
GPIO10	24	GPIO41	72	LHPOUT	127	VDD11_CORE	102
GPIO11	25	GPIO42	74	LMICIN	121	VDD11_CORE	117
GPIO13	26	GPIO43	75	LMICIP	120	VDD11A_MEMPLL	50
GPIO14	27	GPIO44	76	MICBIAS	122	VDD11_CORE	116
GPIO15	28	GPIO45	77	MIPICKN/LVDSN2	110	VDD11_CORE	115
GPIO16	29	GPIO46	78	MIPICKP/LVDSP2	109	VDD11A_PLL	9
GPIO17	30	GPIO47	79	MIPIDN0/LVDSN0	114	VDD18_MEM	44
GPIO18	31	GPIO48	80	MIPIDP0/LVDSP0	113	VDD18_MEM	45
GPIO19/XAIN0	33	GPIO49	81	MIPIDN1/LVDSN1	112	VDD18_MEM	46
GPIO2	15	GPIO5	18	MIPIDP1/LVDSP1	111	VDD18_MEM	47
GPIO20/XAIN1	34	GPIO50	82	MIPIDN2/LVDSN3	108	VDD18_MEM	48
GPIO21/XAIN2	35	GPIO51	83	MIPIDP2/LVDSP3	107	VDD18_MEMCK	49
GPIO22/XAIN3	36	GPIO52	84	MIPIDN3/LVDSN4	106	VDD33_IO	23
GPIO23/XAIN4	37	GPIO53	85	MIPIDP3/LVDSP4	105	VDD33_IO	32
GPIO24/XAIN5	38	GPIO54	86	OSCI	4	VDD33_IO	58
GPIO25/XAIN6	39	GPIO55	88	OSCIO	3	VDD33_IO	69
GPIO26/XAIN7	40	GPIO56	89	PWREN	2	VDD33_IO	87
GPIO27	53	GPIO57	90	R240GND	42	VDD33_IO	103
GPIO28	54	GPIO58	91	R240V18	43	VDD33_RTC	3
GPIO29	55	GPIO59	92	RHPOUT	126	VDD33A_ADDA	123
GPIO3	16	GPIO6	19	RMICIN	119	VDD33A_ADDA	128
GPIO30	56	GPIO60	93	RMICIP	118	VDD33A_SAR	41
GPIO31	57	GPIO61	94	RSTN	11	VDD33A_XTL	6
GPIO32	59	GPIO62	95	USBDM	67	XIN	7
GPIO33	60	GPIO63	96	USBDP	68	XOUT	8

4.1.2 Pin Description

Table 4-3. Pin Description of Supplies Signals

Pin(s) No.	Symbol	Attribute	Power	Description
104	CAP12A_MIPI	Power		***MIPI Supply 1.2V***
10, 51, 52, 73, 97, 102, 115,116,117	VDD11_CORE	Power	-	***Digital Core Supply 1.1V***
50	VDD11A_MEMPLL	Power	-	***Memory phy PLL Supply 1.1V***
9	VDD11A_PLL	Power	-	***System PLL Supply 1.1V***
44, 45, 46, 47, 48	VDD18_MEM	Power	-	***Memory Chip Supply 1.8V***
49	VDD18_MEMCK	Power	-	***Memory Phy clock tree Supply 1.8V power***
23,32,58,69, 87,103	VDD33_IO	Power	-	***Chip IO Supply 3.3V***
5	VDD33_RTC	Power	-	***RTC Supply 3.3V***
123, 128	VDD33A_ADDA	Power	-	***ADDA Supply 3.3V***
41	VDD33A_SAR	Power		***SAR_ADC Supply 3.3V***
6	VDD33A_XTL	Power		***RTC crystal Supply 3.3V***
125	GND_ADDA	Ground		***Audio ADDA ground pin***
66	GNDA_USB	Ground		***USB ground pin***

Table 4-4. Pin Description of USB Signals

Pin(s) No.	Symbol	Attribute	Power	Description
67	USBDM	I/O	VDD33_IO	***USB data in data negative pin terminal***
68	USBDP	I/O	VDD33_IO	***USB data in data positive pin terminal***
65	USBRREF	I/O	VDD33_IO	***USB RREF current source, It needs to connect the 12-kΩ resistor***

Table 4-5. Pin Description of MIPI/LVDS Signals

Pin(s) No.	Symbol	Attribute	Power	Description
114	MIPIDN0/LVDSN0	O	VDD33_IO	***MIPI/ LVDS differential signal pair 0***
113	MIPIDP0/LVDSP0	O	VDD33_IO	***MIPI/ LVDS differential signal pair 0***
112	MIPIDN1/LVDSN1	O	VDD33_IO	***MIPI/ LVDS differential signal pair 1***
111	MIPIDP1/LVDSP1	O	VDD33_IO	***MIPI/ LVDS differential signal pair 1***
108	MIPIDN2/LVDSN3	O	VDD33_IO	***MIPI differential signal pair 2/ LVDS differential signal pair 3***
107	MIPIDP2/LVDSP3	O	VDD33_IO	***MIPI differential signal pair 2/ LVDS differential signal pair 3***
106	MIPIDN3/LVDSN4	O	VDD33_IO	***MIPI differential signal pair 3/ LVDS differential signal pair 4***
105	MIPIDP3/LVDSP4	O	VDD33_IO	***MIPI differential signal pair 3/ LVDS differential signal pair 4***
110	MIPICKN/LVDSN2	O	VDD33_IO	***MIPI differential signal pair CK/ LVDS differential signal pair 2***
109	MIPICKP/LVDSP2	O	VDD33_IO	***MIPI differential signal pair CK/ LVDS differential signal pair 2***

Table 4-6. Pin Description of ADDA Signals

Pin(s) No.	Symbol	Attribute	Power	Description
127	LHPOUT	O	VDD33A_ADDA	***Analog headphone output of the left channel***
126	RHPOUT	O	VDD33A_ADDA	***Analog headphone output of the right channel***

Pin(s) No.	Symbol	Attribute	Power	Description
124	VCM	I	VDD33A_ADDA	***Analog common-mode voltage***
122	MICBIAS	O	VDD33A_ADDA	***Analog microphone bias output***
121	LMICIN	I	VDD33A_ADDA	***Analog microphone input of the left channel Negative channel***
120	LMICIP	I	VDD33A_ADDA	***Analog microphone input of the left channel Positive channel***
119	RMICIN	I	VDD33A_ADDA	***Analog microphone input of the right channel Negative channel***
118	RMICIP	I	VDD33A_ADDA	***Analog microphone input of the right channel Positive channel***

Table 4-7. Pin Description of SARADC Signals

Pin(s) No.	Symbol	Attribute	Power	Description
33	XAIN0	I	VDD33A_SAR	***Analog voltage signal input for SARADC channel0***
34	XAIN1	I	VDD33A_SAR	***Analog voltage signal input for SARADC channel1***
35	XAIN2	I	VDD33A_SAR	***Analog voltage signal input for SARADC channel2***
36	XAIN3	I	VDD33A_SAR	***Analog voltage signal input for SARADC channel3***
37	XAIN4	I	VDD33A_SAR	***Analog voltage signal input for SARADC channel4***
38	XAIN5	I	VDD33A_SAR	***Analog voltage signal input for SARADC channel5***
39	XAIN6	I	VDD33A_SAR	***Analog voltage signal input for SARADC channel6***
40	XAIN7	I	VDD33A_SAR	***Analog voltage signal input for SARADC channel7***

Table 4-8. Pin Description of GPIO Signals

Pin(s) No.	Symbol	Attribute	Power	Description
13	GPIO0	I/O	VDD33_IO	***GPIO0***
14	GPIO1	I/O	VDD33_IO	***GPIO1***
15	GPIO2	I/O	VDD33_IO	***GPIO2***
16	GPIO3	I/O	VDD33_IO	***GPIO3***
17	GPIO4	I/O	VDD33_IO	***GPIO4***
18	GPIO5	I/O	VDD33_IO	***GPIO5***
19	GPIO6	I/O	VDD33_IO	***GPIO6***
20	GPIO7	I/O	VDD33_IO	***GPIO7***
21	GPIO8	I/O	VDD33_IO	***GPIO8***
22	GPIO9	I/O	VDD33_IO	***GPIO9***
24	GPIO10	I/O	VDD33_IO	***GPIO10***
25	GPIO11	I/O	VDD33_IO	***GPIO11***
26	GPIO13	I/O	VDD33_IO	***GPIO13***
27	GPIO14	I/O	VDD33_IO	***GPIO14***
28	GPIO15	I/O	VDD33_IO	***GPIO15***
29	GPIO16	I/O	VDD33_IO	***GPIO16***
30	GPIO17	I/O	VDD33_IO	***GPIO17***
31	GPIO18	I/O	VDD33_IO	***GPIO18***
33	GPIO19	I/O	VDD33_IO	***GPIO19 or XAIN0(SAR ADC channel0)***
34	GPIO20	I/O	VDD33_IO	***GPIO20 or XAIN1(SAR ADC channel1)***
35	GPIO21	I/O	VDD33_IO	***GPIO21 or XAIN2(SAR ADC channel2)***
36	GPIO22	I/O	VDD33_IO	***GPIO22 or XAIN3(SAR ADC channel3)***
37	GPIO23	I/O	VDD33_IO	***GPIO23 or XAIN4(SAR ADC channel4)***
38	GPIO24	I/O	VDD33_IO	***GPIO24 or XAIN5(SAR ADC channel5)***

Pin(s) No.	Symbol	Attribute	Power	Description
39	GPIO25	I/O	VDD33_IO	***GPIO25 or XAIN6(SAR ADC channel6)***
40	GPIO26	I/O	VDD33_IO	***GPIO26 or XAIN7(SAR ADC channel7)***
53	GPIO27	I/O	VDD33_IO	***GPIO27***
54	GPIO28	I/O	VDD33_IO	***GPIO28***
55	GPIO29	I/O	VDD33_IO	***GPIO29***
56	GPIO30	I/O	VDD33_IO	***GPIO30***
57	GPIO31	I/O	VDD33_IO	***GPIO31***
59	GPIO32	I/O	VDD33_IO	***GPIO32***
60	GPIO33	I/O	VDD33_IO	***GPIO33***
61	GPIO34	I/O	VDD33_IO	***GPIO34***
62	GPIO35	I/O	VDD33_IO	***GPIO35***
63	GPIO36	I/O	VDD33_IO	***GPIO36***
64	GPIO37	I/O	VDD33_IO	***GPIO37***
70	GPIO38	I/O	VDD33_IO	***GPIO38***
71	GPIO40	I/O	VDD33_IO	***GPIO40***
72	GPIO41	I/O	VDD33_IO	***GPIO41***
74	GPIO42	I/O	VDD33_IO	***GPIO42***
75	GPIO43	I/O	VDD33_IO	***GPIO43***
76	GPIO44	I/O	VDD33_IO	***GPIO44***
77	GPIO45	I/O	VDD33_IO	***GPIO45***
78	GPIO46	I/O	VDD33_IO	***GPIO46***
79	GPIO47	I/O	VDD33_IO	***GPIO47***
80	GPIO48	I/O	VDD33_IO	***GPIO48***
81	GPIO49	I/O	VDD33_IO	***GPIO49***
82	GPIO50	I/O	VDD33_IO	***GPIO50***
83	GPIO51	I/O	VDD33_IO	***GPIO51***
84	GPIO52	I/O	VDD33_IO	***GPIO52***
85	GPIO53	I/O	VDD33_IO	***GPIO53***
86	GPIO54	I/O	VDD33_IO	***GPIO54***
88	GPIO55	I/O	VDD33_IO	***GPIO55***
89	GPIO56	I/O	VDD33_IO	***GPIO56***
90	GPIO57	I/O	VDD33_IO	***GPIO57***
91	GPIO58	I/O	VDD33_IO	***GPIO58***
92	GPIO59	I/O	VDD33_IO	***GPIO59***
93	GPIO60	I/O	VDD33_IO	***GPIO60***
94	GPIO61	I/O	VDD33_IO	***GPIO61***
95	GPIO62	I/O	VDD33_IO	***GPIO62***
96	GPIO63	I/O	VDD33_IO	***GPIO63***
98	GPIO64	I/O	VDD33_IO	***GPIO64***
99	GPIO65	I/O	VDD33_IO	***GPIO65***
100	GPIO66	I/O	VDD33_IO	***GPIO66***
101	GPIO67	I/O	VDD33_IO	***GPIO67***
105	GPIO68	I/O	VDD33_IO	***GPIO68***
106	GPIO69	I/O	VDD33_IO	***GPIO69***
107	GPIO70	I/O	VDD33_IO	***GPIO70***
108	GPIO71	I/O	VDD33_IO	***GPIO71***
109	GPIO72	I/O	VDD33_IO	***GPIO72***
110	GPIO73	I/O	VDD33_IO	***GPIO73***
111	GPIO74	I/O	VDD33_IO	***GPIO74***
112	GPIO75	I/O	VDD33_IO	***GPIO75***
113	GPIO76	I/O	VDD33_IO	***GPIO76***
114	GPIO77	I/O	VDD33_IO	***GPIO77***

Table 4-9. Pin Description of Misc Signals

Pin(s) No.	Symbol	Attribute	Power	Description
3	OSCIO	O	VDD11A_PLL	***RTC Crystal 32.768KHz Output***
4	OSCI	I	VDD11A_PLL	***RTC Crystal 32.768KHz Input***
7	XIN	I	VDD33A_XTL	***System Crystal 12MHz Input***
8	XOUT	I	VDD33A_XTL	***System Crystal 12MHz output***

Pin(s) No.	Symbol	Attribute	Power	Description
11	RSTN	I	VDD33_IO	***Reset***
12	ENTEST	I	VDD33_IO	***Test Enable***
42	R240GND	I	VDD18_MEM	Pad to the precise internal resistor for compensation the pull-up driver. Tied to Ground through a 240 ohm resistor with 1% tolerance.
43	R240V18	I	VDD18_MEM	Pad to the precise internal resistor for compensation the pull-down driver. Tied to 1.8V through a 240 ohm resistor with 1% tolerance.

4.1.3 Shared GPIO Pin

Table 4-10. Shared GPIO Pin Table

Pin Name	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4
GPIO0	GPIO0				
GPIO1	GPIO1				
GPIO2	GPIO2				
GPIO3	GPIO3				
GPIO4	GPIO4				
GPIO5	GPIO5	AXISPI_CS0			
GPIO6	GPIO6	AXISPI_D0	SD0_D0		
GPIO7	GPIO7	AXISPI_D1	SD0_D1		
GPIO8	GPIO8	AXISPI_D2	SD0_D2		
GPIO9	GPIO9	AXISPI_D3	SD0_D3		
GPIO10	GPIO10	AXISPI_CLK			
GPIO11	GPIO11	AXISPI_CS1	SD1_CLK		
GPIO13	GPIO13		SD0_CMD		
GPIO14	GPIO14		SD0_CLK		
GPIO15	GPIO15		SD0_D0	SPI1_CLK	
GPIO16	GPIO16		SD0_D1	SPI1_CS0	
GPIO17	GPIO17		SD0_D2	SPI1_DO	
GPIO18	GPIO18		SD0_D3	SPI1_DI	
GPIO19/XAIN0	GPIO19	WO1_D0		SPI0_CLK	RX_ZD1
GPIO20/XAIN1	GPIO20	WO1_D1		SPI0_CS0	RX_ZD2
GPIO21/XAIN2	GPIO21	IrDA_RXL		SPI0_DO	RX_ZD3
GPIO22/XAIN3	GPIO22	IrDA_TX		SPI0_DI	
GPIO23/XAIN4	GPIO23	WO0_D0		SPI0_CS1	
GPIO24/XAIN5	GPIO24	WO0_D1		SPI0_CLK	
GPIO25/XAIN6	GPIO25	WO1_D0		SPI0_CS0	
GPIO26/XAIN7	GPIO26	WO1_D1			
GPIO27	GPIO27	MDIO		SPI0_CLK	
GPIO28	GPIO28	MDC		SPI0_CS0	
GPIO29	GPIO29	TXD1		SPI0_DO	
GPIO30	GPIO30	TXD0			
GPIO31	GPIO31	TXEN			
GPIO32	GPIO32	TXC	SD1_CLK		
GPIO33	GPIO33	RX_CRS_DV	SD1_CMD	SPI0_DI	
GPIO34	GPIO34	RXD0	SD1_D0	SPI1_CLK	WO0_D0
GPIO35	GPIO35	RXD1	SD1_D1	SPI1_CS0	WO0_D1
GPIO36	GPIO36	RXER	SD1_D2	SPI1_DO	WO1_D0
GPIO37	GPIO37	INTB	SD1_D3	SPI1_DI	WO1_D1
GPIO38	GPIO38	LDCLK	VD0*$_2$	SPI1_CLK	
GPIO40	GPIO40	LD1*$_1$	VD2*$_2$	SPI1_DO	
GPIO41	GPIO41	LD2*$_1$	VD3*$_2$	SPI1_DI	
GPIO42	GPIO42	LD3*$_1$	VD4*$_2$	SPI1_CS1	SD1_CLK
GPIO43	GPIO43	LD4*$_1$	VD5*$_2$		SD1_CMD
GPIO44	GPIO44	LD5*$_1$	VD6*$_2$		SD1_D0
GPIO45	GPIO45	LD6*$_1$	VD7*$_2$		SD1_D1
GPIO46	GPIO46	LD7*$_1$	VD8*$_2$		SD1_D2
GPIO47	GPIO47	LD8*$_1$	VD9*$_2$	WO0_D0	SD1_D3
GPIO48	GPIO48	LD9*$_1$	VD10*$_2$	WO0_D1	SD1_D4
GPIO49	GPIO49	LD10*$_1$	VD11*$_2$	WO1_D0	SD1_D5
GPIO50	GPIO50	LD11*$_1$	VD12*$_2$	WO1_D1	LDCLK
GPIO51	GPIO51	LD12*$_1$	VD13*$_2$	SD0_CLK	SD1_D6
GPIO52	GPIO52	LD13*$_1$	VD14*$_2$	SD0_CMD	SD1_D7
GPIO53	GPIO53	LD14*$_1$	VD15*$_2$	SD0_D0	
GPIO54	GPIO54	LD15*$_1$	VD16*$_2$	SD0_D1	
GPIO55	GPIO55	LD16*$_1$	VD17*$_2$	SD0_D2	RX_ZCLK
GPIO56	GPIO56	LD17*$_1$	VD18*$_2$	SD0_D3	RX_ZWS
GPIO57	GPIO57	LD18*$_1$	VD19*$_2$	SD0_D4	RX_ZD0

Pin Name	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4
GPIO58	GPIO58	LD19*1	VD20*2	SD0_D5	RX_AMCLK
GPIO59	GPIO59	LD20*1	VD21*2	SD0_D6	LDCLK
GPIO60	GPIO60	LD21*1	VD22*2	SD0_D7	RX_ZCLK
GPIO61	GPIO61	LD22*1	VD23*2	SD1_D1	RX_ZWS
GPIO62	GPIO62	LD23*1	VD24*2	SD1_CMD	RX_ZD0
GPIO63	GPIO63	LD24*1	VD25*2	SD1_CLK	RX_AMCLK
GPIO64	GPIO64	LD25*1			
GPIO65	GPIO65	LD26*1			
GPIO66	GPIO66	LD27*1			
GPIO67	GPIO67	LD28*1			
MIPIDP3/LVDSP4	GPIO68	LD29*1			
MIPIDN3/LVDSN4	GPIO69	LD30*1			
MIPIDP2/LVDSP3	GPIO70	LD31*1			
MIPIDN2/LVDSN3	GPIO71	LD32*1			
MIPICKP/LVDSP2	GPIO72	LD33*1			
MIPICKN/LVDSN2	GPIO73	LD34*1			
MIPIDP1/LVDSP1	GPIO74	LD35*1			
MIPIDN1/LVDSN1	GPIO75	LD36*1			
MIPIDP0/LVDSP0	GPIO76	LD37*1			
MIPIDN0/LVDSN0	GPIO77	LD38*1			LDCLK

Note *1: Those pins can be assigned from any LD1 to LD38.
Note *2: Those pins can be assigned from any VD0 to VD25.

Table 4-11. GPIO Pin Description

Pin Name	Type	Default reset)	Power	Description
GPIO0	I/O	HighZ	VDD_IOA	-
GPIO1	I/O	HighZ	VDD_IOA	-
GPIO2	I/O	HighZ	VDD_IOA	-
GPIO3	I/O	HighZ	VDD_IOA	
GPIO4	I/O	HighZ	VDD_IOA	-
GPIO5	I/O	HighZ	VDD_IOA	-
GPIO6	I/O	HighZ	VDD_IOA	-
GPIO7	I/O	HighZ	VDD_IOA	-
GPIO8	I/O	HighZ	VDD_IOA	-
GPIO9	I/O	HighZ	VDD_IOA	-
GPIO10	I/O	HighZ	VDD_IOA	-
GPIO11	I/O	HighZ	VDD_IOA	-
GPIO13	I/O	HighZ	VDD_IOA	-
GPIO14	I/O	HighZ	VDD_IOA	-
GPIO15	I/O	HighZ	VDD_IOA	-
GPIO16	I/O	HighZ	VDD_IOA	-
GPIO17	I/O	HighZ	VDD_IOA	-
GPIO18	I/O	HighZ	VDD_IOA	-
GPIO19	I/O	HighZ	VDD_IOA	-
GPIO20	I/O	HighZ	VDD_IOA	-
GPIO21	I/O	HighZ	VDD_IOA	-
GPIO22	I/O	HighZ	VDD_IOA	-
GPIO23	I/O	HighZ	VDD_IOA	-
GPIO24	I/O	HighZ	VDD_IOA	-
GPIO25	I/O	HighZ	VDD_IOA	-
GPIO26	I/O	HighZ	VDD_IOA	-
GPIO27	I/O	HighZ	VDD_IOB	-
GPIO28	I/O	HighZ	VDD_IOB	-
GPIO29	I/O	HighZ	VDD_IOB	-
GPIO30	I/O	HighZ	VDD_IOB	-
GPIO31	I/O	HighZ	VDD_IOB	-

Pin Name	Type	Default reset)	Power	Description
GPIO32	I/O	HighZ	VDD_IOB	
GPIO33	I/O	HighZ	VDD_IOB	
GPIO34	I/O	HighZ	VDD_IOB	
GPIO35	I/O	HighZ	VDD_IOB	
GPIO36	I/O	HighZ	VDD_IOB	-
GPIO37	I/O	HighZ	VDD_IOB	-
GPIO38	I/O	HighZ	VDD_IOC	-
GPIO40	I/O	HighZ	VDD_IOC	-
GPIO41	I/O	HighZ	VDD_IOC	-
GPIO42	I/O	HighZ	VDD_IOC	-
GPIO43	I/O	HighZ	VDD_IOC	-
GPIO44	I/O	HighZ	VDD_IOC	-
GPIO45	I/O	HighZ	VDD_IOC	-
GPIO46	I/O	HighZ	VDD_IOC	-
GPIO47	I/O	HighZ	VDD_IOC	-
GPIO48	I/O	HighZ	VDD_IOC	-
GPIO49	I/O	HighZ	VDD_IOC	-
GPIO50	I/O	HighZ	VDD_IOC	-
GPIO51	I/O	HighZ	VDD_IOC	-
GPIO53	I/O	HighZ	VDD_IOC	-
GPIO54	I/O	HighZ	VDD_IOC	-
GPIO55	I/O	HighZ	VDD_IOC	-
GPIO56	I/O	HighZ	VDD_IOC	-
GPIO57	I/O	HighZ	VDD_IOC	-
GPIO58	I/O	HighZ	VDD_IOC	-
GPIO59	I/O	HighZ	VDD_IOC	-
GPIO60	I/O	HighZ	VDD_IOC	-
GPIO61	I/O	HighZ	VDD_IOC	-
GPIO62	I/O	HighZ	VDD_IOC	-
GPIO63	I/O	HighZ	VDD_IOC	-
GPIO64	I/O	HighZ	VDD_IOC	HOST_CFG0
GPIO65	I/O	HighZ	VDD_IOC	HOST_CFG1
GPIO66	I/O	HighZ	VDD_IOC	BOOT_CFG0
GPIO67	I/O	HighZ	VDD_IOC	BOOT_CFG1
GPIO68	I/O	HighZ	VDD_IOC	
GPIO69	I/O	HighZ	VDD_IOC	
GPIO70	I/O	HighZ	VDD_IOC	
GPIO71	I/O	HighZ	VDD_IOC	
GPIO72	I/O	HighZ	VDD_IOC	
GPIO73	I/O	HighZ	VDD_IOC	
GPIO74	I/O	HighZ	VDD_IOC	
GPIO75	I/O	HighZ	VDD_IOC	
GPIO76	I/O	HighZ	VDD_IOC	
GPIO77	I/O	HighZ	VDD_IOC	

Notes: GPIO64~GPIP67 are for the hardware trap. There is pull-high/low resistance on I/O. It cannot drive the value on the external device when the system is resetting.

Table 4-12. SPI Host Interface when HOST_CFG == 01

Pin Name	Type	Default	Description
GPIO0	Input	HighZ	SPI Slave CLK
GPIO1	Input	HighZ	SPI Slave CS#
GPIO2	Input	HighZ	SPI Slave DIN
GPIO3	Output	0	SPI Slave DOUT

Table 4-13. IIC Host Interface when HOST_CFG == 10

Pin Name	Type	Default	Description
GPIO0	I/O	HighZ	IIC SCL
GPIO1	I/O	HighZ	IIC SDA

4.1.4 Hardware Trapping

Table 4-14. IT986x Hardware Trapping

Pin Name	Symbol	Description
GPIO66	BOOT_CFG0	Boot Configuration 00: booting from SD/MMC/EMMC 01: booting from NOR 10: booting from SPI NAND 11: co-operative mode
GPIO67	BOOT_CFG1	
GPIO63	ARM_CFG	ARM Configuration 0: Normal(Default)
GPIO64	HOST_CFG0	Host Configuration 00: select JTAG interface 01: select SPI interface 10: select IIC interface 11: uses as DGPIO[0-3]
GPIO65	HOST_CFG1	

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5. Function Description

5.1 Display Interface

The IT986x family supports 8/9/16/18 bits of CPU interface, 16/18/24 bits of RGB interface, and CCIR601 interface. The IT986x family supports both of LCD modules (LCM) with and without memory. The programmable interface timing is designed to fit most LCMs. Hereunder is the pin share mapping on each different mode.

Table 5-1. LCD Interface General Pin Mapping

Pin Name	RGB I/F	CPU I/F	CCIR 601/656
LVSYNC	VSYNC	XWR	VSYNC
LHSYNC	HSYNC	XRS	HSYNC
LDCLK	DCLK		DCLK
LDEN	DEN		DEN
LD0	D0	D0	D0
LD1	D1	D1	D1
LD2	D2	D2	D2
LD3	D3	D3	D3
LD4	D4	D4	D4
LD5	D5	D5	D5
LD6	D6	D6	D6
LD7	D7	D7	D7
LD8	D8	D8	
LD9	D9	D9	
LD10	D10	D10	
LD11	D11	D11	
LD12	D12	D12	
LD13	D13	D13	
LD14	D14	D14	
LD15	D15	D15	
LD16	D16	D16	
LD17	D17	D17	
LD18	D18		
LD19	D19		
LD20	D20		
LD21	D21		
LD22	D22 / CTG4		CTG4
LD23	D23 / CTG5		CTG5
LCSN	CS0 / CTG7	CS0	CS0 / CTG7
LSA0	A0 / CTG6		A0 / CTG6
LSDA	SDA		SDA
LSCK	SCK / CTG3		SCK / CTG3

Table 5-2. LCD with RGB Interface Pin Mapping for RGB565 and RGB666

Color Mode	RGB565	RGB666					
Panel Interface	16-bit	6-bit			9-bit		18-bit
Timing Sequence	t/pixel	t1/pixel	t2/pixel	t3/pixel	t1/pixel	t2/pixel	t/pixel
LD0	B0	R0	G0	B0	G3	B0	B0
LD1	B1	R1	G1	B1	G4	B1	B1

Color Mode	RGB565	RGB666					
Panel Interface	16-bit	6-bit			9-bit		18-bit
Timing Sequence	t/pixel	t1/pixel	t2/pixel	t3/pixel	t1/pixel	t2/pixel	t/pixel
LD2	B2	R2	G2	B2	G5	B2	B2
LD3	B3	R3	G3	B3	R0	B3	B3
LD4	B4	R4	G4	B4	R1	B4	B4
LD5	G0	R5	G5	B5	R2	B5	B5
LD6	G1				R3	G0	G0
LD7	G2				R4	G1	G1
LD8	G3				R5	G2	G2
LD9	G4						G3
LD10	G5						G4
LD11	R0						G5
LD12	R1						R0
LD13	R2						R1
LD14	R3						R2
LD15	R4						R3
LD16							R4
LD17							R5

Table 5-3. LCD with RGB Interface Pin Mapping for RGB888

Color Mode	RGB888								
Panel Interface	9-bit/mode 1			9-bit/mode 2			18-bit		24-bit
Timing Sequence	t1/pixel	t2/pixel	t3/pixel	t1/pixel	t2/pixel	t3/pixel	t1/pixel	t2/pixel	t/pixel
LD0	R0	G0	B0	GND	GND	GND	R0	B0	B0
LD1	R1	G1	B1	R0	G0	B0	R1	B1	B1
LD2	R2	G2	B2	R1	G1	B1	R2	B2	B2
LD3	R3	G3	B3	R2	G2	B2	R3	B3	B3
LD4	R4	G4	B4	R3	G3	B3	R4	B4	B4
LD5	R5	G5	B5	R4	G4	B4	R5	B5	B5
LD6	R6	G6	B6	R5	G5	B5	R6	B6	B6
LD7	R7	G7	B7	R6	G6	B6	R7	B7	B7
LD8	GND	GND	GND	R7	G7	B7	GND	G0	G0
LD9							GND	G1	G1
LD10							GND	G2	G2
LD11							GND	G3	G3
LD12							GND	G4	G4
LD13							GND	G5	G5
LD14							GND	G6	G6
LD15							GND	G7	G7
LD16							GND	GND	R0
LD17							GND	GND	R1
LD18									R2
LD19									R3
LD20									R4
LD21									R5
LD22									R6
LD23									R7

Table 5-4. LCD Pin Share with GPIO Table (TBD)

5.1.1 General Description

- 80-type CPU interface
- 68-type CPU interface
- RGB with serial interface
- RGB with direct control interface
- CCIR601/CCIR656 output interface

5.1.2 80-Type CPU Interface

The figure below illustrates the implementation for interfacing the IT986x family to an 80-type CPU interface LCM. IT986x family can support dual display for this interface.

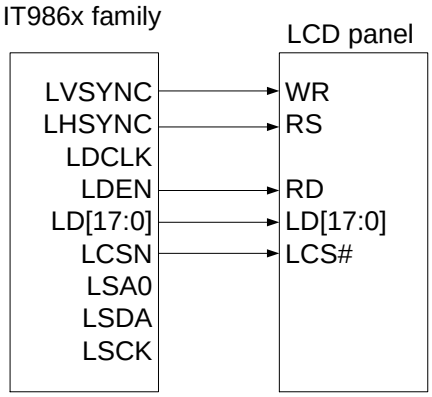


Figure 5-1. Connection of IT986x Family to 80-Type CPU Interface LCM

The timing for 80-type CPU interface is shown in the following figure. There is an internal clock DHCLK. By adjusting the timing parameters T_1 ~ T_8, which are relative to DHCLK, it can satisfy the timing requirement of LCD panels.

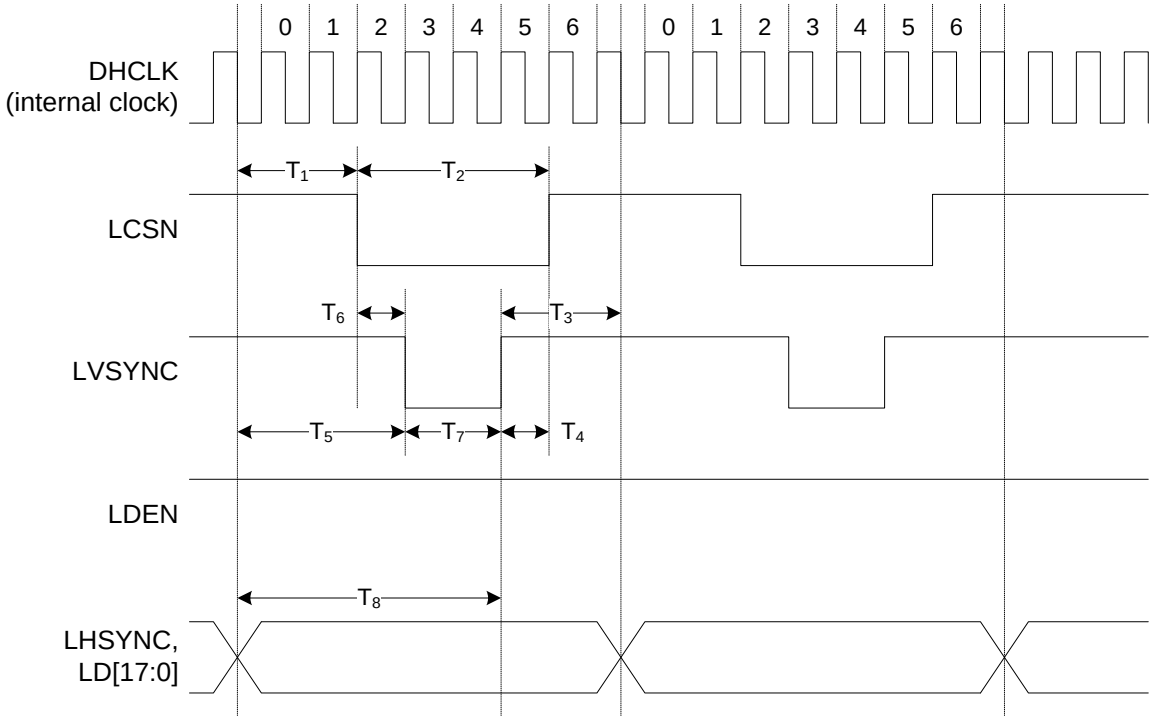


Figure 5-2. 80-Type CPU Interface Timing

5.1.3 68-Type CPU Interface

The figure below illustrates the implementation for interfacing the IT986x family to the LCM with a 68-type CPU interface. IT986x family can support dual displays for this interface.

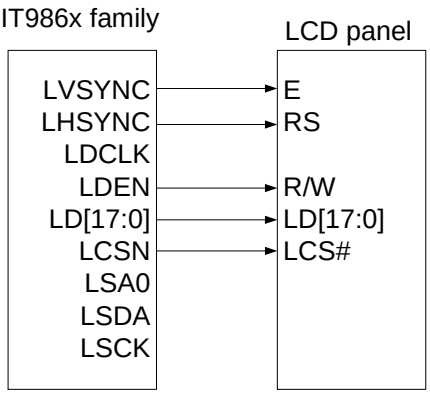


Figure 5-3. Connection of IT986x Family to 68-Type CPU Interface LCM

The timing for 68-type CPU interface is shown in the following figure. There is an internal clock DHCLK. By adjusting the timing parameters T_1 ~ T_8, which are relative to DHCLK, it can satisfy the timing requirement of LCD panels.

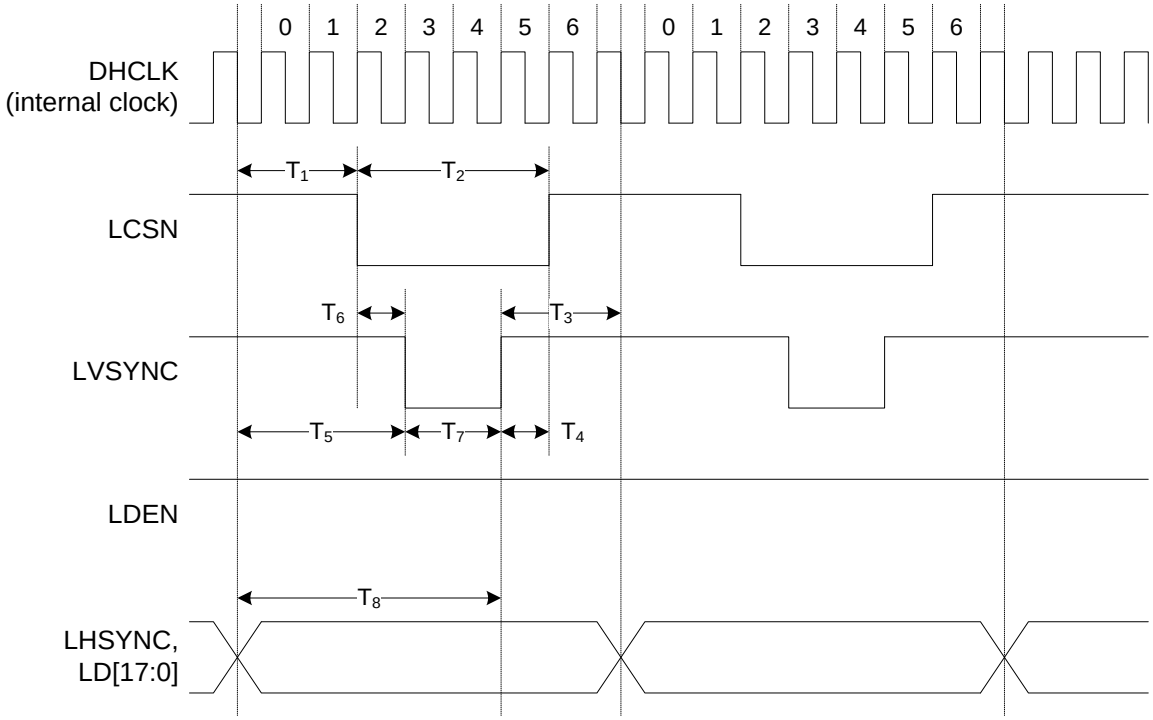


Figure 5-4. 68-Type CPU Interface Timing

5.1.4 RGB with Serial Interface

The figure below illustrates the implementation for interfacing the IT986x family to an RGB with serial interface LCM. IT986x family only supports one display for this interface.

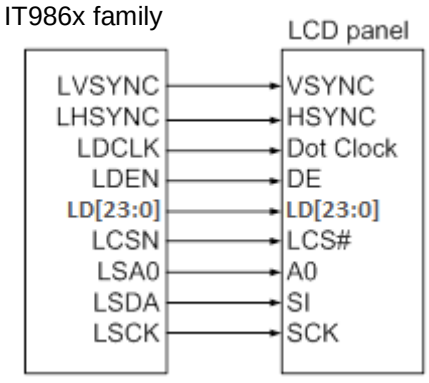


Figure 5-5. Connection of IT986x Family to RGB with Serial Interface LCM

IT986x family supports 8/9/16 bits of serial interface to send the LCM command and uses 6/9/16/18/24 bits of parallel RGB interface to send the display data. The timing for RGB with serial interface is shown in the following figure.

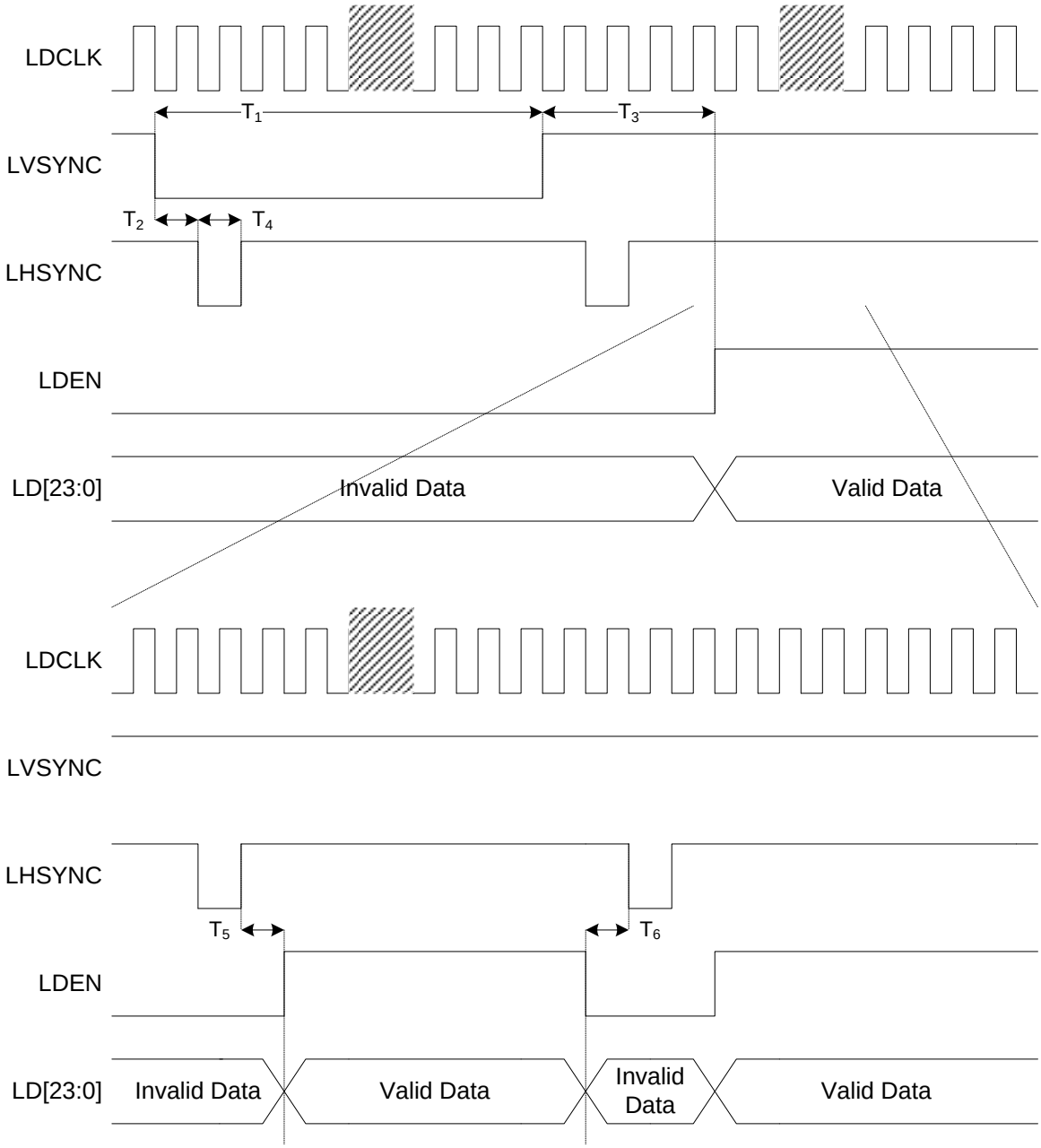


Figure 5-6. RGB Timing (for data)

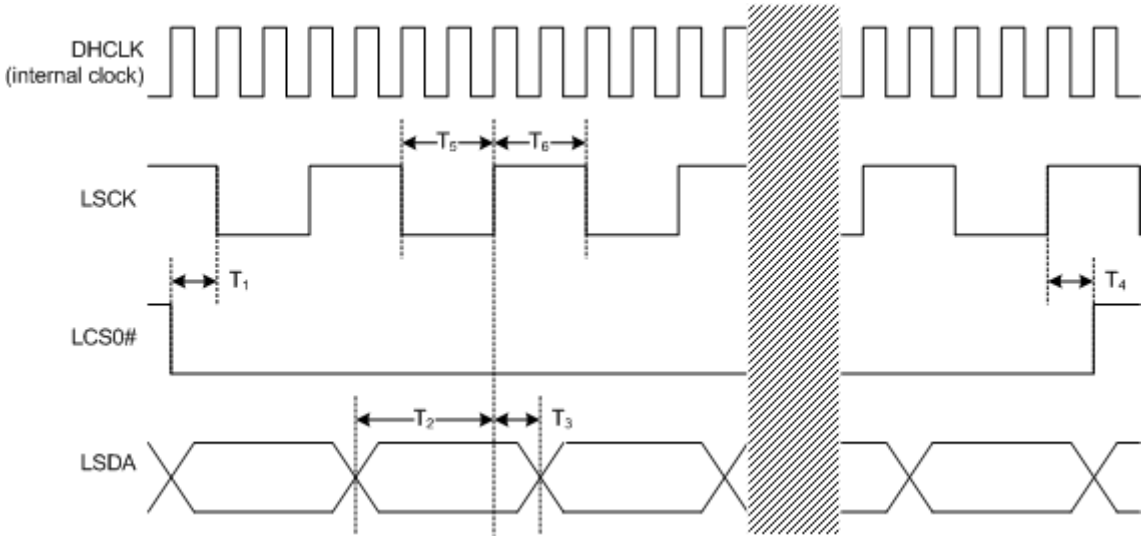


Figure 5-7. RGB Timing (for command)

5.1.5 RGB with Direct Control Interface

The figure below illustrates the implementation for interfacing the IT986x family to a RGB with direct control interface LCM. IT986x family only supports one display with this interface

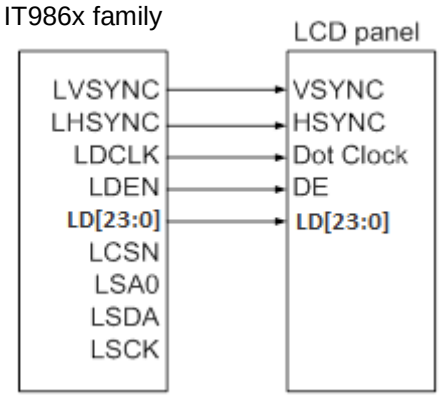


Figure 5-8. Connection of IT986x Family to RGB with Direct Control Interface LCM

Some LCMs do not have any serial interface, but only have parallel RGB interface. In this case, the unused pins LCSN can be defined as GPIO. See Table 5-4 for detail. The timing for RGB parallel interface is shown in the following figure.

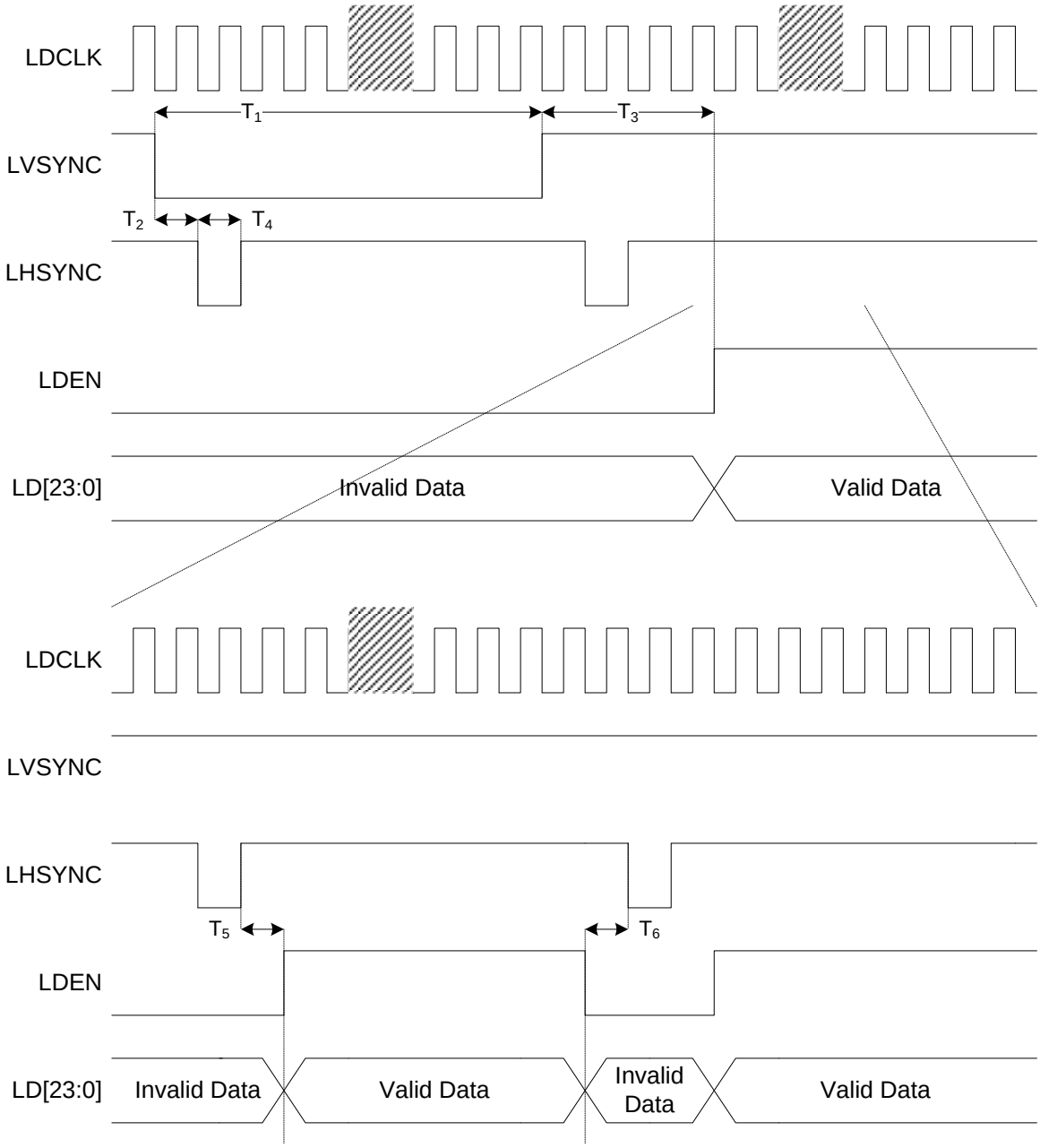


Figure 5-9. RGB with Direct Control Interface Timing (for data)

5.1.6 CCIR601/656 Output Interface

IT986x family supports CCIR601/656 output interface. It can be connected to any device which has CCIR601/656 input interface. The figure below illustrates the implementation. The CCIR601/656 output video resolution and timing are programmable. It can be set to meet the system requirement. The general output resolutions are 800x480, 640x480, 480x272, 320x240 and 240x320.

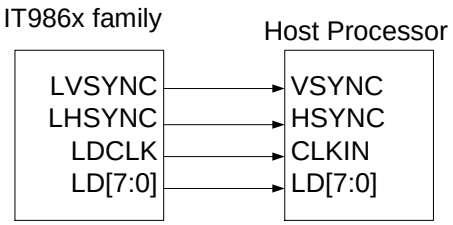


Figure 5-10. Connection of IT986x Family to Host Processor with CCIR601 Interface

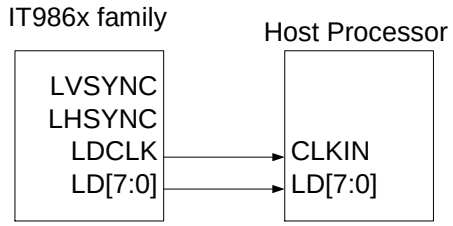


Figure 5-11. Connection of IT986x Family to Host Processor with CCIR656 Interface

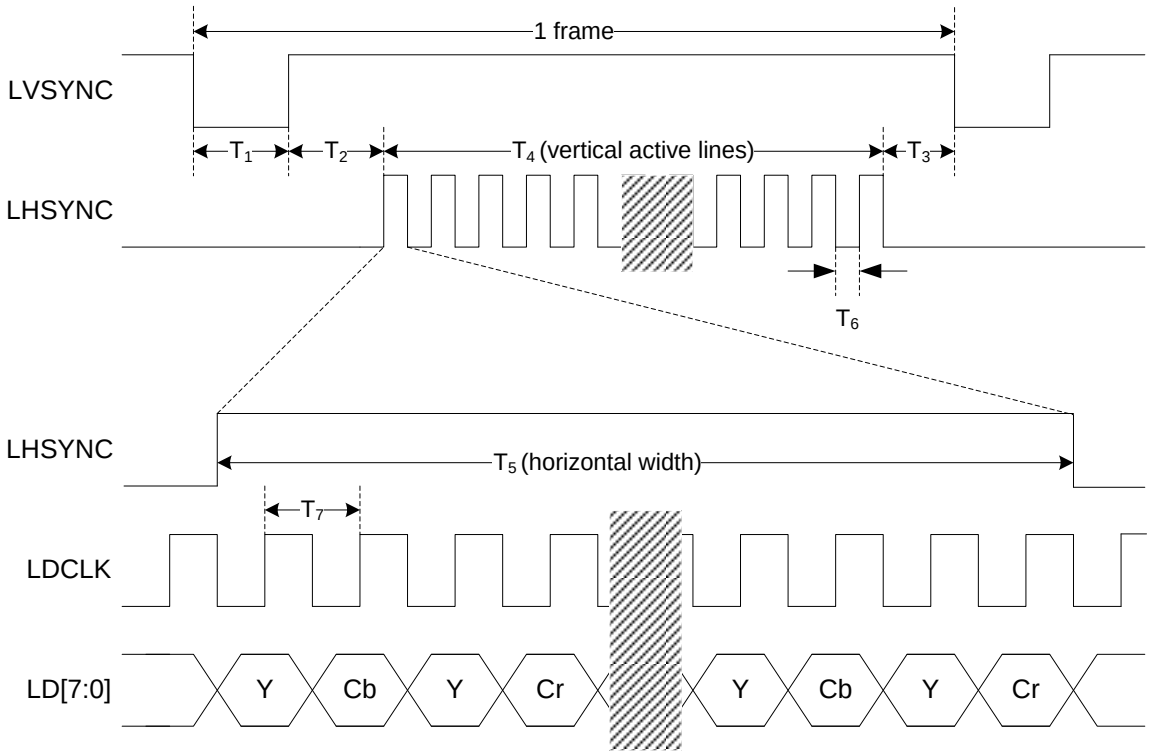


Figure 5-12. CCIR601 Output Interface Timing

Table 5-5. CCIR601 Output Interface Timing Table

Symbol	Parameter	30 Frame/sec.	25 Frame/sec.	Unit
800x480 progressive video				
T_1	Vertical sync pulse width	8	8	line
T_2	Vertical back porch	6	6	line
T_3	Vertical front porch	6	6	line
T_4	Vertical active lines	480	480	line

Symbol	Parameter	30 Frame/sec.	25 Frame/sec.	Unit
T_5	Horizontal width of one active line	1600	1600	T (1)
T_6	Horizontal sync pulse width	200	560	T
T_7	Clock period	37 (2)	37	ns
640x480 progressive video				
T_1	Vertical sync pulse width	8	8	line
T_2	Vertical back porch	6	6	line
T_3	Vertical front porch	6	6	line
T_4	Vertical active lines	480	480	line
T_5	Horizontal width of one active line	1280	1280	T
T_6	Horizontal sync pulse width	520	880	T
T_7	Clock period	37	37	ns
480x272 progressive video				
T_1	Vertical sync pulse width	8	8	line
T_2	Vertical back porch	10	10	line
T_3	Vertical front porch	10	10	line
T_4	Vertical active lines	272	272	line
T_5	Horizontal width of one active line	960	960	T
T_6	Horizontal sync pulse width	40	240	T
T_7	Clock period	111(3)	111	ns
320x240 progressive video				
T_1	Vertical sync pulse width	20	20	line
T_2	Vertical back porch	20	20	line
T_3	Vertical front porch	20	20	line
T_4	Vertical active lines	240	240	line
T_5	Horizontal width of one active line	640	640	T
T_6	Horizontal sync pulse width	110	260	T
T_7	Clock period	148 (4)	148	ns
240x320 progressive video				
T_1	Vertical sync pulse width	15	15	line
T_2	Vertical back porch	20	20	line
T_3	Vertical front porch	20	20	line
T_4	Vertical active lines	320	320	line
T_5	Horizontal width of one active line	480	480	T
T_6	Horizontal sync pulse width	120	240	T
T_7	Clock period	148	148	ns

Notes:

1. T represents the clock period.
2. The clock frequency is 27.0 MHz.
3. The clock frequency is 9.0 MHz.
4. The clock frequency is 6.75 MHz.

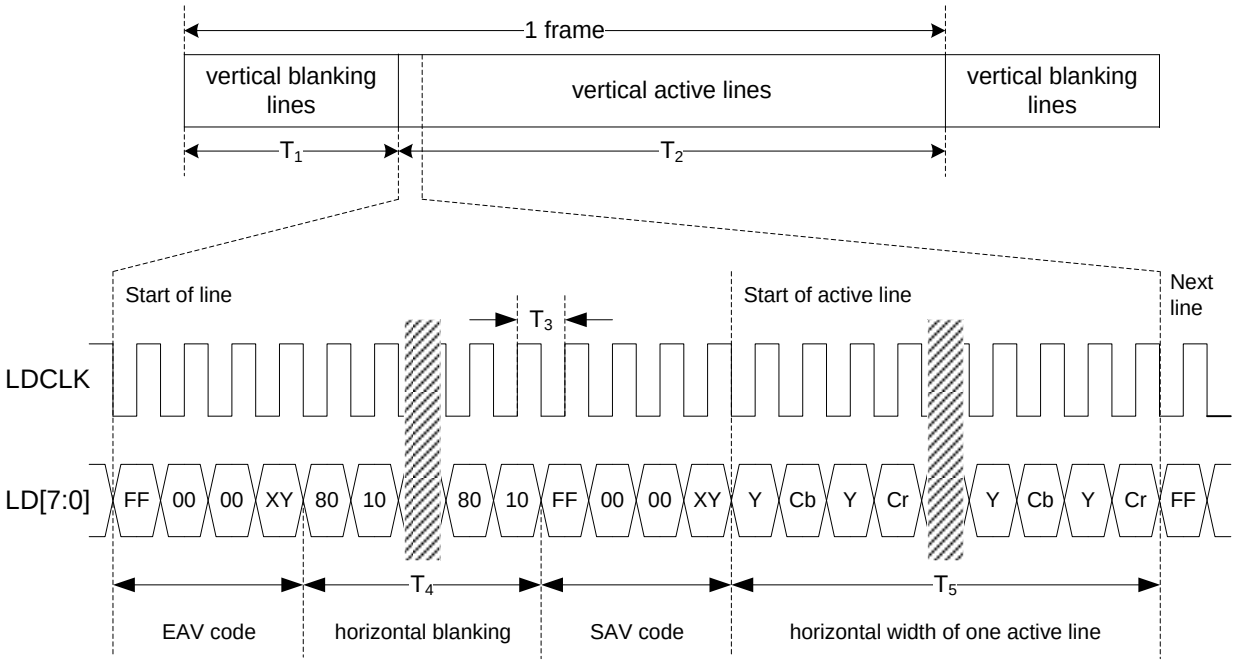


Figure 5-13. CCIR656 Output Interface Timing

The SAV (start of active video) code and EAV (end of active video) code are embedded within the video data stream. They replace the vertical sync and horizontal sync signals. The definitions of SAV and EAV codes are shown in the following table.

Table 5-6. SAV Code and EAV Code

Bit Number	The 1st word	The 2nd word	The 3rd word	The 4th word
7 (MSB)	1	0	0	1
6	1	0	0	F(1)
5	1	0	0	V(2)
4	1	0	0	H(3)
3	1	0	0	P3(4)
2	1	0	0	P2
1	1	0	0	P1
0	1	0	0	P0

Notes:

1. When interleaved video: F = 0 for field 1 and F = 1 for field 2. When progressive video: F = 0.

2. V = 1 during vertical blanking, and V = 0 elsewhere.
3. H = 0 in SAV, H = 1 in EAV.
4. P3 ~ P0 are protection bits. Where P3 = V xor H, P2 = F xor H, P1 = F xor V, P0 = F xor V xor H.

Table 5-7. CCIR656 Output Interface Timing Table

Symbol	Parameter	30 frame/sec.	25 frame/sec.	Unit
800x480 progressive video				
T_1	Vertical blanking lines	20	20	line
T_2	Vertical active lines	480	480	line
T_3	Clock period	37 (2)	37	ns
T_4	Horizontal blanking	192	552	T (1)
T_5	Horizontal width of one active line	1600	1600	T
640x480 progressive video				
T_1	Vertical blanking lines	20	20	line
T_2	Vertical active lines	480	480	line
T_3	Clock period	37	37	ns
T_4	Horizontal blanking	512	872	T
T_5	Horizontal width of one active line	1280	1280	T
480x272 progressive video				
T_1	Vertical blanking lines	28	28	line
T_2	Vertical active lines	272	272	line
T_3	Clock period	111(3)	111	ns
T_4	Horizontal blanking	32	232	T
T_5	Horizontal width of one active line	960	960	T
320x240 progressive video				
T_1	Vertical blanking lines	60	60	line
T_2	Vertical active lines	240	240	line
T_3	Clock period	148 (4)	148	ns
T_4	Horizontal blanking	102	252	T
T_5	Horizontal width of one active line	640	640	T
240x320 progressive video				
T_1	Vertical blanking lines	55	55	line
T_2	Vertical active lines	320	320	line
T_3	Clock period	148	148	ns
T_4	Horizontal blanking	112	232	T
T_5	Horizontal width of one active line	480	480	T

Notes:

1. T represents the clock period.
2. The clock frequency is 27.0 MHz.
3. The clock frequency is 9.0 MHz.
4. The clock frequency is 6.75 MHz.

5.1.7 MIPI Output Interface

IT986x family supports MIPI output interface. The Figure 5-14 illustrates the implementation for interfacing with MIPI Panel. The Line Levels in HS and LP Modes shown in the Figure 5-15. Figure 5-16 shows the sequence of events during the transmission of a Data Burst.

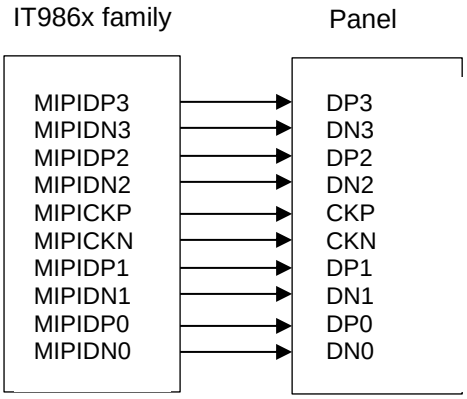


Figure 5-14. Connection of IT986x Family to MIPI Panel

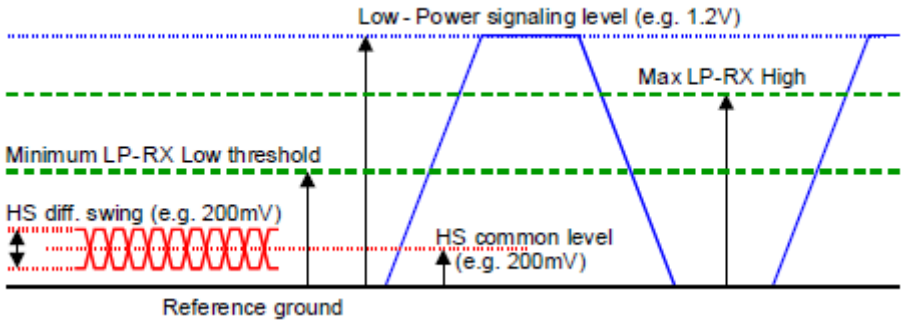


Figure 5-15. Line Levels in HS and LP Modes

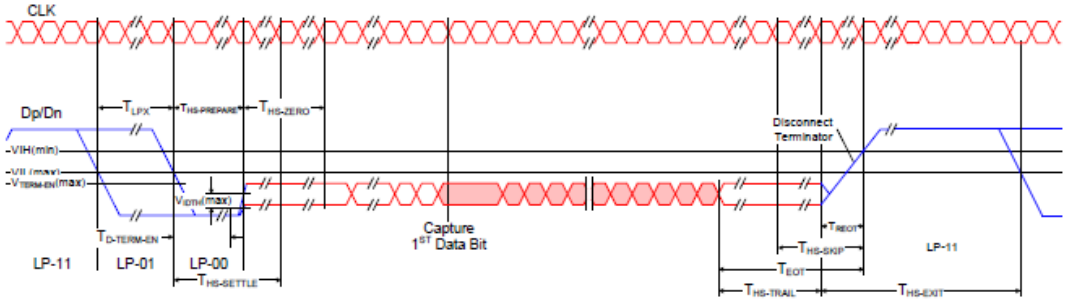


Figure 5-16. High-Speed Data Transmission in Bursts

5.1.8 LVDS Interface

IT986x family supports LVDS interface, compliant with the JEIDA-24 and VESA-18, VESA-24 specifications.

5.1.8.1 JEIDA 24-bits

The Figure 5-17 illustrates the implementation for interfacing with JEIDA 24-bits LVDS panel. Figure 5-18 shows the Interface Timing diagram.

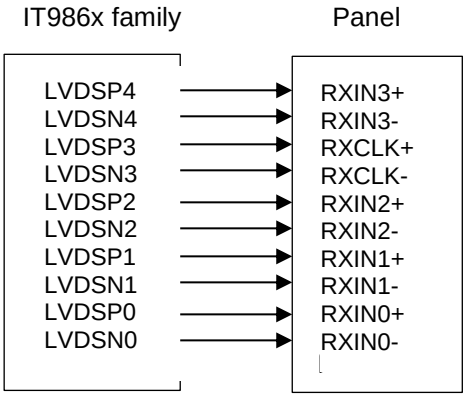


Figure 5-17. Connection of IT986x Family to JEIDA 24-bits LVDS panel

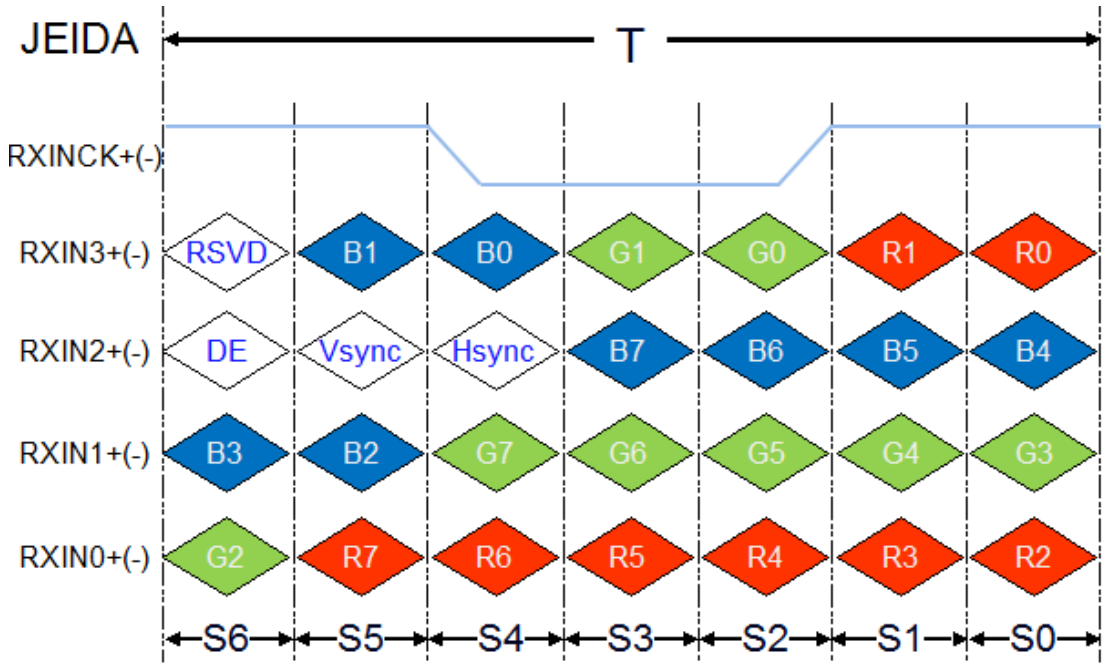


Figure 5-18. JEIDA 24-bits Interface Timing

5.1.8.2 VESA 18-bits

The Figure 5-19 illustrates the implementation for interfacing with VESA 18-bits LVDS panel. Figure 5-20 shows the Interface Timing diagram.

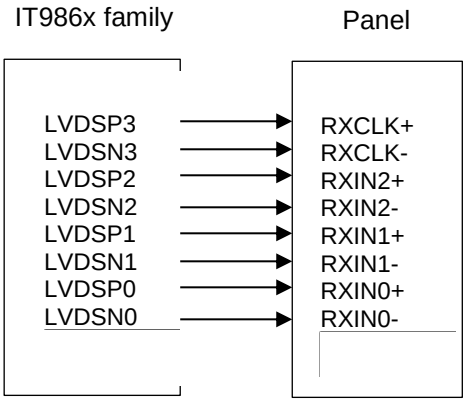


Figure 5-19. Connection of IT986x Family to VESA 18-bits LVDS panel

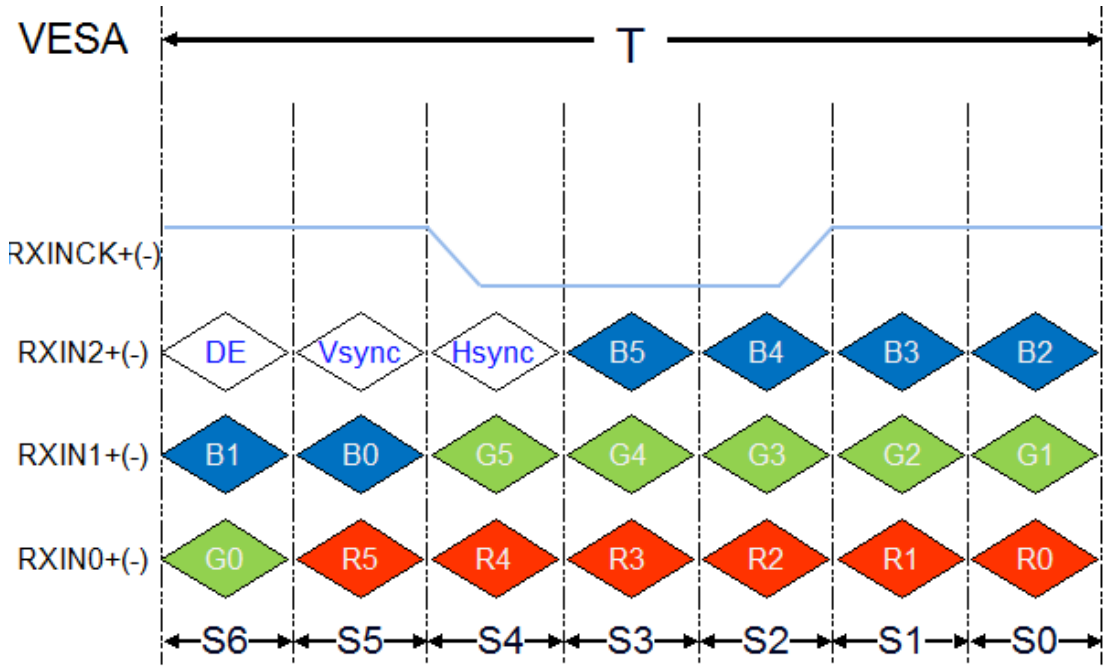


Figure 5-20. VESA 18-bits Interface Timing

5.1.8.3 VESA 24-bits

The Figure 5-21 illustrates the implementation for interfacing with VESA 24-bits LVDS panel. Figure 5-22 shows the Interface Timing diagram.

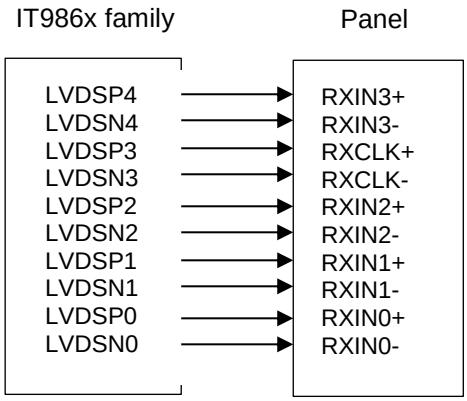


Figure 5-21. Connection of IT986x Family to VESA 24-bits LVDS panel

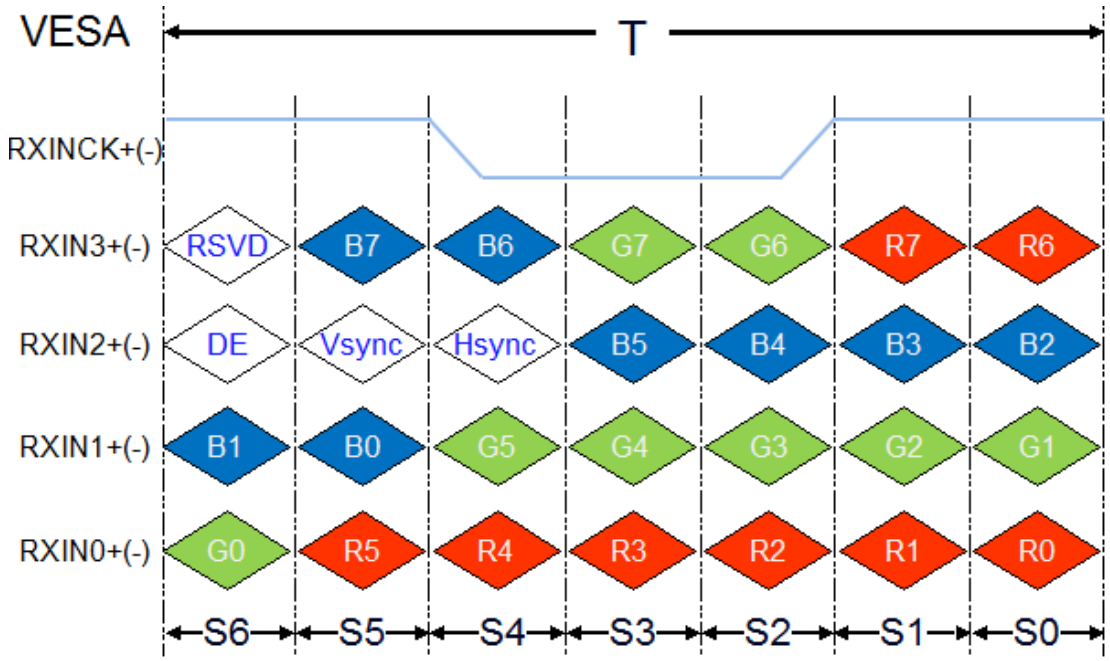


Figure 5-22. VESA 24-bits Interface Timing

5.2 Host/Peripheral USB 2.0 Interface

This is a universal serial bus (USB) 2.0 On-The-Go (OTG) controller, which can play a dual role, either as a host or as a peripheral controller. There are one USB controller. Host/Peripheral selectable. It controls with USB_ID pin which it can be selected by any GPIO pins. When it acts as a host, it contains a USB host controller that supports all-speed transactions. Without the software intervention, the host controller can deal with a transaction-based data structure to offload the CPU and automatically transmit and receive data on the USB bus. When it acts as a peripheral controller, each endpoint, except endpoint 0, accepts programmable HS/FS transfer types to provide flexibility to suit all applications. In addition, complying with OTG standards means both the Session Request Protocol (SRP) and Host Negotiation Protocol (HNP) are supported. The system bus can be a PVCI or AHB 32-bit bus interface. The transceiver interface is UTMI+ level 3, which supports the HS/FS/LS transfers and a HS/FS hub.

Table 5-8. Dynamic Characteristics of DP/DM

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
USB 2.0 transceiver (HS)						
Input levels (Differential receiver)						
V_{HSDIFF}	High-speed differential input sensitivity	$\|V_{I(DP)} - V_{I(DM)}\|$ Measured at the connection as an application circuit	300	-	-	mV
V_{HSCM}	Voltage range of high-speed data signaling in the common mode	-	-50	-	500	mV
V_{HSSQ}	High-speed squelch detection threshold	Squelch is detected.	-	-	100	mV
		Squelch is not detected.	150	-	-	mV
V_{HSDSC}	High-speed disconnection detection threshold	Disconnection is detected.	625	-	-	mV
		Disconnection is not detected.	-	-	525	mV

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
Output levels						
V_{HSOI}	High-speed idle-level output voltage (Differential)	-	-10	-	10	mV
V_{HSOL}	High-speed low-level output voltage (Differential)	-	-10	-	10	mV
V_{HSOH}	High-speed high-level output voltage (Differential)	-	-360	-	400	mV
V_{CHIRPJ}	Chirp-J output voltage (Differential)	-	700	-	1100	mV
V_{CHIRPK}	Chirp-K output voltage (Differential)	-	-900	-	-500	mV
Resistance						
R_{DRV}	Driver output impedance	Equivalent resistance used as the internal chip	40.5	45	49.5	Ω
Termination						
V_{TERM}	Termination voltage of the pull-up resistor on the RPU pin.	-	3.0	-	3.6	V
USB 1.1 transceiver (FS/LS)						
Input levels (Differential receiver)						
V_{DI}	Differential input voltage sensitivity	$\|V_{I(DP)} - V_{I(DM)}\|$	0.2	-	-	V
V_{CM}	Differential common-mode voltage	-	0.8	-	2.5	V
Input levels (single-ended receivers)						
V_{SE}	Single-ended receiver threshold	-	0.8	-	2.0	V
Output levels						
V_{OL}	Low-level output voltage	-	0	-	0.3	V
V_{HL}	High-level output voltage	-	2.8	-	3.6	V

Table 5-9. Static Characteristics of DP/DM

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
Driver characteristics						
High-speed mode						
t_{HSR}	High-speed differential rise time	-	500	-	-	ps
t_{HSF}	High-speed differential fall time	-	500	-	-	ps
Full-speed mode						
t_{FR}	Rise time of DP/DM	C_L = 50 pF; 10% ~ 90% of $\|V_{OH} - V_{OL}\|$	4	-	20	ns
t_{FF}	Fall time of DP/DM	C_L = 50 pF; 90% ~ 10% of $\|V_{OH} - V_{OL}\|$	4	-	20	ns
t_{FRMA}	Differential rise/fall time matching (t_{FR} / t_{FF})	Excluding the first transition from the idle mode	90	-	110	%

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
V_{CRS}	Output signal crossover voltage	Excluding the first transition from the idle mode	1.3	-	2.0	V
Low-speed mode						
t_{LR}	Rise time of DP/DM	CL = 200 pF ~ 600 pF; 10% ~ 90% of $\|V_{OH} - V_{OL}\|$	75	-	300	ns
t_{LF}	Fall time of DP/DM	CL = 200 pF ~ 600 pF; 90% ~ 10% of $\|V_{OH} - V_{OL}\|$	75	-	300	ns
t_{LRMA}	Differential rise/fall time matching (t_{LR}/t_{LF})	Excluding the first transition from the idle mode	80	-	125	%
V_{CRS}	Output signal crossover voltage	Excluding the first transition from the idle mode	1.3	-	2.0	V
Driver timing						
High-speed mode						
	Driver waveform requirement	Please refer to the eye pattern of template 1 described in USB specification, Rev. 2.0.	Follow template 1			
Full-speed mode						
	Propagation delay (VI, FSE 0, OE to DP, DN)	For the detailed description of VI, FSE 0, and OE, please refer to the USB specification, Rev. 1.1.	-	-	15	ns
Low-speed mode						
Not specified: The low-speed delay time is dominated by the slow t_{LR} and t_{LF}.						
Receiver timing						
High-speed mode (Template 4, USB 2.0 spec.)						
	Data source jitter and receiver jitter tolerance	Please refer to the eye pattern of template 4 described in the USB rev 2.0 specification.	Follow template 4			
Full-speed mode						
$t_{PLH(rcv)}$ $t_{PHL(rcv)}$	Receiver propagation delay (DP; DM to RCV)	For the detailed description of RCV, please refer to the USB 1.1 specification.	-	-	15	ns
$t_{PLH(single)}$ $t_{PHL(single)}$	Receiver propagation delay (DP; DM to VOP, VON)	-	-	-	15	ns

5.3 MMC/SD Interface

5.3.1 General Description

The IT986x family supports the MMC/SD card for users to store the audio files, JPEG image and MPEG-4

movies. It is convenient for users to put these data to the computer or download data from the computer. The IT986x family is fully compliant with MMCA v4.3, and 8-bit data of MMCA v4.3.

5.3.2 MMC/SD Interface Timing Diagram

The MMC/SD Interface Timing diagram is shown in Figure 5-23. The detailed timing description is shown in Table 5-10.

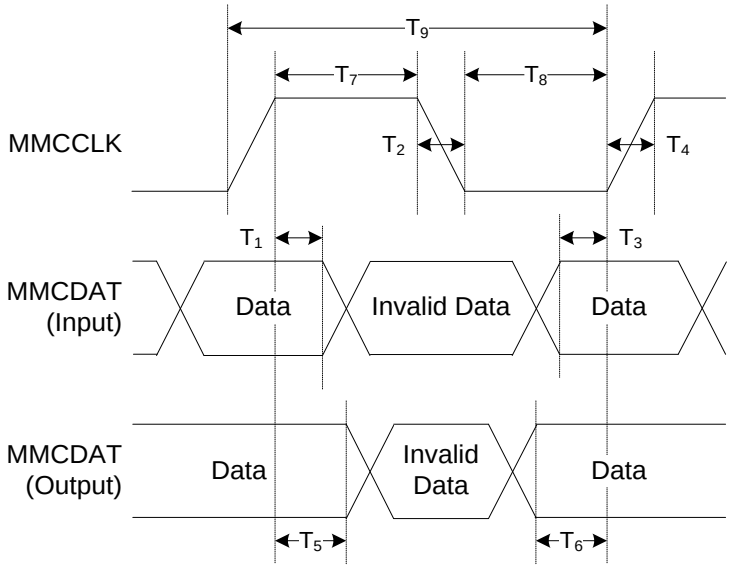


Figure 5-23. MMC/SD Interface Timing Diagram

Table 5-10. MMC/SD Interface Timing Table

Symbol	Parameter	Min.	Max.	Units
T1	Input Hold Time	5	-	ns
T2	Clock fall time	-	10	ns
T3	Input Setup Time	5	-	ns
T4	Clock Rise Time	-	10	ns
T5	Output Hold Time	3	-	ns
T6	Output Setup Time	3	-	ns
T7	Clock High Time	10	-	ns
T8	Clock Low Time	10	-	ns
T9	Clock Cycle Time	40	-	ns

5.3.3 Multi SD Device Connection

5.3.3.1 Two SD card

Pin Name	SD0 Device	SD1 Device
GPIO13	SD0_CMD	SD1_CMD
GPIO15	SD0_D0	SD1_D0
GPIO16	SD0_D1	SD1_D1
GPIO17	SD0_D2	SD1_D2
GPIO18	SD0_D3	SD1_D3
GPIO14	SD0_CLK	

Pin Name	SD0 Device	SD1 Device
GPIO11	-	SD1_CLK

5.3.3.2 SD card + SDIO

Pin Name	SD Device	SDIO Device
GPIO13	SD0_CMD	-
GPIO15	SD0_D0	-
GPIO16	SD0_D1	-
GPIO17	SD0_D2	-
GPIO18	SD0_D3	-
GPIO14	SD0_CLK	-
GPIO43	-	SD1_CMD
GPIO42	-	SD1_CLK
GPIO44	-	SD1_D0
GPIO45	-	SD1_D1
GPIO46	-	SD1_D2
GPIO47	-	SD1_D3

5.4 SPI Interface

Table 5-11. NOR Interface AC Timing

Symbol	Alt	Parameter	Min.	Typ.	Max.	Units
F_{clk}		Serial Clock Frequency	D.C.		80	MHz
t_{CH}		Serial Clock High Time	5.6			ns
t_{CL}		Serial Clock Low Time	5.6			ns
t_{CLCH}		Serial Clock Rise Time (Slew Rate)	0.1			V/ns
t_{CHCL}		Serial Clock Fall Time (Slew Rate)	0.1			V/ns
t_{SLCH}	t_{CSS}	CS# Active Setup Time	3			ns
t_{CHSH}		CS# Active Hold Time	3			ns
t_{SHSL}	t_{CSH}	CS# High Time	50			ns
t_{CLQX}	t_{HO}	Output Hold Time	1			ns
t_{DVCH}	t_{DSU}	Data In Setup Time	2			ns
t_{CHDX}	t_{DH}	Data In Hold Time	2			ns
t_{CLQV}		t_V Output Valid from SCK			6	ns

Notes: $t_{CLH} + t_{CLL}$ must greater than $1 / F_{CLK}$

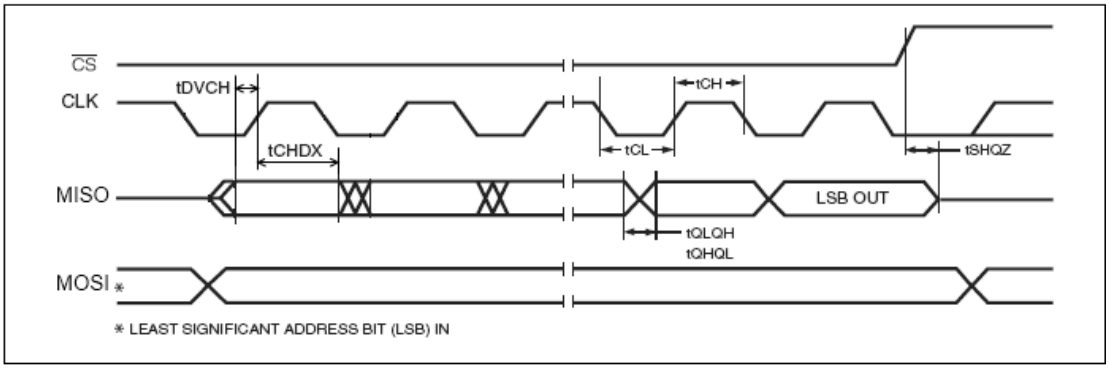


Figure 5-24. Serial Input Timing

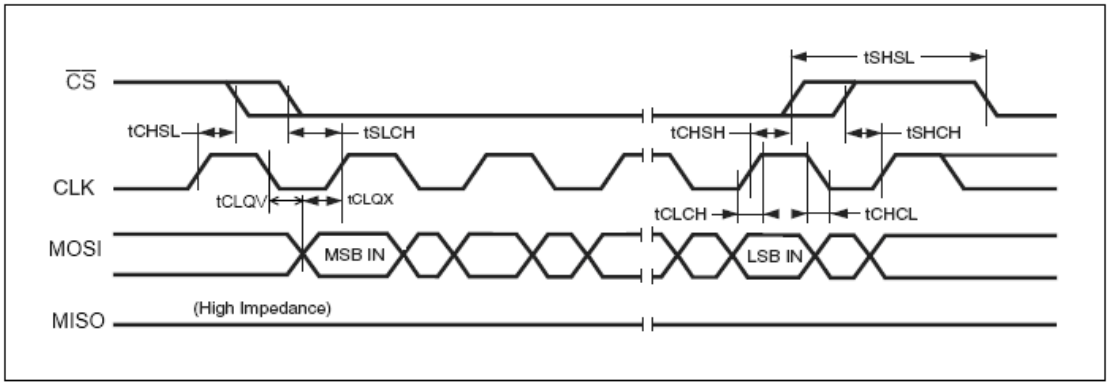


Figure 5-25. Serial Output Timing

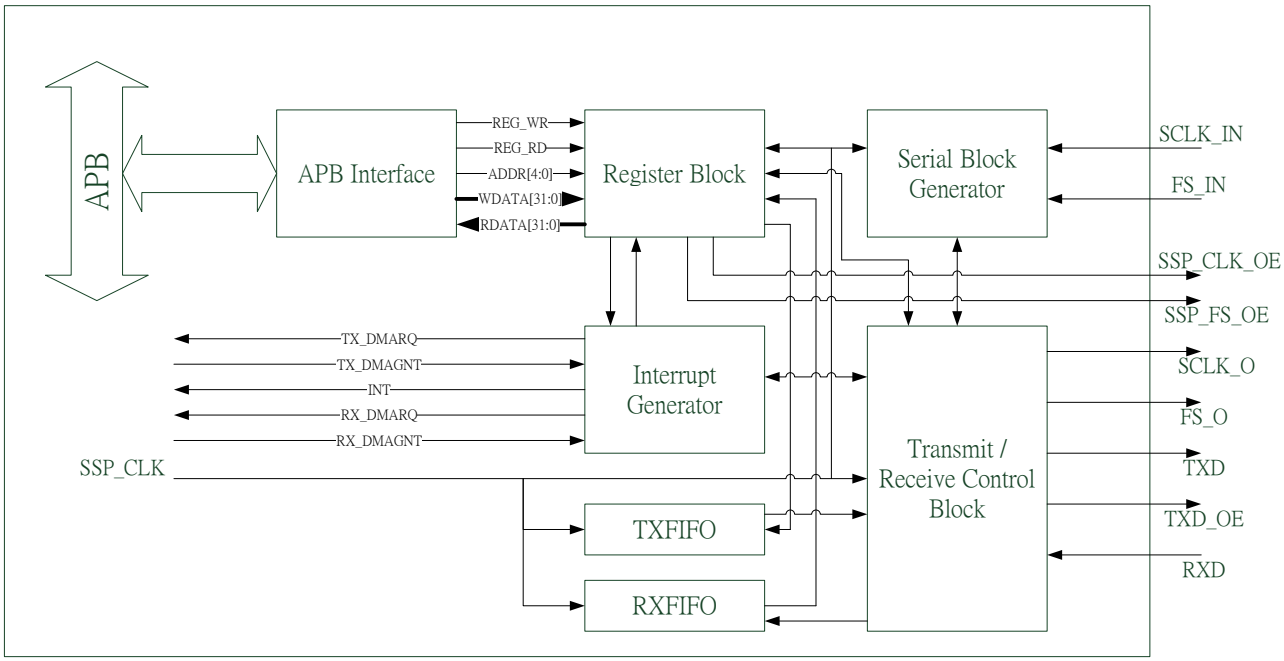
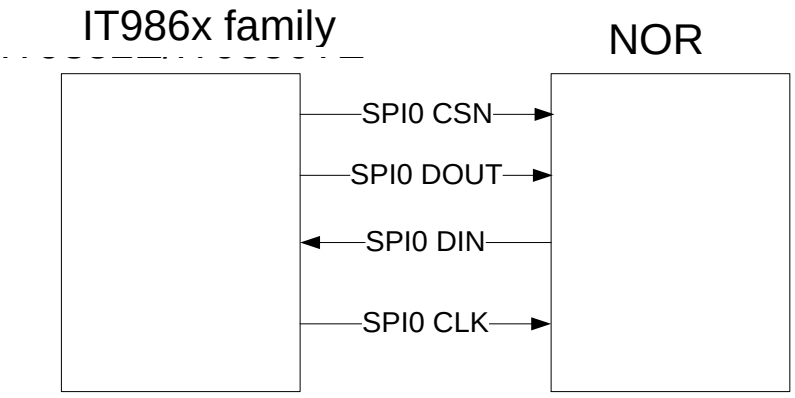


Figure 5-26. Block Diagram of NOR Interface

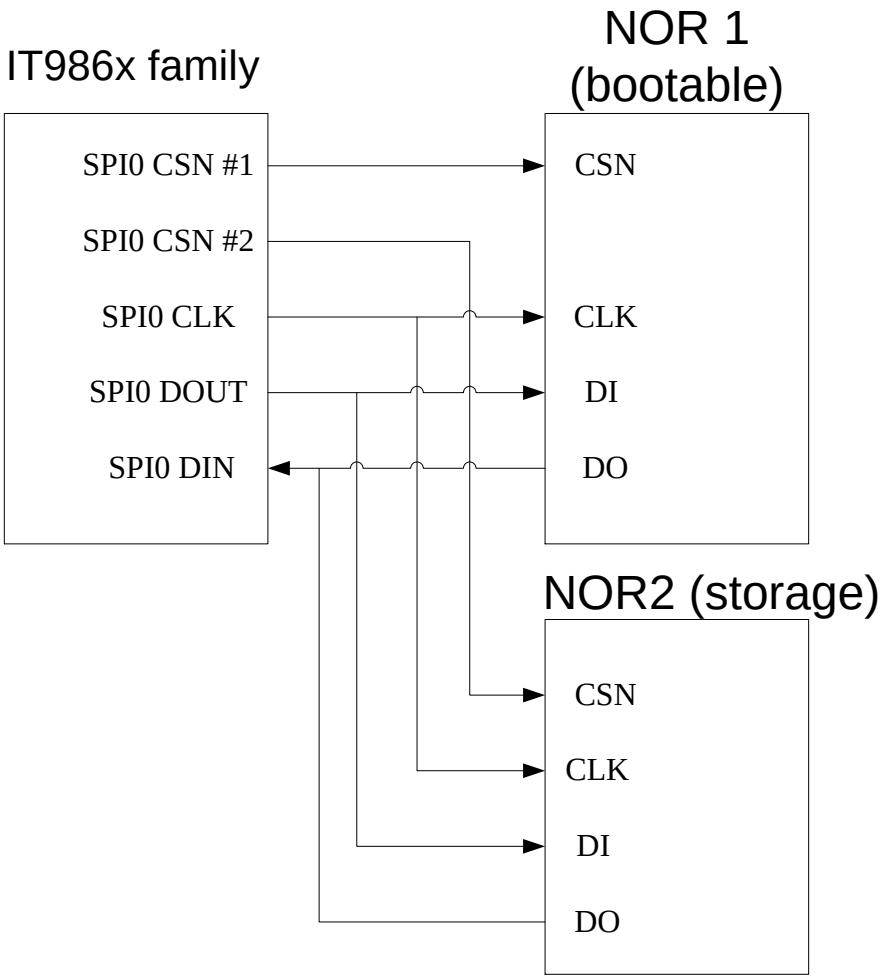
Table 5-12. Pin Share for AXISPI Interface

Pin Name	Mode 0	Mode 1
GPIO10	GPIO10	AXISPI_CLK
GPIO5	GPIO5	AXISPI_CS0
GPIO6	GPIO6	AXISPI_D0
GPIO7	GPIO7	AXISPI_D1
GPIO8	GPIO8	AXISPI_D2
GPIO9	GPIO9	AXISPI_D3

For the NOR booting, it only can connect GPIO5, GPIO6, GPIO7, GPIO8, GPIO9 and GPIO10 to the NOR device. The other pins are for the storage devices and without booting capability.



Hereunder is multi-chips connection to support two NORs. NOR1 is for the boot device while NOR2 is for the storage device.



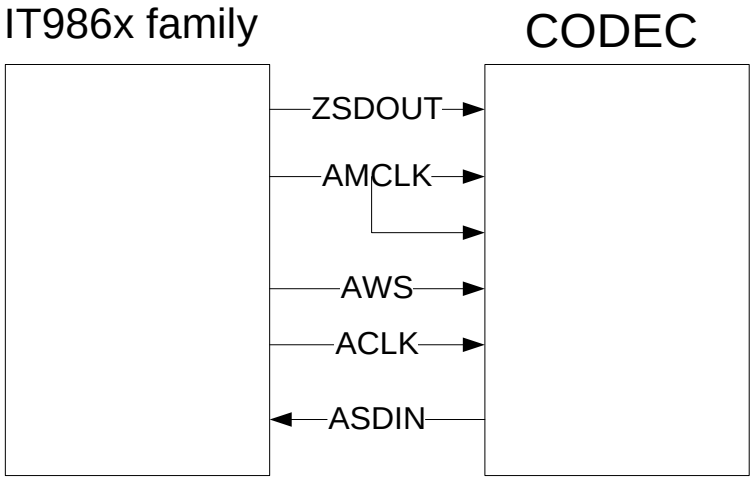
5.5 Digital Audio Interface

5.5.1 General Description

IT986x family features a standard audio interface to support the transmission of mono or stereo data to and from the DAC or ADC. The standard audio IT986x family support two data formats. One is standard IIS data format and the other is left justified data format. IT986x family audio interface may be configured as either master or slave. As a master interface mode, IT986x family generates the ACLK (ZCLK) and AWS (ZWS) and controls sequencing of the data transfer. In the slave mode, DAC or ADC generates the ACLK (ZCLK) and AWS (ZWS) and controls the sequencing of data transfer.

5.5.2 Digital Audio Interface Implementation

The audio interface in IT986x family has seven pins to support all the application implementation. The IT986x family can connect one DAC and one ADC. IT986x family can be connected to CODAC as well, which depends on the application's purpose. There are three kinds of interface implementations, all of which can be configured as either master or slave mode.



5.5.3 Audio Interface Data Formats

IT986x family supports IIS and left justified audio interface data formats.

In IIS mode, The MSB is available on the second rising edge of ACLK following the AWS transition. The other bits up to LSB are then transmitted in order. The figure below illustrates the IIS interface.

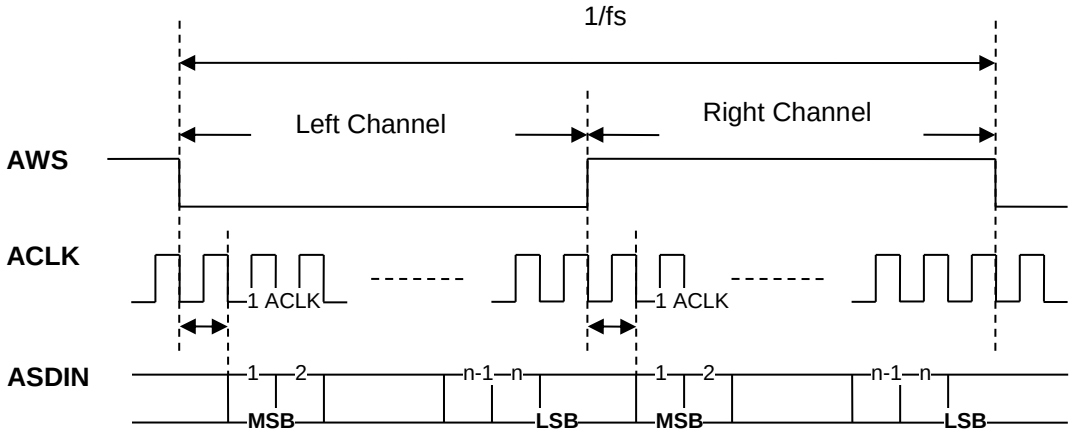


Figure 5-27. IIS Audio Interface

In Left justified mode, The MSB is available on the first rising edge of ACLK following the AWS transition. The other bits up to LSB are then transmitted in order. The figure below illustrates the IIS interface.

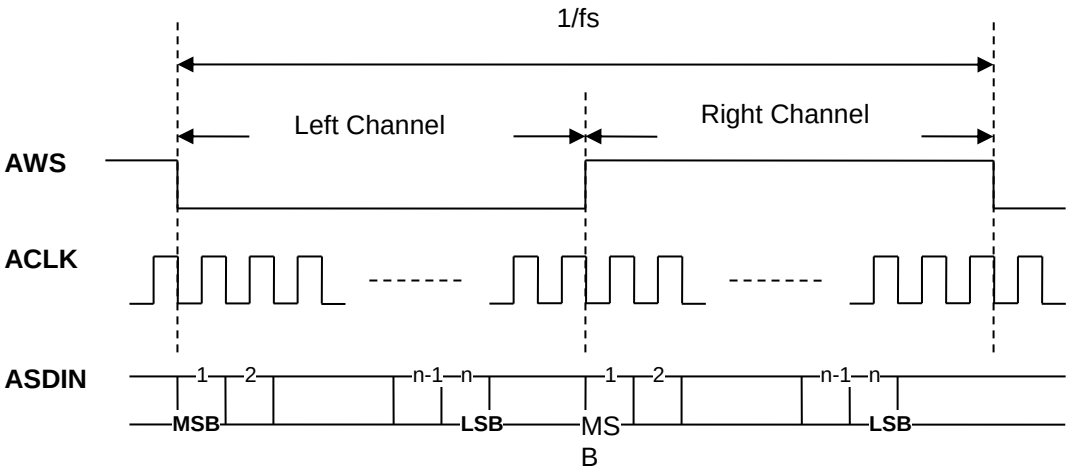


Figure 5-28. MSB Left Justified Interface

5.6 UART and IrDA Interface

The UART and IrDA controller is a serial communication element that implements the most common infrared communication protocols. In addition to the infrared modes, the device also provides the operation in the UART mode, which is backward compatible to 16550 to support the existing communication software.

It provides the following features:

- Firmware compatible with the high-speed NS 16C550A UART
- IrDA 1.3 SIR with up to 115.2 kbps data rate
- SIR pulse width programmable as 1.6 μs or 3/16 of the baud-rate pulse width
- Supports IrDA 1.3 FIR
- Multi-frame transmission and reception in FIR mode
- Back-to-back infrared frame transmission and reception in FIR mode
- 32-bit IEEE 802 CRC32 hardware CRC generators and checkers for FIR communications
- Break, parity, overrun, and framing error simulations in UART mode
- CRC error and physical error simulation in FIR mode

5.7 DMA Controller

IT986x family's Direct Memory Access controller is designed to enhance the system performance and reduce processor-interrupt generation. The system efficiency is improved by employing high-speed data transfer between the system and device. The DMA controller provides 8 channels for memory-to-memory, memory-to-peripheral, and peripheral-to-memory transfer with a shared buffer.

Here are the main features:

- An AHB slave port for DMA controller configuration
- 2 AHB master interfaces for data transfer
- 8 configurable DMA channels
- Supports chain transfer
- Memory-to-memory, memory-to-peripheral, and peripheral-to-memory transfers
- Group round-robin arbitration scheme with 4 priority levels
- Supports 8-, 16-, and 32-bit wide data transaction
- Supports big-endian and little-endian

5.8 Ethernet MAC Interface

The IT986x family provides a high-quality 10/100 Ethernet controller with DMA function. It includes an AHB wrapper, DMA engine, on-chip memories (TX FIFO and RX FIFO), MAC, and RMII interface. It is an Ethernet controller that provides AHB master capability and is fully compliant with the IEEE 802.3 100 Mbps and 10 Mbps specifications. The MAC DMA controller handles all data transfers between the system memory and on-chip memories. The DMA engine supports the zero-copy data transfer that drastically improves the system performance. The DMA engine can be used to reduce the CPU loading, maximize the performance, and minimize the FIFO size. It has on-chip memories for buffering, which does not require the external local buffer memory. The RMII interface can support two specific data rates, 10 Mbps and 100 Mbps. The functionality is identical at both data rates, and so is the signal timing relationship. The only difference between the 10 Mbps and 100 Mbps operations is the nominal clock frequency.

5.9 PLL Interface

IT986x family has three clock synthesizers to generate all of the internal clocks. The clock synthesizer can generate a wide range of programmable frequencies up to 1GHz. The clock synthesizer accepts 12 MHz reference clock input. Moreover, the system can even stop the reference clock after the PLL locks the target frequency and phase for power saving.

5.10 2D Graphice Engine

The 2D Graphics Accelerator supports the following functions:

- Bit Block Transfer (BitBlt) with ROP3 operation
- Mask plane with 1bpp, 2bpp, 4bpp, and 8bpp format
- Color expansion with 1bpp, 2bpp, 4bpp and 8bpp format
- Constant/Variable global alpha blending
- Coordinate transform
- Gradient (horizontal / vertical) fill with dithering / solid color fill
- Clipping window
- Supports following color formats:
  - 32-bit ARGB8888, ABGR8888, RGBA8888, and BGRA8888
  - 16-bit ARGB4444, ABGR4444, RGBA4444, BGRA4444, ARGB1555, ABGR1555, RGBA1555, and BGRA1555
  - 16-bit RGB565, and BGR565
  - Alpha A_8, A_4, A_2, and 1-bit black and white BW_1
- Color depth conversion from any to any RGB format with dithering
- Supports interrupt output
- 64-bit memory interface with maximum 4-pixel pipelined engine
- Up to 4096x4096 pixels display resolution
- Automatic clock gating

5.11 JPEG

The IT986x family's JPEG codec is based on the JPEG baseline standard and the arithmetic accuracy meets the requirement of the compatibility test of JPEG Part-2 (ISO/IEC10918-2). The maximum image size is 256M pixels (16376x16376). The parameters in the luminance and chrominance quantization table are fully programmable. The Huffman table is the default one suggested by the specification. The decoding process supports YUV 4:4:4, 4:2:2, 4:1:1 and 4:2:0 with the interleaved format, but the encoding process only supports the YUV 4:2:2 with the interleaved format. The progressive mode is not supported, while the sequential mode is supported.

5.12 Video

Supports H.264 decoding, which meets high/main profile level 3.1 and decodes 1080p@30fps (1920x1080) in real time.

5.13 SAR ADC

It is an 8-channel analog-to-digital converter which supports sampling rate of 1 Mhz with 12 bits resolution.

5.14 General-Purpose I/O

The GPIO controller is a user programmable general-purpose I/O controller. It is used to input/output data from the system and device. Each GPIO can be programmed as the input or output and pulled high or pulled low.

This GPIO can also be an interrupt input. It supports the rising edge, falling edge, both edge, and high/low level interrupt sense types. Each port can choose the pre-scale APB clock source as an interrupt source.

All GPIO pins are set to input upon the hardware reset.

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6. DC Characteristics

Absolute Maximum Ratings*

Core Power (VDD_CORE) ..... -0.3V to 2.0V

IO Power (VDD_IO) ..... -0.3V to 4.0V

Input Voltage (Vi)..... -0.3V to VDD_IO + 10%

Output Voltage (Vo)..... -0.3V to VDD_IO + 10%

Operation Temperature (Topt) .....-40°C to +85°C

Storage Temperature ..... -55°C to +125°C

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Normal Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD_CORE	Core Power (IVDD) – CPU	0.99	1.1	1.21	V
VDD_MEM	DDR2 Memory Power (IT9862, IT9866)	1.7	1.8	1.9	V
VDD_MEM	DDR3 Memory Power (IT9868)	1.35	1.5	1.65	V
VDD_IOA VDD_IOB	I/O Power	3.0	3.3	3.6	V
VDD_RTC	RTC Power	2.0	3.3	3.6	V
VDD_PLL	OSC Power	0.99	1.1	1.21	V
VDD_USB	USB Power	2.0	3.3	3.6	V
-	Operating Temperature	-40	-	+85	^{0}C

DC Electrical Characteristics

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7. AC Characteristics

7.1 Reset Timing

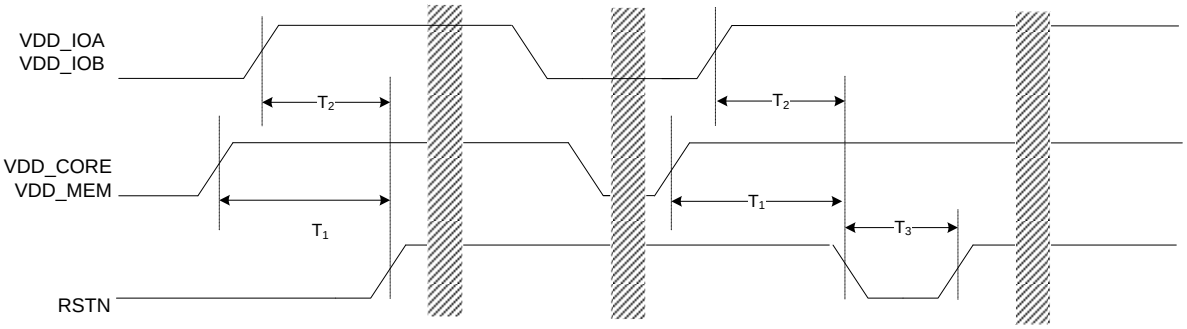

Figure 7-1. Reset Timing

Table 7-1. Reset Timing Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_1	Core Power (memory power) valid to reset inactive	-	50	-	ms
T_2	I/O Power valid to reset inactive	-	40	-	ms
T_3	Minimum reset pulse width	1	-	-	ms

Notes: The registers can be accessed 4 ms after the reset process is finished.

7.2 Power Sequence

Specific sequencing requirements shall be followed for all I/O power and core power

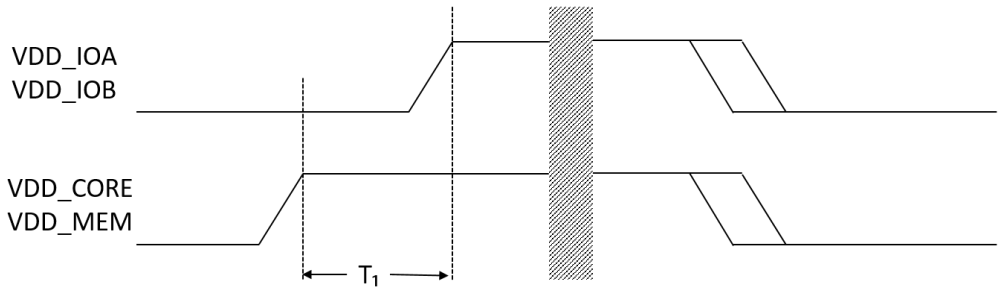

Figure 7-2. Power Sequence Timing

Table 7-2. Power Sequence Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_1	Core power (memory power) valid to I/O power valid	10	-	-	us

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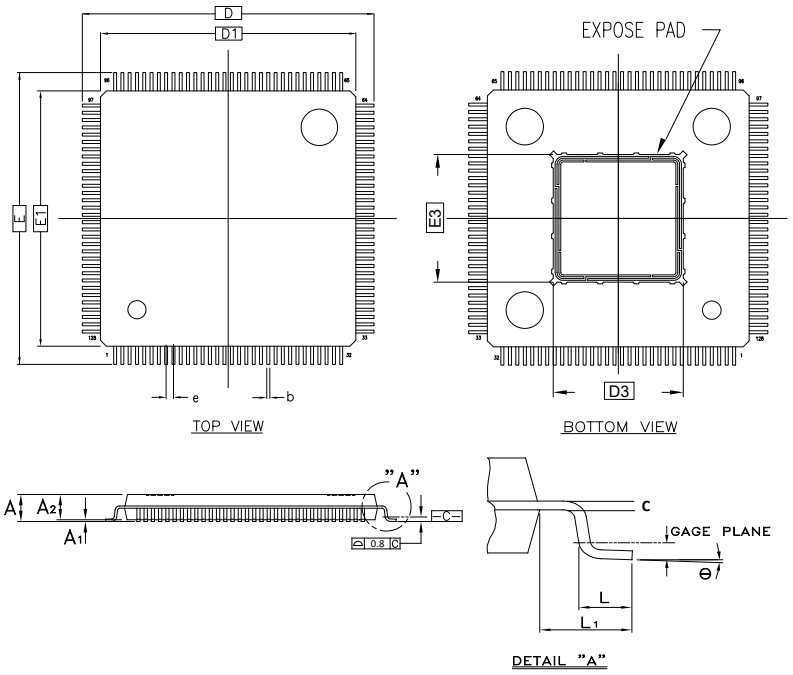
8. Package Information

8.1 IT986x Family Package Information

LQFP 128(14*14) Outline Dimensions for IT9862, IT9866, and IT9868
unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	0.063	-	-	1.60
A1	0.002	-	0.006	0.05	-	0.15
A2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.005	0.006	0.009	0.13	0.16	0.23
c	0.004	-	0.008	0.09	-	0.20
D / E	0.630 BSC			16.00 BSC		
D_1 / E_1	0.551 BSC			14.00 BSC		
D_3 / E_3	0.270	0.274	0.278	6.86	6.96	7.06
e	0.016 BSC			0.40 BSC		
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	0.039 REF.			1.0 REF.		
θ	0°	-	7°	0°	-	7°

Notes:
1. Dimensions D1 and E1 do not include mold protrusion, but mold mismatch is included.
2. Dimensions b does not include dambar protrusion.
3. Controlling dimensions: Millimeter

DI-E(274*274MIL)-LQFP128(14*14)v0

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9. Ordering Information

Part Number	Description	Package	Body Size
IT9862E/AW	Application Processor SoC	128 pins LQFP/EPAD	14*14 mm
IT9866E/AW	Application Processor SoC With H.264 Decoder	128 pins LQFP/EPAD	14*14 mm
IT9868E/AW	Application Processor SoC With H.264 Decoder	128 pins LQFP/EPAD	14*14 mm

All green components provided are in compliance with RoHS, and Halogen-Free.