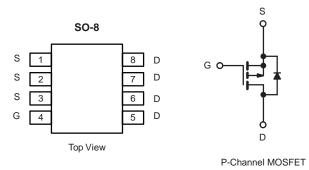


IRF9393TRPBF-VB Datasheet P-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY						
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^d	Q _g (Typ.)			
- 30	0.011 at V _{GS} = - 10 V	- 11.6	22 nC			
	0.012 at V _{GS} = - 4.5 V	- 10	22110			



FEATURES

- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET[®] Power MOSFET
- 100 % Rg Tested
- 100 % UIS Tested

APPLICATIONS

- Load Switches
- Notebook PCs
 - Desktop PCs



COMPLIANT HALOGEN

FREE vailable

Parameter	Symbol	Limit	Uni		
Drain-Source Voltage		V _{DS}	- 30	V	
Gate-Source Voltage		V _{GS}	± 20		
	T _C = 25 °C		- 11.6		
Continuous Drain Current (T 150 °C)	T _C = 70 °C		- 10.5		
Continuous Drain Current (T _J = 150 °C)	T _A = 25 °C	I _D	- 8.7 ^{a, b}		
	T _A = 70 °C		- 7.7 ^{a, b}	•	
Pulsed Drain Current	I _{DM}	- 40	— A		
Outility of the Device Divide Output	T _C = 25 °C		- 4.6		
Continuous Source-Drain Diode Current	T _A = 25 °C	- I _S	2.0 ^{a, b}		
Avalanche Current		I _{AS}	- 20		
Single-Pulse Avalanche Energy	L = 0.1 mH	E _{AS}	20	mJ	
	T _C = 25 °C		5.6	-	
Mauintura Davias Diasia atian	T _C = 70 °C	р	3.6	w	
Maximum Power Dissipation	T _A = 25 °C	P _D	2.5 ^{a, b}	VV	
	T _A = 70 °C		1.6 ^{a, b}		
Operating Junction and Storage Temperature Range	T _J , T _{sta}	- 55 to 150	°C		

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^{a, c}	t ≤ 10 s	R _{thJA}	39	50	°C/W	
Maximum Junction-to-Foot	Steady State	R _{thJF}	18	22	C/W	

Notes:

a. Surface mounted on 1" x 1" FR4 board.

c. Maximum under Steady State conditions is 85 °C/W. d. Based on $T_C = 25$ °C.

b. t = 10 s.

IRF9393TRPBF-VB

SPECIFICATIONS T _J = 25 °C, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static		•					
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA	- 30			V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	ID = - 750 UA		- 31		mV/°C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			5.5			
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = -250 \ \mu A$	- 1.0		- 3.0	V	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 25 V$			± 100	nA	
Zara Cata Valtaga Drain Current	1	$V_{DS} = -30 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$			- 1	μA	
Zero Gate Voltage Drain Current	IDSS	V _{DS} = - 30 V, V _{GS} = 0 V, T _J = 55 °C			- 5		
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge -10 \text{ V}, \text{ V}_{GS} = -10 \text{ V}$	- 30			А	
		V _{GS} = - 10 V, I _D = - 10 A		0.011		Ω	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 4.5 V, I _D = - 7 A		0.012			
Forward Transconductance ^a	9 _{fs}	V _{DS} = - 10 V, I _D = - 10 A		23		S	
Dynamic ^b	•	·	•		•	•	
Input Capacitance	C _{iss}			1960		pF	
Output Capacitance	C _{oss}	V _{DS} = - 15 V, V _{GS} = 0 V, f = 1 MHz		380			
Reverse Transfer Capacitance	C _{rss}			325			
Total Gate Charge		$V_{DS} = -15 \text{ V}, V_{GS} = -10 \text{ V}, I_{D} = -10 \text{ A}$		43	65	nC	
	Q _g			22	33		
Gate-Source Charge	Q _{gs}	$V_{DS} = -15 \text{ V}, V_{GS} = -4.5 \text{ V}, I_{D} = -10 \text{ A}$		6			
Gate-Drain Charge	Q _{gd}			11			
Gate Resistance	R _g	f = 1 MHz	0.3	1.3	2.5	Ω	
Turn-On Delay Time	t _{d(on)}			11	22		
Rise Time	t _r	V_{DD} = - 15 V, R_L = 3 Ω		13	25		
Turn-Off DelayTime	t _{d(off)}	$I_D \cong$ - 5 A, V_{GEN} = - 10 V, R_g = 1 Ω		32	50		
Fall Time	t _f			9	18		
Turn-On Delay Time	t _{d(on)}			44	70	ns	
Rise Time	t _r	V_{DD} = - 15 V, R_L = 3 Ω		100	160	-	
Turn-Off DelayTime	t _{d(off)}	$\text{I}_\text{D}\cong$ - 5 A, V_GEN = - 4.5 V, R_g = 1 Ω		28	50		
Fall Time	t _f			15	30		
Drain-Source Body Diode Characteris	tics	•					
Continuous Source-Drain Diode Current	ا _s	T _C = 25 °C			- 4.6	•	
Pulse Diode Forward Current	I _{SM}				- 50	A	
Body Diode Voltage	V _{SD}	I _S = - 2 A, V _{GS} = 0 V		- 0.75	- 1.2	V	
Body Diode Reverse Recovery Time	t _{rr}			28	45	ns	
Body Diode Reverse Recovery Charge		Q_{rr} Ir = -2 A, dl/dt = 100 A/us, T ₁ = 25 °C		20	40	nC	
Reverse Recovery Fall Time	t _a			13			
Reverse Recovery Rise Time	t _b	1		15		ns	

Notes:

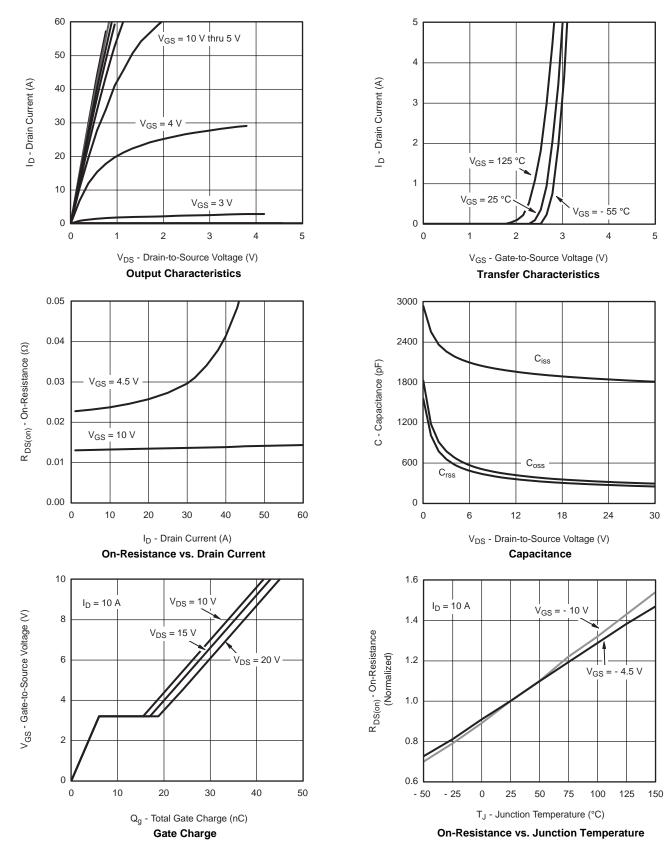
a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %.

b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

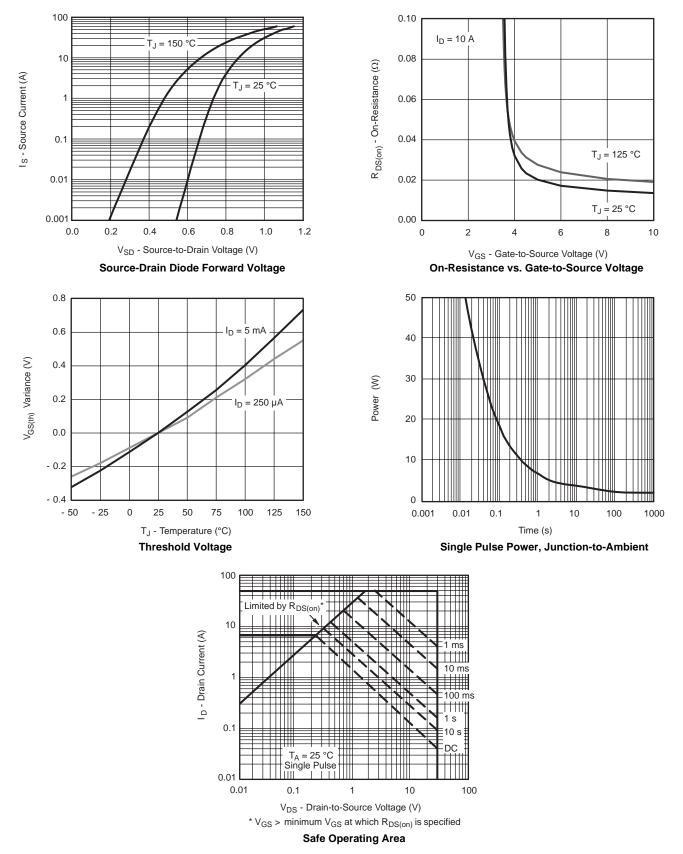
Bsemi



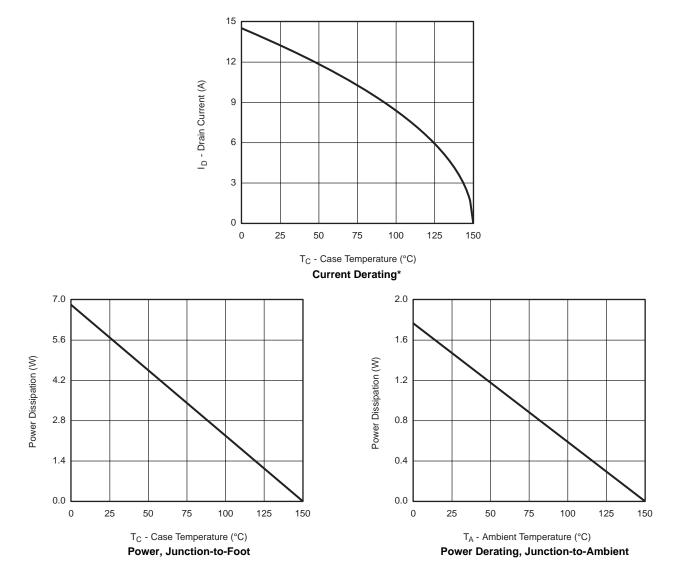


服务热线:400-655-8788



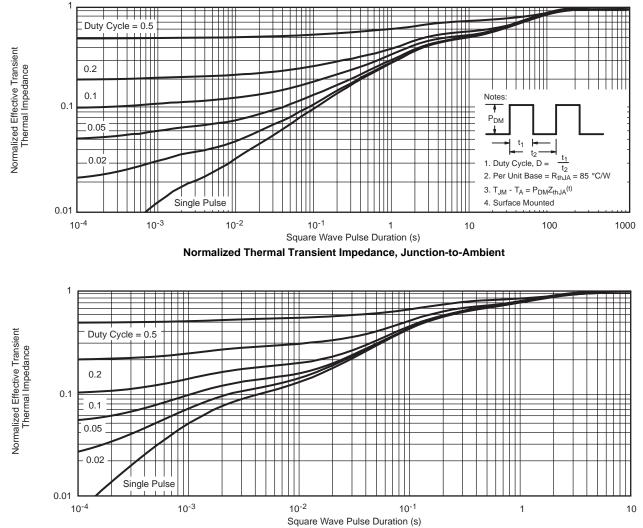






* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





Normalized Thermal Transient Impedance, Junction-to-Foot



SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012

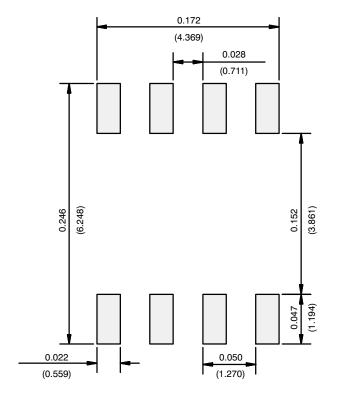




	MILLIM	IETERS	INC	HES	
DIM	Min	Мах	Min	Max	
A	1.35	1.75	0.053	0.069	
A ₁	0.10	0.20	0.004	0.008	
В	0.35	0.51	0.014	0.020	
С	0.19	0.25	0.0075	0.010	
D	4.80	5.00	0.189	0.196	
E	3.80	4.00	0.150	0.157	
е	1.27 BSC		0.050 BSC		
н	5.80	6.20	0.228	0.244	
h	0.25	0.50	0.010	0.020	
L	0.50	0.93	0.020	0.037	
q	0°	8°	0°	8°	
S	0.44	0.64	0.018	0.026	
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498					



RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads Dimensions in Inches/(mm)



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