

Programmable Differential Oscillator

YSV322PT VC-TCXO

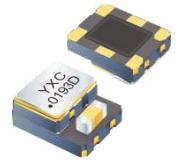


Applications

- Networking
- Industrial

Features

- Low Current Consumption
(44 mA for PECL 212.500 MHz at 3.3V)
- Low Jitter Design with New Developed IC
- Package Size: 3.2*2.5mm, 7.0*5.0mm



Specifications (规格参数)

Output Type	PECL	LVDS
Frequency Range 额定频率范围	10MHz ~ 1500MHz	10MHz ~ 1500MHz
Supply Voltage VDD 电源电压	2.5V, 3.3V	2.5V, 3.3V
Operating Temperature Range 工作温度	-40 ~ +85°C, or specify	-40 ~ +85°C, or specify
Storage Temperature Range 储存温度	-55 ~ +150°C	-55 ~ +150°C
Output Load 输出负载	50Ω into Vcc - 2V or Thevenin equivalent	100Ω
Rise Time/Fall Time (Tr / Tf : 10% ↔ 90% waveform) 上升沿/下降沿	0.2 nsec (typ.) 0.5 nsec (max.)	0.2 nsec (typ.) 0.4 nsec (max.)
Duty Cycle 占空比	45~55%	45~55%
Start-up Time 启动时间	5.0 msec (max.)	5.0 msec (max.)
RMS Jitter [12 kHz ~ 20 MHz] 相位抖动	1.5 psec (typ.)	1.5 psec (typ.)
Current Consumption (max.) (VDD = + 2.5V) 消耗电流	50MHz : 46mA	50MHz : 32mA
	125MHz : 50mA	125MHz : 40mA
	200MHz : 60mA	200MHz : 44mA
Current Consumption (max.) (VDD = + 3.3V) 消耗电流	50MHz : 50mA	50MHz : 35mA
	125MHz : 55mA	125MHz : 40mA
	200MHz : 62mA	200MHz : 44mA
Current with Output Disabled 禁用电流	18mA (typ.)	18mA (typ.)
Initial Calibration Tolerance 初始校准公差	±2.0 ppm (max.) at +25°C±2°C (at the shipment)	

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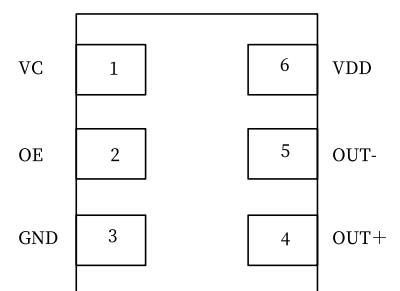
Output Type	PECL	LVDS
Frequency Stability 频率偏差	Temperature (ref to +25°C)	± 2.5 ppm over -40°C to +85°C (default)
	Aging at Ta = +25°C	± 1.0 ppm max, first year at 25°C
	Voltage Change	± 0.2 ppm max, for a ±5% input voltage change
	Load Change	± 0.2 ppm max, for a ±10% load condition change
	Reflow	± 1.0 ppm max, 1 reflow and measured 24 hours afterwards

Control Voltage Function on Pin 1	
Control Voltage Center and Range 控制电压	+1.5V ± 1.0V for both VDD = 2.5V and 3.3V
Frequency Pulling Range 牵引频率	± 8 ppm (min.)
Linearity 线性	± 1 % (typ.) ± 10% (max.)
Transfer Function 传递函数	Positive Transfer
Absolute Voltage 绝对电压	4.0V (max.)
Input Impedance 输入阻抗	770KΩ (typ.)
Output Enable Function on Pin 2	
Voltage VOH (Min.) / VOL (Max.) 输入电压	70% of VDD (min.) to enable output (Open connection prohibit.)
	30% of VDD (max.) to disable output

Pin Dimension (脚位尺寸)

Pin	#1	#2	#3
FUNCTION	Voltage Control	Out Enable	Ground
Pin	#4	#5	#6
FUNCTION	Output	Complementary	Supply Voltage

Pin Assignments



Top View

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Dimensions and Recommended Land Pattern (外观尺寸及推荐焊盘)

Dimensions (Unit: mm)	Recommended Land Pattern (Unit: mm)
<p>3.2*2.5mm</p>	
<p>7.0*5.0mm</p>	

Test Circuit (测试电路)

PECL	LVDS
<p>No Connection for TCXO Voltage Control VCTCXO</p> <p>VDD=3.3V: R1=R3=127Ω; R2=R4=82.5Ω VDD=2.5V: R1=R3=250Ω; R2=R4=62.5Ω</p>	<p>No Connection for TCXO Voltage Control VCTCXO</p>