

AUF7342Q-VB Datasheet

Dual P-Channel 60-V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^{d, e}	Q _g (Typ.)
- 60	0.054 at V _{GS} = - 10 V	- 5.3	17 nC
	0.060 at V _{GS} = - 4.5 V	- 5.0	

FEATURES

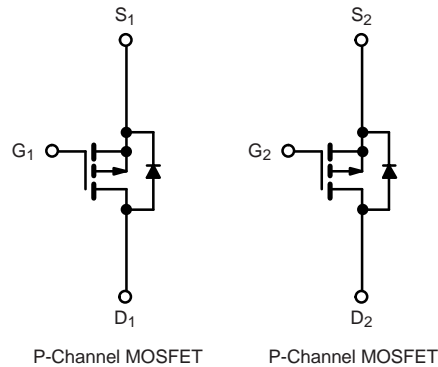
- Halogen-free
- TrenchFET[®] Power MOSFET
- 100 % UIS Tested

APPLICATIONS

- Load Switches



RoHS
COMPLIANT



ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	- 60	V	
Gate-Source Voltage	V _{GS}	± 20		
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	- 5.3 ^e	
		T _C = 70 °C	- 5.0 ^e	
		T _A = 25 °C	- 5.3 ^{a, b}	
		T _A = 70 °C	- 5.0 ^{a, b}	
Pulsed Drain Current	I _{DM}	- 32 ^e	A	
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C		- 4.1
		T _A = 25 °C		- 2.0 ^{a, b}
Avalanche Current	I _{AS}	- 20	mJ	
Single-Pulse Avalanche Energy	E _{AS}	20		
Maximum Power Dissipation	P _D	T _C = 25 °C	4.0	
		T _C = 70 °C	2.5	
		T _A = 25 °C	2.0 ^{a, b}	
		T _A = 70 °C	1.4 ^{a, b}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^{a, c}	R _{thJA}	38	50	°C/W	
Maximum Junction-to-Foot	R _{thJF}	20	25		

Notes:

- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- Maximum under Steady State conditions is 85 °C/W.
- Based on T_C = 25 °C.
- Limited by package.

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	- 60			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\text{ }\mu\text{A}$		- 31		mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$		4.5			
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	- 1.0		- 3.0	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -30\text{ V}, V_{GS} = 0\text{ V}$			- 1	μA
		$V_{DS} = -30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			- 5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq -10\text{ V}, V_{GS} = -10\text{ V}$	- 30			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -5\text{ A}$		0.054		Ω
		$V_{GS} = -4.5\text{ V}, I_D = -4.5\text{ A}$		0.060		
Forward Transconductance ^a	g_{fs}	$V_{DS} = -10\text{ V}, I_D = -5\text{ A}$		23		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = -15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		1345		pF
Output Capacitance	C_{oss}		210			
Reverse Transfer Capacitance	C_{rss}		180			
Total Gate Charge	Q_g	$V_{DS} = -15\text{ V}, V_{GS} = -10\text{ V}, I_D = -5\text{ A}$		32	50	nC
				15	25	
Gate-Source Charge	Q_{gs}	$V_{DS} = -15\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -5\text{ A}$		4		nC
Gate-Drain Charge	Q_{gd}		7.5			
Gate Resistance	R_g		$f = 1\text{ MHz}$		5.8	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -15\text{ V}, R_L = 15\text{ }\Omega$ $I_D \cong -1\text{ A}, V_{GEN} = -10\text{ V}, R_g = 1\text{ }\Omega$		10	15	ns
Rise Time	t_r		8	15		
Turn-Off DelayTime	$t_{d(off)}$		45	70		
Fall Time	t_f		12	25		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -15\text{ V}, R_L = 15\text{ }\Omega$ $I_D \cong -1\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 1\text{ }\Omega$		42	70	
Rise Time	t_r		35	60		
Turn-Off DelayTime	$t_{d(off)}$		40	70		
Fall Time	t_f		16	30		
Drain-Source Body Diode Characteristics						
Continous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			- 4.1	A
Pulse Diode Forward Current	I_{SM}				- 32	
Body Diode Voltage	V_{SD}	$I_S = -2\text{ A}, V_{GS} = 0\text{ V}$		- 0.75	- 1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = -2\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		34	60	ns
Body Diode Reverse Recovery Charge	Q_{rr}		22	40	nC	
Reverse Recovery Fall Time	t_a		11		ns	
Reverse Recovery Rise Time	t_b		23			

Notes:

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

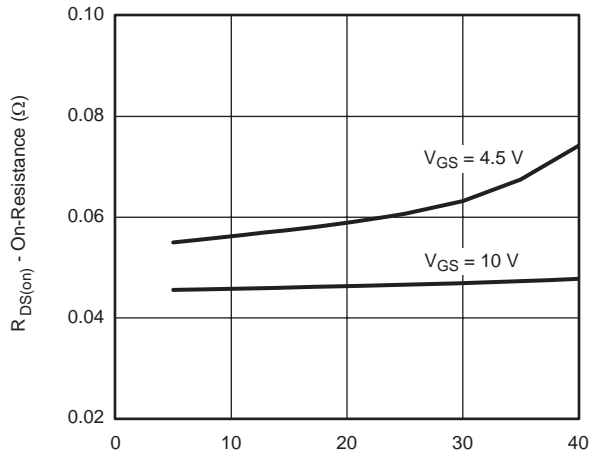
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Output Characteristics



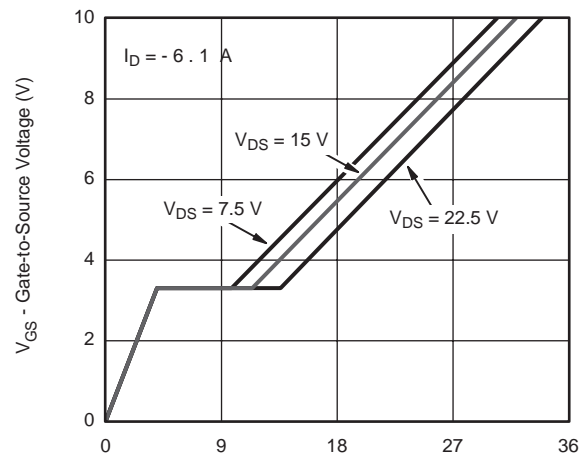
Transfer Characteristics



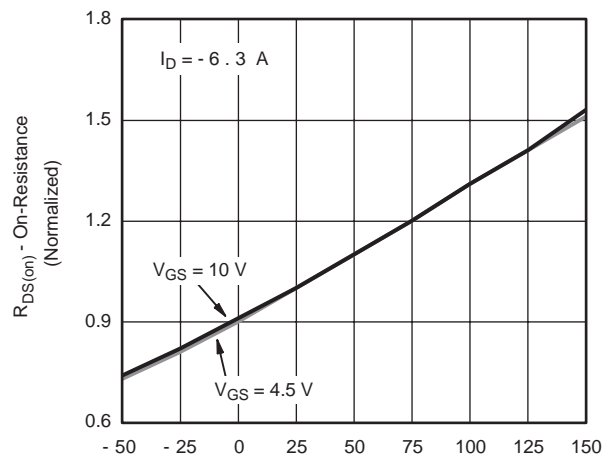
On-Resistance vs. Drain Current



Capacitance

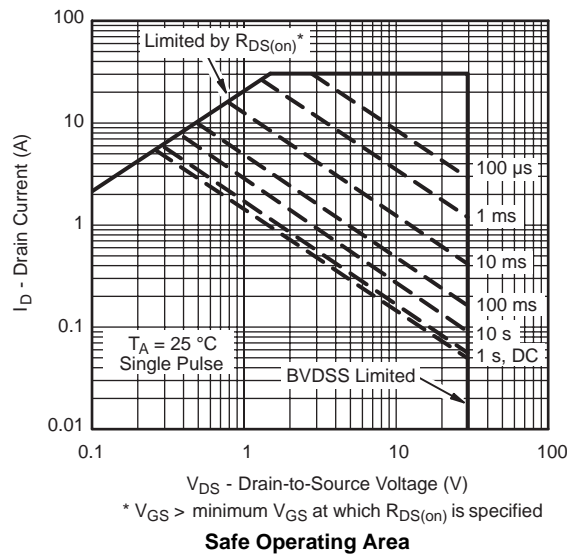
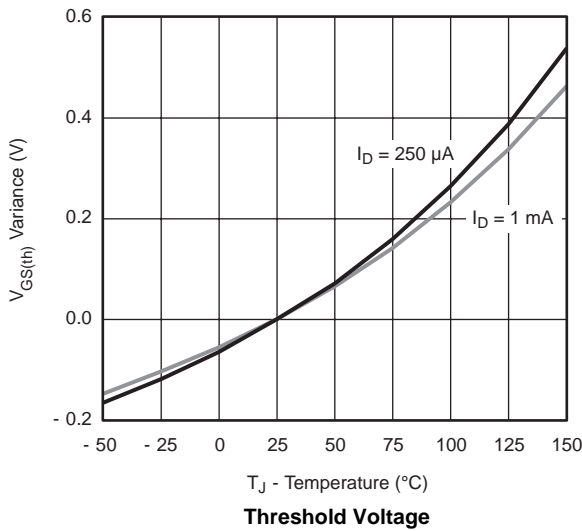
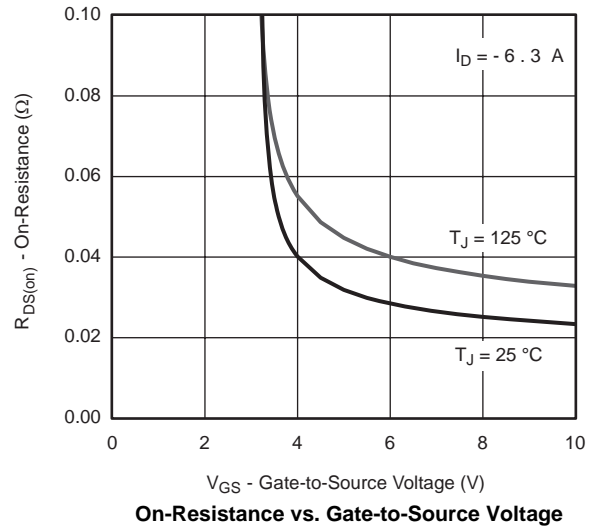
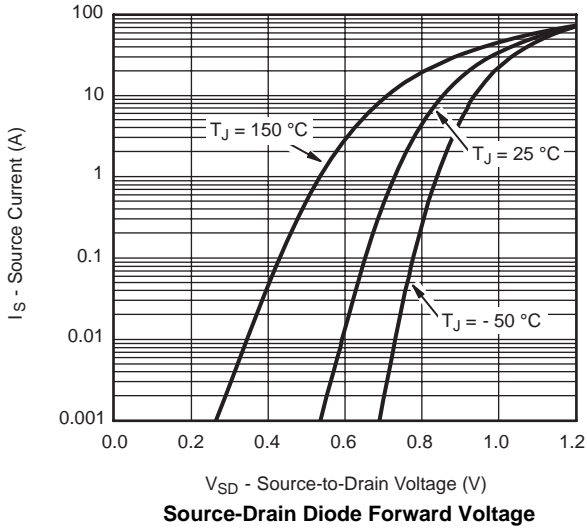


Gate Charge



On-Resistance vs. Junction Temperature

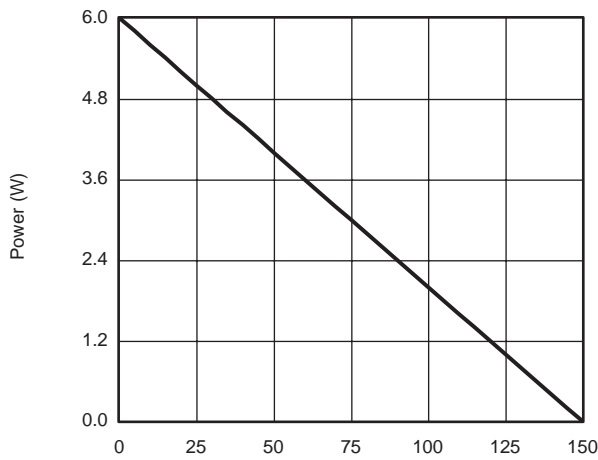
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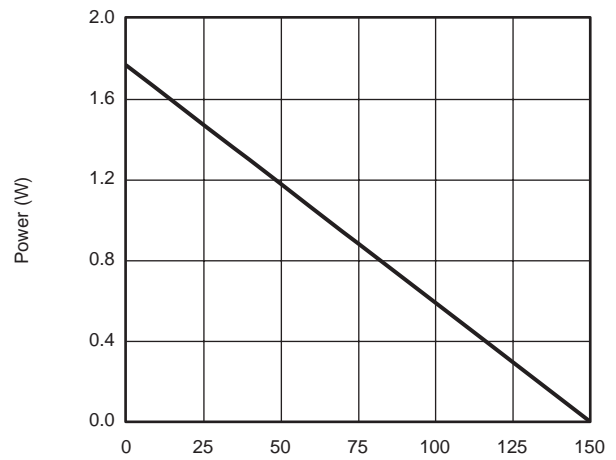
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Current Derating*



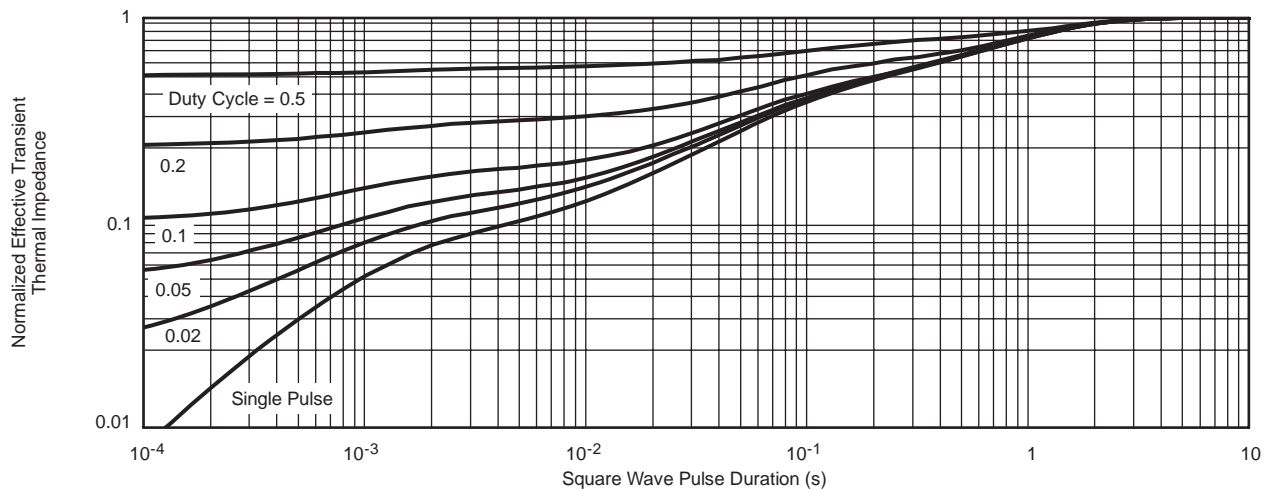
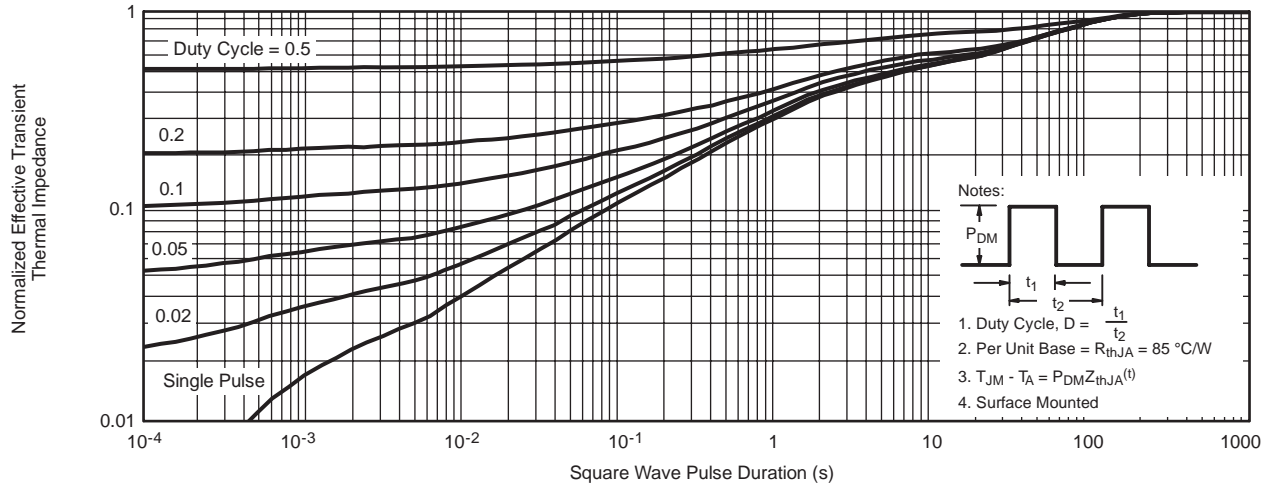
Power, Junction-to-Foot



Power Derating, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



SOIC (NARROW): 8-LEAD
JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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