

8-Ch Auto Sensitivity Calibration Capacitive Touch Sensor

SPECIFICATION V2.2

Drafter	Director	Review	Marketing	QA	Approval

■ Revision History

Rev.	Description of change	Date	Originator
1.0	Initial Release (ALRS08FB)	09.11.26	KD PARK
2.0	- LED control individually - LDO output - Variable sensing period of R.N.D channel - Sensitivity limit - Holding calibration after touch off for a while(about 200ms) - Unused CS pin -> Connect with GND	10.02.10	KD PARK
2.1	- Marking spec alteration ALRS 08 FB → ALRS 8	10.02.18	KD PARK
2.2	- Operating voltage 변경: max 5.5V -> max 3.3V	10.05.10	KD PARK

ALRS08FB (8-CH Auto Sensitivity Calibration Capacitive Touch Sensor)

1 Specification

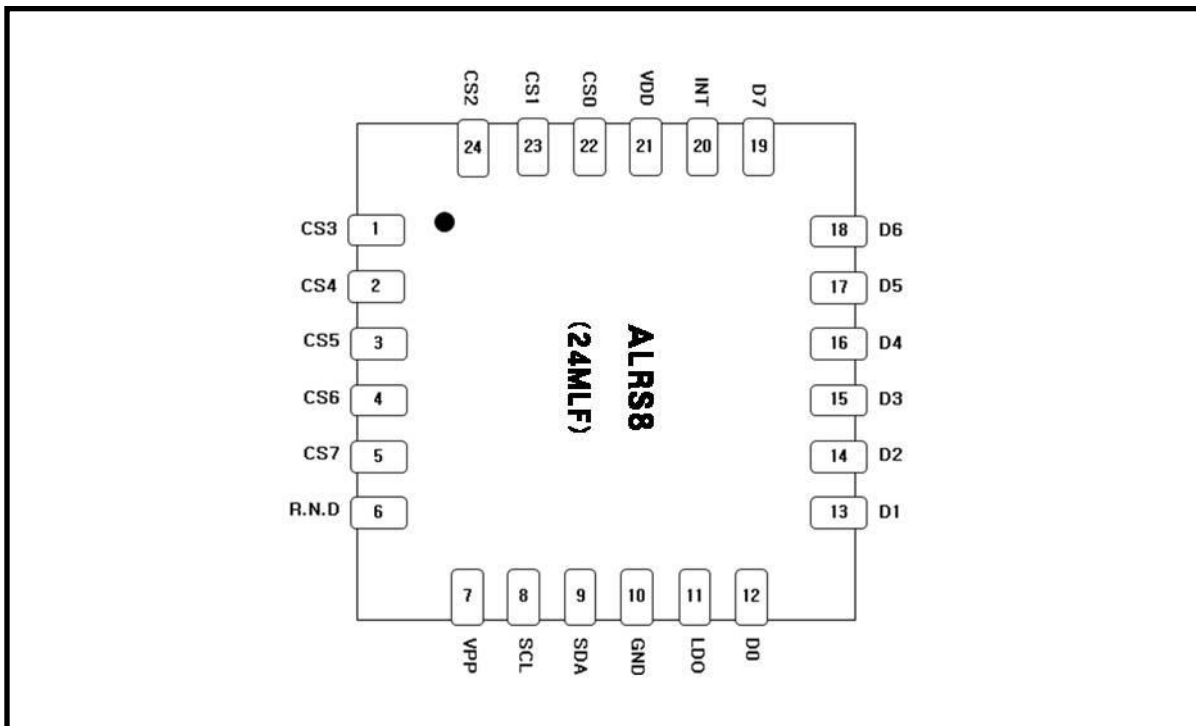
1.1 General Feature

- 8-Channel capacitive sensor with auto sensitivity calibration
- Available LED PWM drive up to 8
- Multi interface (Parallel outputs / I²C serial interface)
- Selectable output operation mode (Single output / Multi output)
- Selectable output logic level (Active high / Active low)
- Independently adjustable in 64 steps sensitivity
- Almost no external component needed
- Low current consumption
- Embedded common and normal noise elimination circuit
- RoHS compliant 24MLF package

1.2 Application

- Home appliances (TV, Monitor keypads)
- Mobile applications (PMP, MP3, Car navigation)
- Membrane switch replacement
- Sealed control panels, keypads
- Touch screen replacement application

1.3 Package (24MLF)



※ Drawings not to scale

ALRS08FB (8-CH Auto Sensitivity Calibration Capacitive Touch Sensor)

2 Pin Description

VDD, GND

Supply voltage and ground pin

R.N.D

Radio frequency Noise Detection pin. Normally, R.N.D pin does not connect to anywhere. But, in radio frequency noise environment, this pin must form a pattern line on PCB.

CS0~CS7

Capacitive sensor input pins.

VPP

VPP is external supply voltage for OTP writing.

LDO

LDO on-off control output pin for MCU wake-up.

D0~D7

Parallel output ports of CS0~CS7 respectively / LED PWM drive output ports. The structure of these parallel output ports are can be selected open drain NMOS for active low output level operation as well as open drain PMOS for active high output level operation.

SCL, SDA

SCL is I²C clock input pin and SDA is I²C data input-output pin. These ports have internal pull-up resistor which can be activated by "global_ctrl1" register¹ setting. In case of not use, this pin must be not connected to any circuitry.

INT

Touch sensing interrupt output pin.

¹ Refer to the chapter 8.2.6. Global option control 1 register

ALRS08FB (8-CH Auto Sensitivity Calibration Capacitive Touch Sensor)

2.1 ALRS08FB (24MLF package)

Pin No.	Name	I/O	Description	Protection
1	CS3	Analog Input	Capacitive sensor input3	VDD/GND
2	CS4	Analog Input	Capacitive sensor input4	VDD/GND
3	CS5	Analog Input	Capacitive sensor input5	VDD/GND
4	CS6	Analog Input	Capacitive sensor input6	VDD/GND
5	CS7	Analog Input	Capacitive sensor input7	VDD/GND
6	R.N.D	Analog Input	Radio frequency Noise Detection pin	VDD/GND
7	VPP	Power	External OTP writing Power (11.5V)	GND
8	SCL	Digital Input	I ² C clock input	VDD/GND
9	SDA	Digital Input / Output	I ² C data input-output Open drain NMOS structure	VDD/GND
10	GND	Ground	Supply ground	VDD
11	LDO	Digital Output	LDO on-off control output Open drain NMOS structure	VDD/GND
12	D0	Digital Output	Parallel output of CS0 (Active high/Active low) LED PWM drive output0 Open drain NMOS/ PMOS structure	VDD/GND
13	D1	Digital Output	Parallel output of CS1 (Active high/Active low) LED PWM drive output1 Open drain NMOS/ PMOS structure	VDD/GND
14	D2	Digital Output	Parallel output of CS2 (Active high/Active low) LED PWM drive output2 Open drain NMOS/ PMOS structure	VDD/GND
15	D3	Digital Output	Parallel output of CS3 (Active high/Active low) LED PWM drive output3 Open drain NMOS/ PMOS structure	VDD/GND
16	D4	Digital Output	Parallel output of CS4 (Active high/Active low) LED PWM drive output4 Open drain NMOS/ PMOS structure	VDD/GND
17	D5	Digital Output	Parallel output of CS5 (Active high/Active low) LED PWM drive output5 Open drain NMOS/ PMOS structure	VDD/GND
18	D6	Digital Output	Parallel output of CS6 (Active high/Active low) LED PWM drive output6 Open drain NMOS/ PMOS structure	VDD/GND
19	D7	Digital Output	Parallel output of CS7 (Active high/Active low) LED PWM drive output7 Open drain NMOS/ PMOS structure	VDD/GND
20	INT	Digital Output	Touch sensing interrupt output1 Open drain NMOS structure	VDD/GND
21	VDD	Power	Power (2.5V~3.3V)	GND
22	CS0	Analog Input	Capacitive sensor input0	VDD/GND
23	CS1	Analog Input	Capacitive sensor input1	VDD/GND
24	CS2	Analog Input	Capacitive sensor input2	VDD/GND

3 Absolute Maximum Rating

Battery supply voltage	3.3V
Maximum voltage on any pin	VDD+0.3
Maximum current on any PAD	100mA
Power Dissipation	800mW
Storage Temperature	-50 ~ 150℃
Operating Temperature	-20 ~ 75℃
Junction Temperature	150℃

Note : Unless any other command is noted, all above are operated in normal temperature.

4 ESD & Latch-up Characteristics

4.1 ESD Characteristics

Mode	Polarity	Max	Reference
H.B.M	Pos / Neg	8000V	VDD
		8000V	VSS
		8000V	P to P
M.M	Pos / Neg	500V	VDD
		500V	VSS
		500V	P to P
C.D.M	–	1000V	Field Induced Charge

4.2 Latch-up Characteristics

Mode	Polarity	Max	Reference
I Test	Positive	100mA	JESD78A
	Negative	-100mA	
V supply over 5.0V	Positive	18.0V	

ALRS08FB (8-CH Auto Sensitivity Calibration Capacitive Touch Sensor)

5 Electrical Characteristics

▪ **Note :** $V_{DD}=3.3V$, Typical system frequency (Unless otherwise noted), $T_A = 25^{\circ}C$

Characteristics	Symbol	Test Condition		Min	Typ	Max	Units
Power supply requirement and current consumption							
Operating voltage	V _{DD}			2.5		3.3	V
OTP writing voltage	V _{PP}			11	11.5	12	V
Current consumption	I _{DD}	V _{DD} = 3.3V	Slow calibration speed ²	–	55	85	μA
			Normal calibration speed	–	90	120	
			Fast calibration speed	–	160	210	
Reset and input level							
Internal reset voltage	V _{DD_RST}	T _A = 25℃		–	1.8	2.0	V
Input high level	V _{IH}	I _{IH} ≤ +5μA		V _{DD} *0.7		V _{DD} +0.3	V
Input low level	V _{IL}	I _{IL} ≤ +5μA		–0.3		V _{DD} *0.3	V
Self calibration time after system reset	T _{CAL}	Slow calibration speed		–	100	–	msec
		Normal calibration speed		–	80	–	
		Fast calibration speed		–	60	–	
Internal P/U resister of SDA(SCL) and INT	R _{P/U}			–	30(15)	–	kΩ
Touch sensing performance							
Minimum detective capacitance difference	ΔC _{MIN}			0.1	–	–	pF
Sense input capacitance range ³	C _S			–	–	50	pF
Output impedance (open drain)	Z _O	ΔC > ΔC _{MIN}		–	12	–	Ω
		ΔC < ΔC _{MIN}		–	30M	–	
System performance							
Max. output current (LED drive current)	I _{OUT}	Per unit drive output port		–	–	8.0	mA
LED PWM control ⁴	N _{PWM}			–	16	–	step
Sensitivity control ⁵				–	64	–	step
Max. I ² C SCL clock speed	f _{SCL_MAX}	Maximum internal I ² C clock		–	–	2	MHz
Touch expired time	T _{FX}	Normal calibration speed		–	30	–	sec

² Slow calibration speed isn't recommended if it has not problem of current consumption.

³ The sensitivity can be decreased with higher parallel capacitance of CS pin including parasitic capacitance made by neighbor GND or other pattern. The series resistor(under 1k Ω) of CS can be used in noisy condition to avoid mal-function from external surge and ESD.

⁴ Refer to the chapter 8.2.7. Global option control 2 register

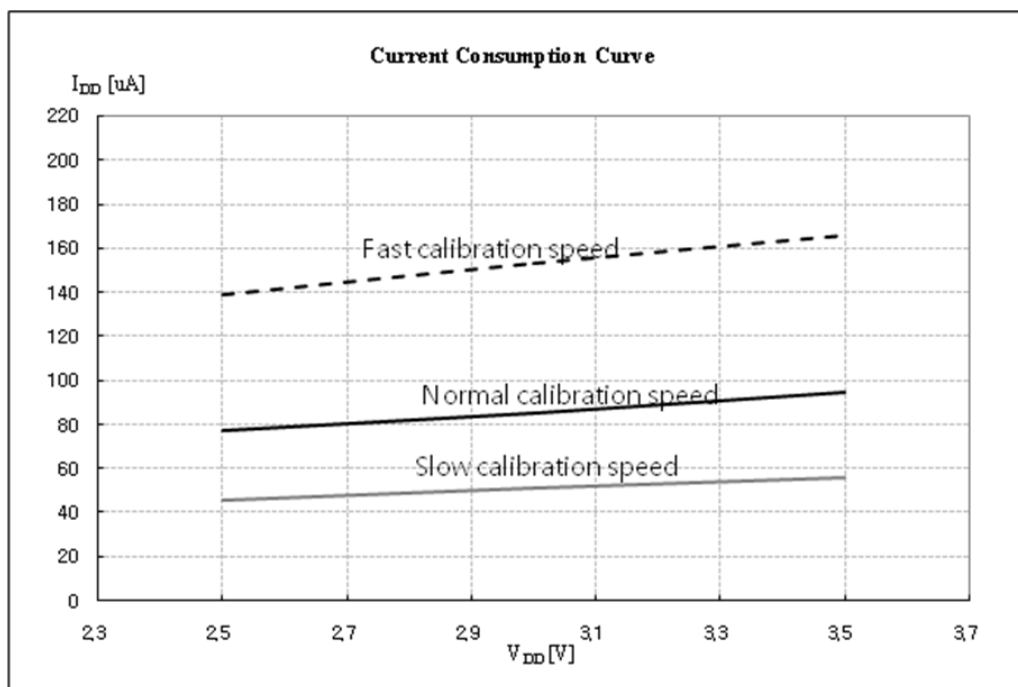
Refer to the chapter 8.2.14. LED luminance control register

⁵ Refer to the chapter 8.2.11. Sensitivity register

6 ALRS08 Implementation

6.1 Typical current consumption

ALRS08 uses internal bias circuit, so internal clock frequency and current consumption is fixed and no external bias circuit is needed. ALRS08 has three optional calibrations speed. Fast calibration speed needs more current consumption than normal or slow calibration speed. Internal clock frequency and calibration speed can be changed by I²C register setting⁶. Slow calibration speed isn't recommended if it has not problem of current consumption. The typical current consumption curve of ALRS08 is represented in accordance with V_{DD} voltage as below. Internal bias circuit can make the circuit design simple and reduce external components.



Typical current consumption curve of ALRS08

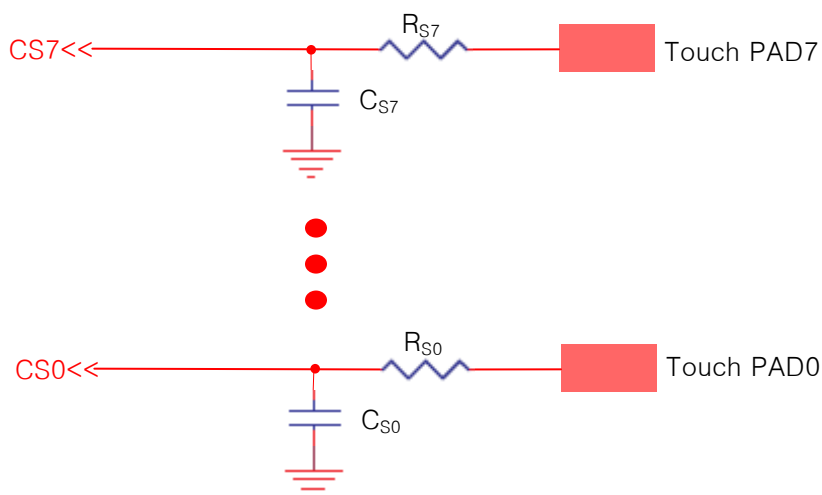
⁶ Refer to 8.2.6 Global option control 1

ALRS08FB (8-CH Auto Sensitivity Calibration Capacitive Touch Sensor)

6.2 CS implementation

ALRS08 has 64 step selections of sensitivity and internal surge protection resistor. Sensitivity of each sensing channel (CS) can be independently controlled on others. External components of CS pin such as series resistor or parallel capacitor isn't necessary. The parallel parasitic capacitance of CS pins caused by touch line, touch pad and neighbor GND or other pattern may affect sensitivity. The sensitivity will be decreased when bigger parallel parasitic capacitance of CS pin is added.

Parallel capacitor ($C_{S0\sim S7}$) of CS pin is useful in case of detail sensitivity mediation is required such as for complementation sensitivity difference between channels. Same as above parallel parasitic capacitance, sensitivity will be decreased when a big value of parallel capacitor ($C_{S0\sim S7}$) is used. Under 50pF capacitor can be used as sensitivity meditation capacitor and a few pF is usually used. The R_S , serial connection resistor of CS pins, may be used to avoid mal-function from external surge and ESD. (It might be optional.) From 200 Ω to 1k Ω is recommended for R_S . Refer to below CS pins application figure.



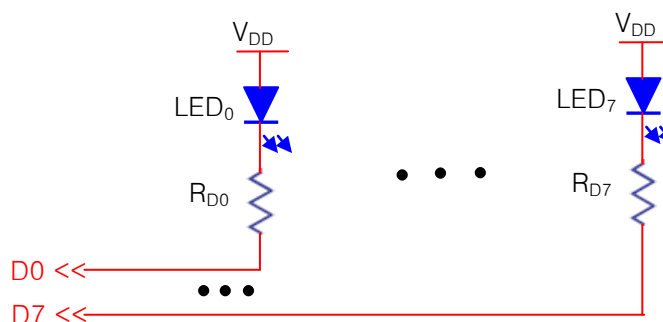
The ALRS08 has eight independent touch sensor input from CS0 to CS7. The internal touch decision process of each channel is separated from others. Therefore eight channel touch key board application can be designed by using only one ALRS08 without coupling problems.

The size and shape of PAD might have influence on the sensitivity. The sensitivity will be optimal when the size of PAD is approximately an half of the first knuckle (it's about 10 mm x 7 mm). The connection line of CS to touch PAD is recommended to be routed as short as possible to prevent from abnormal touch detect caused by connection line. The unused CS pin must be connected with the ground to prevent the unpredictable mal-function that occurred in the floating CS pin.

6.3 D0~D7 implementation

6.3.1 LED drive

ALRS08 has a function to control the LED using D0~D7 ports. For using D0~D7 as LED driver ports, LEDs and resistors must be equipped as below figure, and set the 'dx_mode' bit of "port mode" register⁷ as '1'. D0 ~ D7 ports can drive LEDs by "LED_control" register⁸ control. ALRS08 can drive up to 8 LED as below method. In addition, ALRS08 can control the LED luminance by using LED luminance control register⁹.



6.3.2 Parallel output

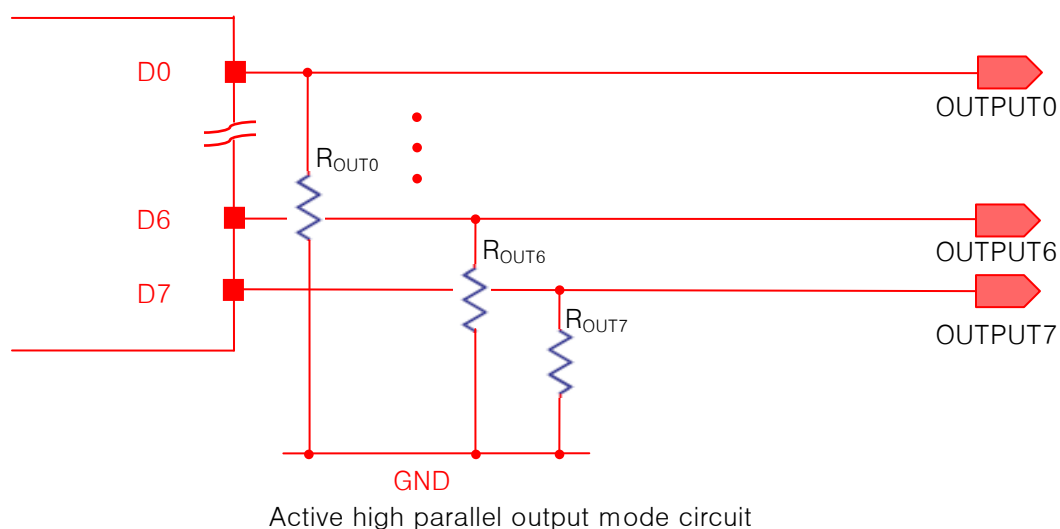
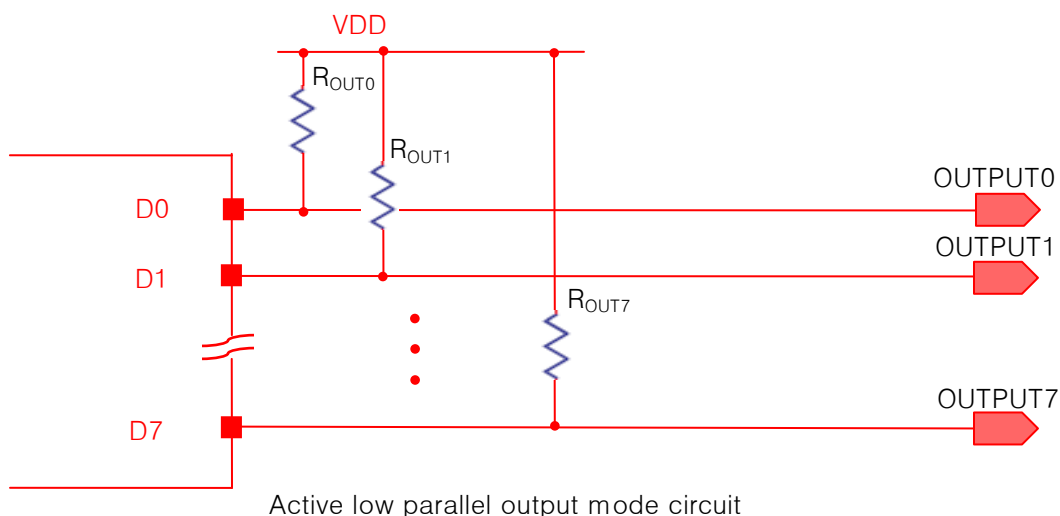
ALRS08 has 2 parallel output mode controlled by 'par_output_pol' bit of "global_ctrl2" register¹⁰ setting. One is active high parallel output mode and the other is active low parallel output mode. Structures of D0~D7 are same. In case of active high parallel output mode, parallel output ports (D0~D7) have an open drain PMOS structure. In other case of active low parallel output mode, parallel output ports (D0~D7) have an open drain NMOS structure. For this reason, both parallel output modes of ALRS08 need R_{OUT} as below figures. The maximum output drive current is 8mA, so over a few kΩ must be used as R_{OUT}. Normally 10kΩ is used as R_{OUT}.

⁷ Refer to the chapter 8.2.16. Output port mode control register.

⁸ Refer to the chapter 8.2.4. LED control register

⁹ Refer to the chapter 8.2.14. LED luminance control register

¹⁰ Refer to the chapter 8.2.7. Global option control 2.

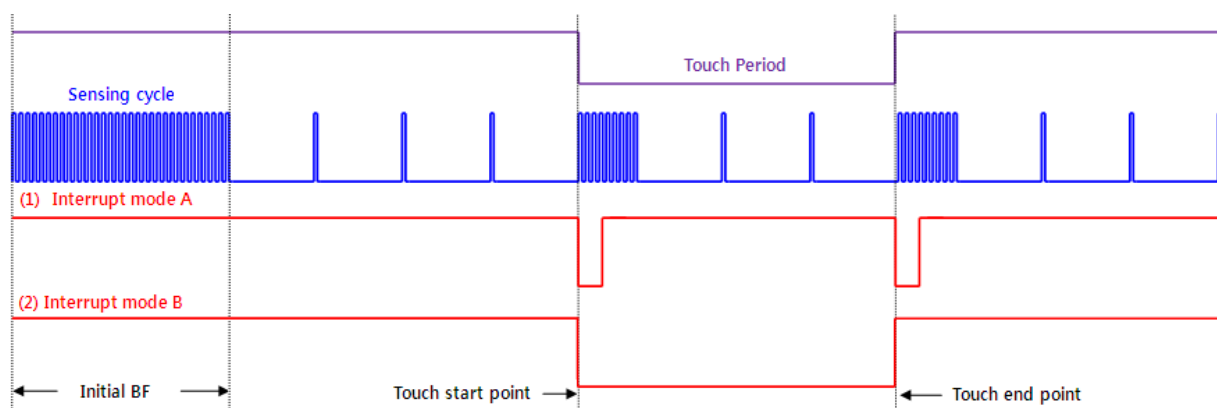


6.4 INT (Interrupt output) implementation

There are two interrupt operation is possible and can be selected by 'global_ctrl3' register¹¹ setting. In first interrupt operation case, the interrupt pulse is generated only during short period of every each channel touch start points and touch end point. In other interrupt operation case, the interrupt pulse is generated during every each channel touch duration. Interrupt pulse has logical low level in both two interrupt modes. Pull-up resistor about a few kΩ is required for interrupt output. Because of internal pull-up resistor of INT which can be activated by 'global_ctrl1' register¹² setting, external pull-up resistor can be removed.

¹¹ Refer to the chapter 8.2.8. Global option control 3.

¹² Refer to the chapter 8.2.6. Global option control 1.



6.5 LDO implementation

LDO pin acts as a LDO on-off control output pin. LDO on-off control output operation can help power saving in mobile application. Writing '1' on 'micom_sleep' bit of 'global_ctrl0' register¹³ make LDO output low. This low LDO output can be used as LDO which offers MCU power off signal. Any touch output writes '0' on 'micom_sleep' bit of 'global_ctrl0' register, and LDO output level becomes high again.

6.6 Change initial reset register values (OTP writing)

ALRS08 has eight integrated OTP (One Time Programmable) ROM cells. So, initial reset register values can be rewritten up to eight times. One OTP ROM cell size is 64-byte. User can write the data eight times to the OTP.

There are three operation modes about OTP read/write. These are automatically load operation mode, writing operation mode and reading operation mode.

Automatically load operation mode

After power reset, ALRS08 start to read the LSB of 00H address in each OTP ROM cells from 8th to 1st. ALRS08 automatically loads the data of the first OTP ROM cell of which LSB of 00H address has '0' into the control register. And then ALRS08 is starting to work with control register values that are loaded from OTP ROM cell. If there are no OTP ROM cell which has '0' in LSB of 00H address, ALRS08 is working with initial control register value.

Writing operation mode

OTP ROM cell writing provides the flexible reset register values that control all the operation options of ALRS08. So, additional communication programs on MCU for operation option select or register value setting are not required.

There are two writing operation modes. When the 'write_all' bit of 'mtp_cmd' register¹⁴ is '0', single byte writing mode is activated. User can select OTP ROM cell and address on which new

¹³ Refer to the chapter 8.2.2. Global option control 0.

¹⁴ Refer to the chapter 8.2.19. OTP ROM control register.

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register value is wanted to be written. OTP ROM cell selection is enabled by writing 'mtp_sel_en' bit of 'usr_mtp_sel' register¹⁵ '1'. When 'mtp_sel_en' bit of 'usr_mtp_sel' register is '0', OTM ROM cell is automatically selected from 1st to 8th. And, 'org_usr_mtp_sel' bits of 'usr_mtp_sel' register are for the OTP ROM selection. Read or write command register is 'mtp_cmd' registers and user can start writing by 'wr_start' bit of 'mtp_cmd' register setting as '1'. This 'wr_start' bit of 'mtp_cmd' register is recovered as '0' at ending of writing.

When the 'write_all' bit of 'mtp_cmd' register is '1', all bytes writing operation mode is activated. User can write all register frame data on selected OTP ROM cell. At this writing operation mode, only OTP ROM cell has to be selected. Writing start is same as single byte writing mode.

OTP ROM writing needs another 11.5V power supply voltage. VPP pin is for this writing 11.5V power.

Reading operation mode

When OTP ROM data is required to be read, user can read all the OTP ROM cell data by reading operation. When the 'read_all' bit of 'mtp_cmd' register is '0', user can read one byte data that is written on selected address of selected OTP ROM cell. OTP ROM cell and address selection are same as single byte writing operation mode. When 'mtp_sel_en' bit of 'usr_mtp_sel' register is '0', OTM ROM cell is automatically selected from 8th to 1st.

When the 'read_all' bit of 'mtp_cmd' register is '1', user can read all data on selected OTP ROM cell.

OTP ROM read start command bit is 'rd_start' bit of 'mtp_cmd' register. When the 'rd_start' bit of 'mtp_cmd' register is '1', ALRS08 starts to read. This 'rd_start' bit of 'mtp_cmd' register is recovered as '0' at ending of reading.

6.7 SCL, SDA implementation

SCL is I²C clock input and SDA is I²C data input-output. These ports have internal pull-up resistor which can be activated by 'global_ctrl1' register¹⁶ setting. SCL has Schmitt trigger input structure to prevent clock signal from being broken. Maximum supported I²C clock frequency is 2MHz. SDA has NMOS open drain structure and internal pull-up resistor of which value is 30kΩ typical. So, according to communication speed a few kΩ resistor must be used as pull-up resistor for proper data pulse rising time. For more details refer to 'Chapter 7. I²C Interface'.

¹⁵ Refer to the chapter 8.2.18. OTP ROM cell select register.

¹⁶ Refer to the chapter 8.2.6. Global option control 1.

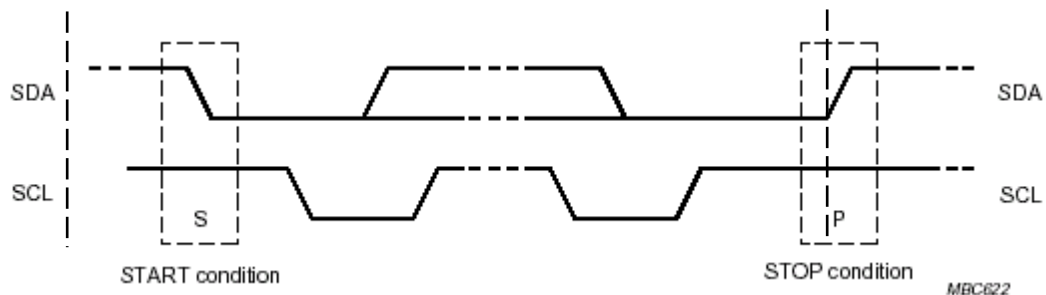
7 I²C Interface

7.1 I²C Enable / Disable

If the SDA or SCL signal goes to low, I²C control block is enabled automatically. And if the SDA and SCL signal maintain high during about 2 us, I²C control block is disabled automatically also.

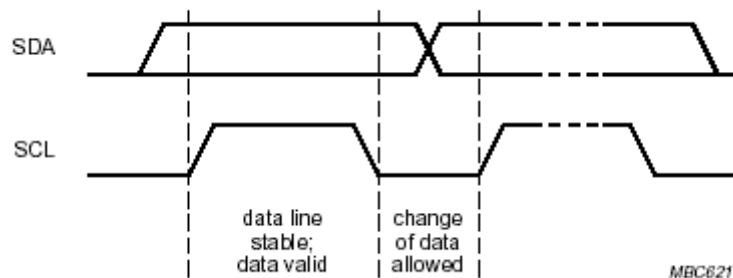
7.2 Start & stop condition

- ◀ Start Condition (S)
- ◀ Stop Condition (P)
- ◀ Repeated Start (Sr)



7.3 Data validity

The SDA should be stable when the SCL is high and the SDA can be changed when the SCL is low.

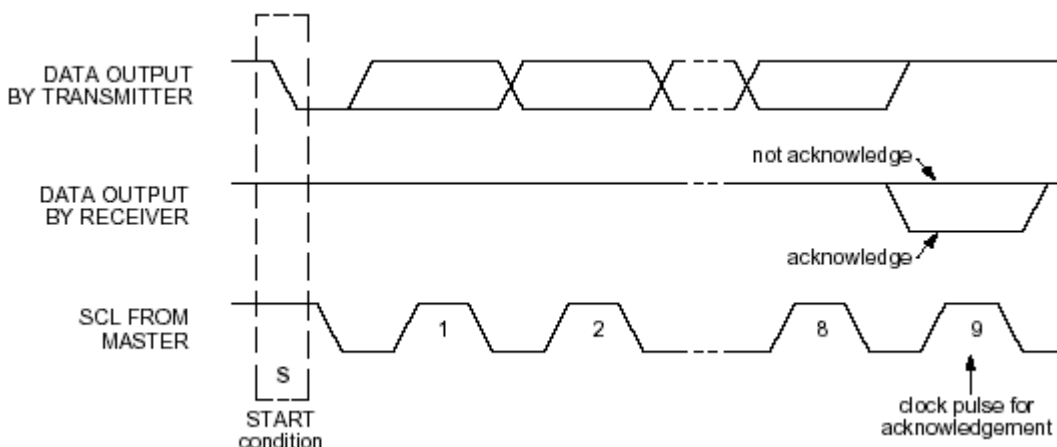


7.4 Byte format

The byte structure is composed with 8Bit data and an acknowledge signal.

7.5 Acknowledge

It is a check bit whether the receiver gets the data from the transmitter without error or not. The receiver will write '0' when it received the data successfully and '1' if not.



7.6 First byte

7.6.1 Slave address

It is the first byte from the start condition. It is used to access the slave device. The initial chip address of ALRS08 is '48' hex number and the chip address is possible to change with "I²C Address of ALRS08" register¹⁷. And if user uses the 7-bit chip address protocol for I²C, the initial chip address of ALRS08 is to be '24'.

7.6.2 R/W

The direction of data is decided by the bit and it follows the address data.

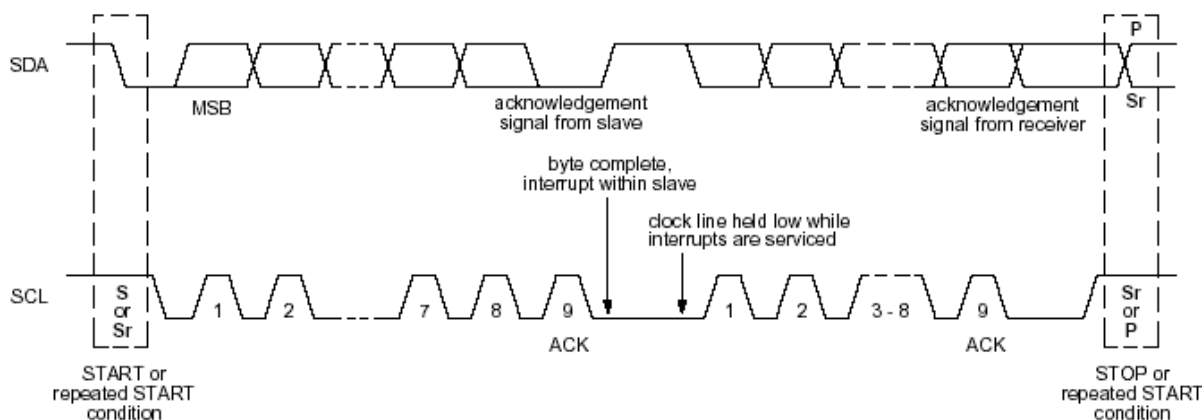


¹⁷ Refer to the chapter 8.2.3.

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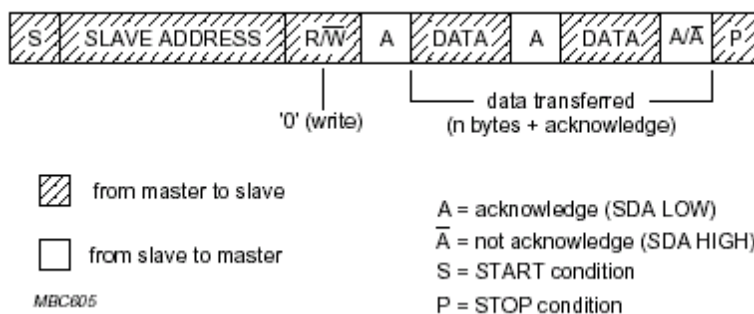


7.7 Transferring data

7.7.1 Write operation

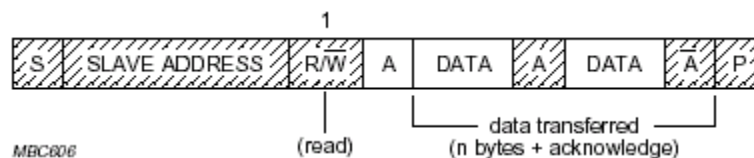
The byte sequence is as follows:

1. The first byte gives the device address plus the direction bit (R/W = 0).
2. The second byte contains the internal address of the first register to be accessed.
3. The next byte is written in the internal register. Following bytes are written in successive internal registers.
4. The transfer lasts until stop conditions are encountered.
5. The ALRS08 acknowledges every byte transfer.



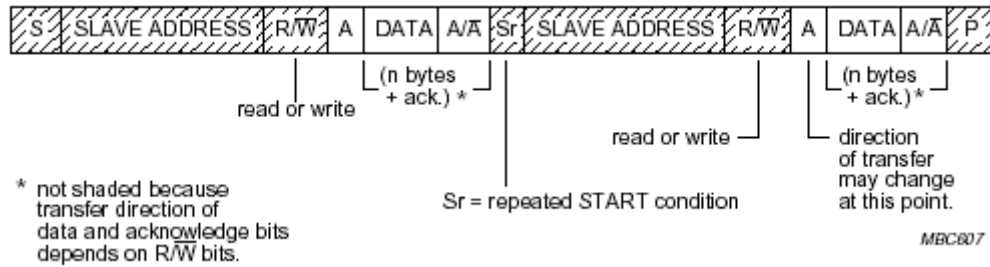
7.7.2 Read operation

The address of the first register to read is programmed in a write operation without data, and terminated by the stop condition. Then, another start is followed by the device address and R/W= 1. All following bytes are now data to be read at successive positions starting from the initial address.



ALRS08FB (8-CH Auto Sensitivity Calibration Capacitive Touch Sensor)

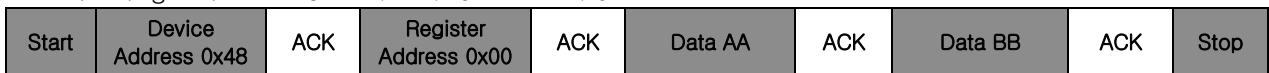
7.7.3 Read/Write Operation



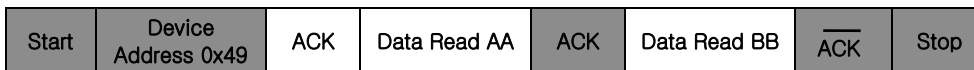
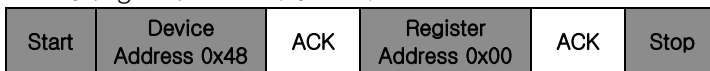
7.8 I²C write and read operations in normal mode

The following figure represents the I²C normal mode write and read registers.

☞ Write register 0x00 to 0x01 with data AA and BB



Read register 0x00 and 0x01



ALRS08FB (8-CH Auto Sensitivity Calibration Capacitive Touch Sensor)

8 ALRS08 Control Register List

- ◀ Note: The unused bits (defined as reserved) in I²C registers must be kept to zero.
- ◀ Note: The reset value of ALRS08 can be changed by MTP ROM writing.

8.1 I²C Register Map

Name	Addr. (Hex)	Reset Value (Bin)	Bit name of each bytes								
			Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
ch_enable /soft_rst	01H	1111 1111	ch7_en	ch6_en	ch5_en	ch4_en	ch3_en	ch2_en	ch1_en	ch0_en	
global_ctrl0	05H	---- 0--0	-	-	-	-	micom_sleep	-	-	bf_option	
i2c_id	06H	0100 1000	i2c_id								wr_bit
LED_control	07H	0000 0000	dl7_on	dl6_on	dl5_on	dl4_on	dl3_on	dl2_on	dl1_on	dl0_on	
output	2AH	0000 0000	o_ch7	o_ch6	o_ch5	o_ch4	o_ch3	o_ch2	o_ch1	o_ch0	
global_ctrl1	34H	0000 1010	int_pu_up	sda(scl)_pu_up	imp_sel_opt	irb_mode	irb_sel		rb_sel		
global_ctrl2	35H	---- -00-	-	-	-	-	-	pwm_sel	par_output_pol	-	
global_ctrl3	36H	-0-- -000	ldo_pu_up	int_out_mode	-	-	-	0	0	0	
global_ctrl4	37H	0000 1100	cal_pause	sen_lim_opt	sts_clr_en	response_ctrl			clk_off	sw_rst	
global_ctrl5	38H	0101 0100	cal_hold	sin_multi_mode	cal_hold_time				exp_op_en	exp_op_mode	
Sensitivity0	39H	--00 1001			sensitivity00						
Sensitivity1	3AH	--00 1001	-	-	sensitivity01						
Sensitivity2	3BH	--00 1001	-	-	sensitivity02						
Sensitivity3	3CH	--00 1001	-	-	sensitivity03						
Sensitivity4	3DH	--00 1001	-	-	sensitivity04						
Sensitivity5	3EH	--00 1001	-	-	sensitivity05						
Sensitivity6	3FH	--00 1001	-	-	sensitivity06						
Sensitivity7	40H	--00 1001	-	-	sensitivity07						
cal_speed	41H	1111 1010	bf_up		bf_down		bs_up		bs_down		
Variable fduty	42H	---- 0000	-	-	dm_fduty						
pwm0	43H	---- 0000	-	-	-	-	pwm0				
pwm1	44H	---- 0000	-	-	-	-	pwm1				
pwm2	45H	---- 0000	-	-	-	-	pwm2				
pwm3	46H	---- 0000	-	-	-	-	pwm3				
pwm4	47H	---- 0000	-	-	-	-	pwm4				
pwm5	48H	---- 0000	-	-	-	-	pwm5				
pwm6	49H	---- 0000	-	-	-	-	pwm6				
pwm7	4AH	---- 0000	-	-	-	-	pwm7				
sensitivity limit0	4BH	0000 0000	sen_limit_high1				sen_limit_high0				
sensitivity limit1	4CH	0000 0000	sen_limit_high3				sen_limit_high2				
sensitivity limit2	4DH	0000 0000	sen_limit_high5				sen_limit_high4				
sensitivity limit3	4EH	0000 0000	sen_limit_high7				sen_limit_high6				
port mode	4FH	0000 0000	d7_mode	d6_mode	d5_mode	d4_mode	d3_mode	d2_mode	d1_mode	d0_mode	

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Name	Addr. (Hex)	Reset Value (Bin)	Bit name of each bytes							
			Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
rd_ch_H1	53H	0000 0000	rd_ch_H1							
rd_ch_L1	54H	---- ---0	-	-	-	-	-	-	-	rd_ch_L1
sen_H	55H	--00 0000	-	-	sen_count[13:8]					
sen_L	56H	0000 0000	sen_count[7:0]							
ref_H	57H	--00 0000	-	-	ref_count[13:8]					
ref_L	58H	0000 0000	ref_count[7:0]							
rd_ch_H2	59H	0000 0000	rd_ch_H2							
rd_ch_L2	5AH	---- ---0	-	-	-	-	-	-	-	rd_ch_L2
usr_mtp_sel	5BH	0000 0000	0	0	0	mtp_sel_en	org_usr_mtp_sel			
mtp_cmd	5CH	0000 0000	0	0	write_all	read_all	0	0	wr_start	rd_start
mtp_status	5DH	---- ----	-	org_mtp_sel				wr_done_sts	rd_done_sts	no_load_sts
otp_add_sel	5EH	0000 0000	0	0	otp_add_sel					
otp_wr_data	5FH	0000 0000	otp_wr_data							
otp_rd_data	60H	---- ----	otp_rd_data							

ALRS08FB (8-CH Auto Sensitivity Calibration Capacitive Touch Sensor)

8.2 Details

8.2.1 Channel enable / reset register

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
01h	ch_enable /soft_rst	ch7_en	ch6_en	ch5_en	ch4_en	ch3_en	ch2_en	ch1_en	ch0_en

Description

Enable, disable and reset of each channel control register.

Bit name	Reset value	Function
chx_en	1	Channel enable / disable and Channel reset (chx_en is control bit for CSx channel)  0 : Channel disable and sensing channel reset  1 : Channel enable

8.2.2 Global option control register 0

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
05h	global_ctrl0	-	-	-	-	micom_sleep	-	-	bf_opt

Description

Operation mode selection control register.

Bit name	Reset value	Function
bf_opt	0	Operation mode selection  0 : Normal mode  1 : BF mode
micom_sleep	0	LDO output control register. This bit is cleared if any key is touched.  0 : LDO output high  1 : LDO output low

ALRS08FB (8-CH Auto Sensitivity Calibration Capacitive Touch Sensor)

8.2.3 I²C address of ALRS08

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
06h	i2c_id	i2c_id							wr_bit

Description

Chip address of ALRS08 control register. User can change this address value with OTP ROM write. During reset period OTP ROM data is loaded to registers.

Bit name	Reset value	Function
wr_bit	0	Write/Read address selection - 0 : Write address, 1 : Read address
i2c_id	0100100	Chip address of ALRS08.

8.2.4 LED Control

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
07h	LED_control	dl7_on	dl6_on	dl5_on	dl4_on	dl3_on	dl2_on	dl1_on	dl0_on

Description

LED ON/OFF control registers of D0~D7. Firstly output port is defined as a LED driver in the “port mode”¹⁸ register.

Bit name	Reset value	Function
dlx_on	0	LED on/off control (dlx_en is LED enable bit for DX output port) ✚ 0 : Turn the LED off ✚ 1 : Turn the LED on

8.2.5 Output data

Type: R

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
2Ah	output	o_ch7	o_ch6	o_ch5	o_ch4	o_ch3	o_ch2	o_ch1	o_ch0

Description

The output data register from channel 0 to channel 7.

Bit name	Reset value	Function
o_chx	0	o_chx is output bit for CSx channel ✚ 0 : No touch detected ✚ 1 : Touch detected

¹⁸ Refer to the chapter 8.2.16, Output port mode control

ALRS08FB (8-CH Auto Sensitivity Calibration Capacitive Touch Sensor)

8.2.6 Global option control 1

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
34h	global_ctrl1	int_pu_u p	sda(scl)_ pu_up	imp_sel_ opt	irb_ mode	irb_sel		rb_sel	

Description

This register controls the global options of ALRS08

Bit name	Reset value	Function
rb_sel	10	ALRS08 provides three internal calibration speeds and user can control the ALRS08 calibration speed by using these bits. ✚ 00, 01 : Fast ✚ 10 : Normal ✚ 11 : Slow
[irb_mode : irb_sel]	010	ALRS08 provides six internal I ² C clock frequencies. Slower one reduces current consumption. ✚ 000 : Fast ✚ 100 : Slowest ✚ 001 : Faster ✚ 101 : Slower ✚ 010 , 011 : Fastest ✚ 110,111: Slow
imp_sel_opt	0	Impedance of the sensing wire of all channels control bit. ✚ 0 : High impedance ✚ 1 : Low impedance except sensing period.
sda(scl)_pu_up	0	Pull-up resistor enable control bit on the SDA(SCL) port. ✚ 0 : Disable pull-up resistor ✚ 1 : Enable pull-up resistor
int_pu_up	0	Pull-up resistor enable control bit on the INT port. ✚ 0 : Disable pull-up resistor ✚ 1 : Enable pull-up resistor

8.2.7 Global option control 2

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
35h	global_ctrl2	-	-	-	-	-	pwm_sel	par_outp ut_pol	-

Description

This register controls the global options of ALRS08.

Bit name	Reset value	Function
par_output_p ol	0	Polarity of parallel outputs selection bit. ✚ 0 : Active low ✚ 1 : Active high
pwm_sel	0	LED PWM output enable bit. If user wants to use D0~D7 ports as a LED PWM drive ports, this bit has to be '1' under condition of the register "port mode" ¹⁹ is '1'. And the PWM width is controlled by LED PWM control register ²⁰ . ✚ 0 : Disable LED PWM output ✚ 1 : Enable LED PWM output

¹⁹ Refer to the chapter 8.2.16, Output port mode control

²⁰ Refer to the chapter 8.2.14, LED luminance control register.

ALRS08FB (8-CH Auto Sensitivity Calibration Capacitive Touch Sensor)

8.2.8 Global option control 3

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
36h	global_ctrl3	ldo_pu_up	int_out_mode	-	-	-	0	0	0

Description

This register controls the global options of ALRS08.

Bit name	Reset value	Function
int_out_mode	0	Interrupt output mode selection.  0 : Pulse mode (Interrupt mode A)  1 : Level mode (Interrupt mode B)
ldo_pu_up	0	Pull-up resistor enable control bit on the LDO port.  0 : Disable pull-up resistor  1 : Enable pull-up resistor

8.2.9 Global option control 4

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
37h	global_ctrl4	cal_pause	sen_lim_opt	sts_clr_en	response_ctrl			clk_off	sw_rst

Description

This register controls the global options of ALRS08.

Bit name	Reset value	Function
sw_rst	0	Software reset control bit.  0 : Not reset  1 : Reset
clk_off	0	System clock off control bit.  0 : Not clock off  1 : Clock off
response_ctrl	011	Numbers of continuous touch detections for touch decision.  Response ctrl[2:0] + 1 (Maximum time : 7)
sts_clr_en	0	Clear the 'mtp_status' register (Address: 5DH) control bit.  0 : Not clear  1 : Clear
sen_lim_opt	0	Sensitivity limit high enable control bit. If this bit is set '1', user can set the sensitivity limit high with "sensitivity limit" ²¹ register to prevent the mal-function from strong RF noise.  0 : Disable sensitivity limit high operation  1 : Enable sensitivity limit high operation
cal_pause	0	Holding calibration for a while after touch off (about 200ms).  0 : Disable holding calibration  1 : Enable holding calibration

²¹ Refer to the chapter 8.2.15, Sensitivity limit high control register.

ALRS08FB (8-CH Auto Sensitivity Calibration Capacitive Touch Sensor)

8.2.10 Global option control 5

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
38h	global_ctrl5	cal_hold	sin_multi_mode	cal_hold_time			exp_op_en	exp_op_mode	

Description

This register controls the global options of ALRS08.

Bit name	Reset value	Function
exp_op_mode	0	Output expiration time count mode selection bit.  0 : Expiration time counter is reset when any touch output is not appeared.  1 : Expiration time counter is reset when any output state is changed.
exp_op_en	0	Output expiration enable control bit.  0 : Don't use output expiration  1 : Use output expiration
cal_hold_time	0101	Output expiration Time control.  cal_hold_time[3:0] x 4 (seconds)
sin_multi_mode	1	Single/Multi output operation mode selection bit.  0 : Single output mode  1 : Multi output mode
cal_hold	0	Calibration hold of all channels control bit.  0 : Calibration  1 : Calibration hold

8.2.11 Sensitivity

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
39h ~ 40h	Sensitivity0 ~ sensitivity7	-	-	sensitivity00 ~ sensitivity07					

Description

ALRS08 can control the sensitivities of all channels independently.

Bit name	Reset value	Function
sensitivity00 ~ sensitivity07	001001	Sensitivities of each channel.  Sensitivity of CSx channel: {(sensitivity0x[5:0] x 0.1) + 0.05} (%).

ALRS08FB (8-CH Auto Sensitivity Calibration Capacitive Touch Sensor)

8.2.12 Calibration speed control register

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
41h	cal_speed	bf_up		bf_down		bs_up		bs_down	

Description

Calibration speed of each operation mode can be controlled by this 'cal_speed' register.

Bit name	Reset value	Function
bs_down	10	Down calibration speed in BS mode control bits.  00 : Fastest  01 : Fast  10 : Normal  11 : ref. count ← sen. count. (Most priority)
bs_up	10	Up calibration speed in BS mode control bits.  00 : Fastest  01 : Fast  10 : Normal  11 : Slow
bf_down	11	Down calibration speed in BF mode control bits.  00 : Fastest  01 : Fast  10 : Normal  11 : Slow
bf_up	11	Up calibration speed in BF mode control bits.  00 : Fastest  01 : Fast  10 : Normal  11 : Slow

8.2.13 Variable dummy sensing duty control register

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
42h	Variable fduty	-	-	dm_fduty					

Description

The sensing duty of the R.N.D channel can be increased with setting this register.

Bit name	Reset value	Function
dm_fduty	000000	The sensing duty of R.N.D channel control.  dm_fduty[5:0] * 19.8us

ALRS08FB (8-CH Auto Sensitivity Calibration Capacitive Touch Sensor)

8.2.14 LED luminance control register

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
43h ~ 4Ah	pwm0~pwm7	-	-	-	-	pwm0 ~ pwm7			

Description

LED luminance control.

Bit name	Reset value	Function
pwm _x	0000	The LED PWM control bits of Dx port. 0000 : The minimum low duty 1111 : The maximum low duty

8.2.15 Sensitivity limit high control register

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
4Bh	sensitivity limit0	sen_limit_high1				sen_limit_high0			
4Ch	sensitivity limit1	sen_limit_high3				sen_limit_high2			
4Dh	sensitivity limit2	sen_limit_high5				sen_limit_high4			
4Eh	sensitivity limit3	sen_limit_high7				sen_limit_high6			

Description

ALRS08 can control the sensitivity limit high of all channels independently.

Bit name	Reset value	Function
sen_limit_high0 ~sen_limit_high7	0000	Sensitivity limit high of each channel. 0000 : Disable 0100 : 1.60% 1000 : 2.00% 1100 : 4.00% 0001 : 1.00% 0101 : 1.70% 1001 : 2.20% 1101 : 5.00% 0010 : 1.20% 0110 : 1.80% 1010 : 2.50% 1110 : 7.50% 0011 : 1.50% 0111 : 1.90% 1011 : 3.00% 1111 : 10.00%

8.2.16 Output port mode control

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
4Fh	port mode	d7_mode	d6_mode	d5_mode	d4_mode	d3_mode	d2_mode	d1_mode	d0_mode

Description

This register controls the mode of output port.

Bit name	Reset value	Function
dx_mode	0	Select the output port operation mode of each channels. 0 : Parallel output mode 1 : LED drive mode

ALRS08FB (8-CH Auto Sensitivity Calibration Capacitive Touch Sensor)

8.2.17 Sense, reference count read register

Type: R

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
53h	rd_ch_H1	rd_ch_H1							
54h	rd_ch_L1	-	-	-	-	-	-	-	rd_ch_L1
55h	sen_H	-	-	sen_count[13:8]					
56h	sen_L	sen_count[7:0]							
57h	ref_H	-	-	ref_count[13:8]					
58h	ref_L	ref_count[7:0]							
59h	rd_ch_H2	rd_ch_H2							
5Ah	rd_ch_L2	-	-	-	-	-	-	-	rd_ch_L2

Description

ALRS08 provides the special function to read sense count of each channels or reference count.

Bit name	Reset value	Function
rd_ch_H1	00000000	Read channel indication register. 00000001 : Dummy channel 00000010 : CS0 channel 00000100 : CS1 channel 00001000 : CS2 channel 00010000 : CS3 channel 00100000 : CS4 channel 01000000 : CS5 channel 10000000 : CS6 channel
rd_ch_L1	0	Read channel indication register. 1 : CS7 channel
sen_count[13:8]	0000000	Sense count data of most significant six bits. Sense count [13:8]
sen_count[7:0]	00000000	Sense count data of least significant eight bits. Sense count [7:0]
ref_count[13:8]	0000000	Reference count data of most significant six bits. Reference count [13:8]
ref_count[7:0]	00000000	Reference count data of least significant eight bits. Reference count [7:0]
rd_ch_H2	00000000	Read channel confirm register. 00000001 : Dummy channel 00000010 : CS0 channel 00000100 : CS1 channel 00001000 : CS2 channel 00010000 : CS3 channel 00100000 : CS4 channel 01000000 : CS5 channel 10000000 : CS6 channel
rd_ch_L2	0	Read channel confirm register. 1 : CS7 channel

ALRS08FB (8-CH Auto Sensitivity Calibration Capacitive Touch Sensor)

8.2.18 OTP ROM cell select register

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
5Bh	usr_mtp_sel	0	0	0	mtp_sel_en	org_usr_mtp_sel			

Description

The OTP ROM cells of ALRS08 are made up of eight memory cells of 64 bytes. ALRS08 provides the way to access OTP ROM cells with this register. User can select the OTP ROM cell with 'org_usr_mtp_sel' bits and if user doesn't want to select the OTP ROM cell directly, 'mtp_sel_en' bit leaves '0', then OTP ROM cell is selected the automatically.

Bit name	Reset value	Function
org_usr_mtp_sel	0000	OTP ROM cell selection bits. 0000, 0001 : 1st OTP ROM cell 0010 : 2nd OTP ROM cell 0011 : 3rd OTP ROM cell 0100 : 4th OTP ROM cell 0101 : 5th OTP ROM cell 0110 : 6th OTP ROM cell 0111 : 7th OTP ROM cell 1000 : 8th OTP ROM cell
mtp_sel_en	0	OTP ROM cell selection enable bit. 0 : Select OTP ROM cell automatically 1 : Select OTP ROM cell by user

8.2.19 OTP ROM control register (OTP ROM command)

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
5Ch	mtp_cmd	0	0	write_all	read_all	0	0	wr_start	rd_start

Description

OTP ROM commands to access.

Bit name	Reset value	Function
rd_start	0	Reading selected OTP ROM cell start command bit. 0 : Don't start 1 : Start to read
wr_start	0	Writing on selected OTP ROM cell start command bit. 0 : Don't write 1 : Start to write
read_all	0	Unit of reading the selected OTP ROM cell control bit. 0 : 1-Byte reading 1 : All bytes of selected OTP ROM cell reading
write_all	0	Unit of writing on selected OTP ROM cell control bit. 0 : 1-Byte writing 1 : All bytes of selected OTP ROM cell writing

ALRS08FB (8-CH Auto Sensitivity Calibration Capacitive Touch Sensor)

8.2.20 OTP ROM status register.

Type: R

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
5Dh	mtp_status	-	org_mtp_sel				wr_done_sts	rd_done_sts	no_load_sts

Description

This register indicates the status of operation of selected one OTP ROM cell.

Bit name	Reset	Function
no_load_sts	-	This bit indicates whether some data are loaded from OTP ROM cells. 0 : There is some data loaded from OTP ROM cells 1 : No data loaded from OTP ROM cells
rd_done_sts	-	This bit indicates the end of reading. 0 : 1 : End of reading
wr_done_sts	-	This bit indicates the end of writing. 0 : 1 : End of writing
org_mtp_sel	-	These bits indicate that OTP ROM cell is loaded at initial time. 0000 : No loaded 0001 : 1st OTP ROM cell 0010 : 2nd OTP ROM cell 0011 : 3rd OTP ROM cell 0100 : 4th OTP ROM cell 0101 : 5th OTP ROM cell 0110 : 6th OTP ROM cell 0111 : 7th OTP ROM cell 1000 : 8th OTP ROM cell

8.2.21 OTP ROM data address select register

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
5Eh	otp_add_sel	0	0	otp_add_sel					

Description

Register for the specific address of selected OTP ROM cell. User can access OTP ROM data of specific address by leaving 'read_all' and 'write_all' bits in the 'mtp_cmd' register '0', selecting the OTP ROM cell with 'usr_mtp_sel' register and selecting the specific address with this register.

Bit name	Reset	Function
otp_add_sel	000000	Select specific address of selected OTP ROM cell. otp_add_sel[5:0] : Address

ALRS08FB (8-CH Auto Sensitivity Calibration Capacitive Touch Sensor)

8.2.22 OTP ROM data register to write

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
5Fh	otp_wr_data	otp_wr_data							

Description

The data register to write on specific address of selected OTP ROM cell.

Bit name	Reset	Function
otp_wr_data	00000000	Data register to write. otp_wr_data[7:0] : Data

8.2.23 OTP data register to read

Type: R

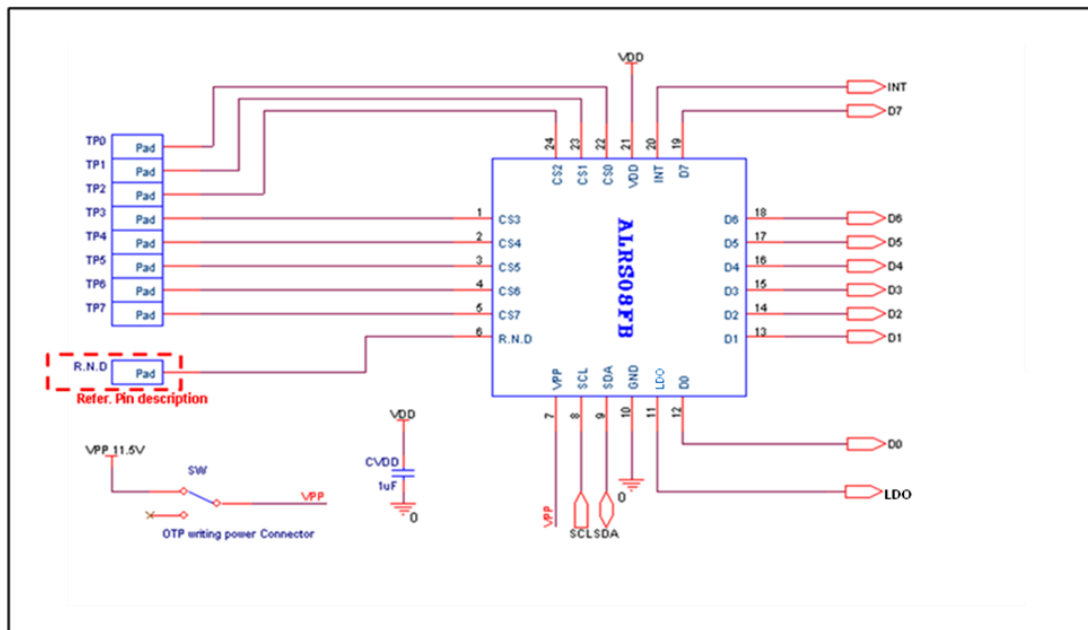
Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
60h	otp_rd_data	otp_rd_data							

Description

The data register for reading data from specific address of selected OTP ROM cell.

Bit name	Reset	Function
otp_rd_data	----	Data register for reading OTP ROM data. otp_rd_data [7:0] : Data

9 Recommended Circuit Diagram



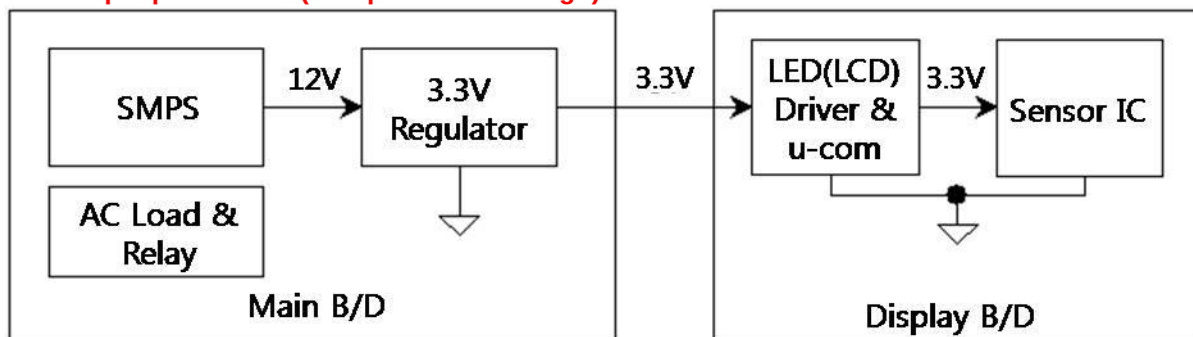
ALRS08FB(24MLF) Application Example Circuit for parallel output

- ✦ ALRS08 is reset by internal reset circuit. VDD voltage rising time should be shorter than 100msec for proper operation.
- ✦ Normally, R.N.D pin dose not connection to anywhere. But, in radio frequency noise environment, R.N.D pin must form a pattern line on PCB.
- ✦ The VDD periodic voltage ripple over 50mV and the ripple frequency is lower than 10 kHz can cause wrong sensitivity calibration. To prevent above problem, power (VDD, GND) line of touch circuit should be separated from other circuit. Especially LED driver power line or digital switching circuit power line certainly should be treated to be separated from touch circuit.
- ✦ The CS patterns also should be routed as short as possible and the width of line might be about 0.25mm.
- ✦ Parallel capacitor of CS pin could be useful in case detail sensitivity mediation is required such as for complementation sensitivity difference between channels.
- ✦ Serial connection resistor of CS pins may be used to avoid mal-function from external surge and ESD.
- ✦ The capacitor that is between VDD and GND is an obligation. It should be located as close as possible from ALRS08.
- ✦ The CS pattern routing should be formed by bottom metal (opposite metal of touch PAD).
- ✦ The empty space of PCB must be filled with GND pattern to strengthen GND pattern and to prevent external noise from interfere with sensing frequency.
- ✦ The D0 ~ D7 are open drain output ports. Therefore, in the case of active high output or active low output, the pull-up or pull-down resistor should be needed as above figure.
- ✦ Unused CS pins may be connected to GND for stable operation.
- ✦ 'Vpp' pin for 11.5V voltage input is needed at OTP ROM writing only.

ALRS08FB (8-CH Auto Sensitivity Calibration Capacitive Touch Sensor)

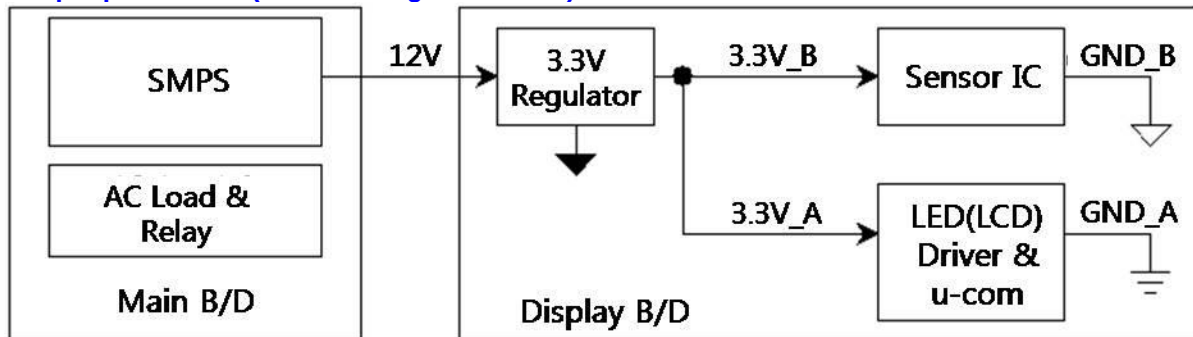
9.1 Example – Power Line Split Strategy PCB Layout

A. Not split power Line (Bad power line design)

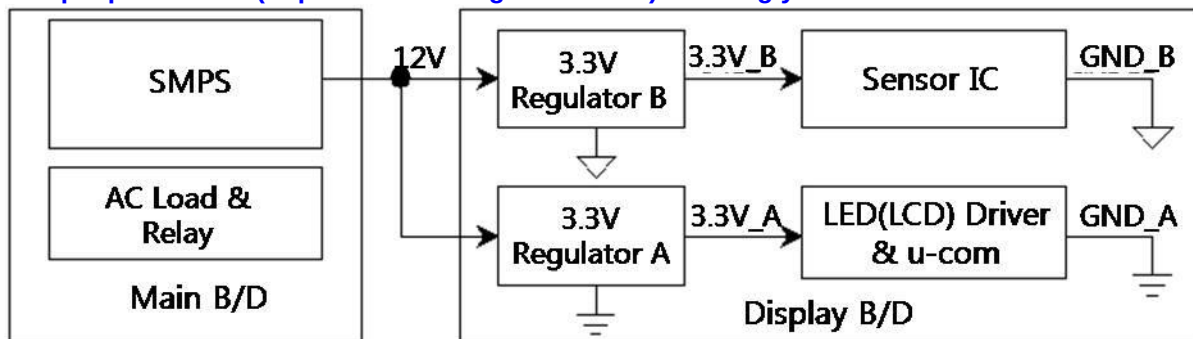


- The noise that is generated by AC load or relay can be loaded at 3.3V power line.
- A big inductance might be appeared in case of the connection line between main board and display board is too long, moreover the voltage ripple could be generated by LED (LCD) display driver at VDD (3.3V).

B. Split power Line (One 3.3V regulator used) – Recommended



C. Split power Line (Separated 3.3V regulator used) – Strongly recommended



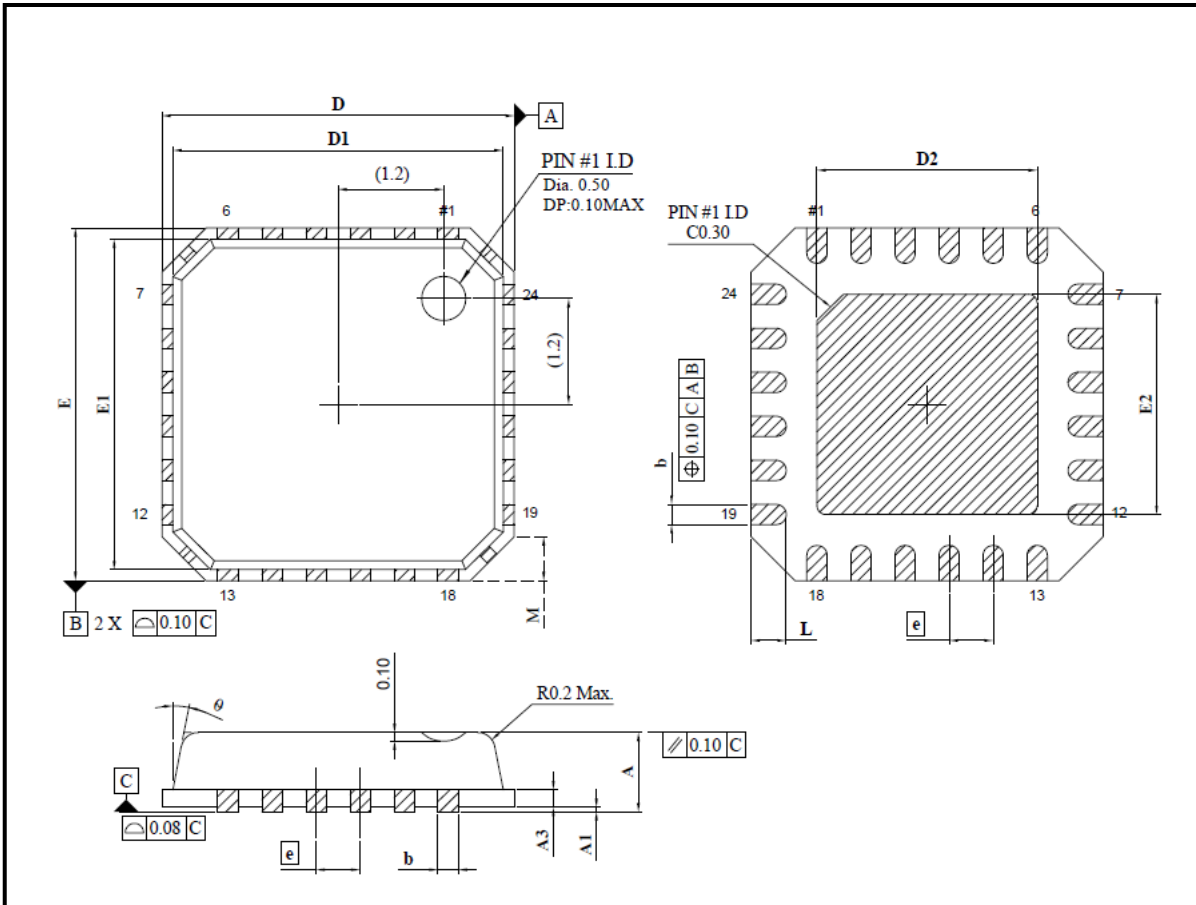
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10 MECHANICAL DRAWING

10.1 Mechanical Drawing of ALRS08FB (24MLF package)



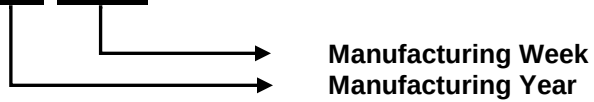
DIM	MIN.	NOR.	MAX.	NOTES
A	0.75	0.85	0.95	1.0 DIMENSIONING & TOLERANCEING CONFIRM TO ASME Y14.5M-1994.
A1	0.00	-	0.05	
A3		0.20 REF.		
b	0.18	0.23	0.28	
D		4.00 BSC.		
D1		3.75 BSC.		2.0 ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
D2	2.40	2.50	2.60	
E		4.00 BSC.		
E1		3.75 BSC.		3.0 COPLANARITY APPLIES TO THE EXPOSED HEAT SLUG AS WELL AS THE TERMINAL.
E2	2.40	2.50	2.60	
e		0.50 BSC.		4.0 RADIUS ON TERMINAL IS OPTIONAL. 5.0 MOLD SURFACE ROUGHNESS : 0.8~1.0m(Ra)
L	0.35	0.40	0.45	
M	0.45	0.50	0.55	
θ	-	11°	12°	

11 MARKING DESCRIPTION

Device Code : **ALRS 8**



Weekly Code : **YY WW**



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NOTES:

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