

FDS4885C-NL-VB Datasheet

N-and P-Channel 40V (D-S) MOSFET

PRODUCT SUMMARY				
	V _{DS} (V)	R _{DS(on)} (Ω) Typ.	I _D (A) ^a	Q _g (Typ.)
N-Channel	40	0.015 at V _{GS} = 10 V	9.0	13.3
		0.018 at V _{GS} = 4.5 V	7.6	
P-Channel	- 40	0.017 at V _{GS} = - 10 V	-8.0	13
		0.022 at V _{GS} = - 4.5 V	-6.8	

FEATURES

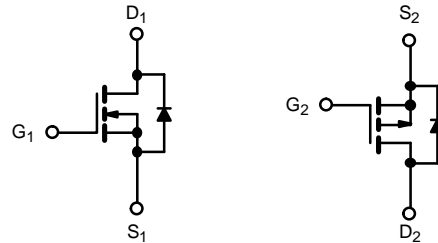
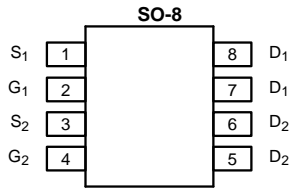
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- 100 % R_g and UIS Tested
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Motor Drive



ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)					
Parameter	Symbol	N-Channel	P-Channel	Unit	
Drain-Source Voltage	V _{DS}	40	- 40	V	
Gate-Source Voltage	V _{GS}	± 20	± 20		
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	9.0	- 8.0	A
		T _C = 70 °C	7.6	- 6.8	
		T _A = 25 °C	6.8 ^{b, c}	-5.6 ^{b, c}	
		T _A = 70 °C	5.4 ^{b, c}	- 4.3 ^{b, c}	
Pulsed Drain Current (10 μs Pulse Width)	I _{DM}	35	- 30	A	
Source-Drain Current Diode Current	I _S	T _C = 25 °C	3.6		- 3.6
		T _A = 25 °C	1.6 ^{b, c}		- 1.6 ^{b, c}
Pulsed Source-Drain Current	I _{SM}	35	- 30	mJ	
Single Pulse Avalanche Current	I _{AS}	20	- 20		
Single Pulse Avalanche Energy	E _{AS}	25	20	W	
Maximum Power Dissipation	P _D	T _C = 25 °C	6.1		5.2
		T _C = 70 °C	3.6		3.1
		T _A = 25 °C	3 ^{b, c}		3 ^{b, c}
		T _A = 70 °C	2.28 ^{b, c}	2.28 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150		°C	

THERMAL RESISTANCE RATINGS							
Parameter	Symbol	N-Channel		P-Channel		Unit	
		Typ.	Max.	Typ.	Max.		
Maximum Junction-to-Ambient ^{b, d}	R _{thJA}	20	32.5	27	32.5	°C/W	
Maximum Junction-to-Foot (Drain)	R _{thJF}	10	20	19	28		

Notes:

- Based on T_C = 25 °C.
- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- Maximum under steady state conditions is 120 °C/W (n-channel) and 110 °C/W (p-channel).
- Package limited.

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
Parameter	Symbol	Test Conditions	Min.	Typ. ^a	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	N-Ch	40		V	
		$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	P-Ch	-40			
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$	N-Ch		30	mV/ $^\circ\text{C}$	
		$I_D = -250\text{ }\mu\text{A}$	P-Ch		-24		
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250\text{ }\mu\text{A}$	N-Ch		-4.1		
		$I_D = -250\text{ }\mu\text{A}$	P-Ch		5		
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	N-Ch	1	2.2	V	
		$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	P-Ch	-0.9	-2.5		
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$	N-Ch		± 100	nA	
		$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$	P-Ch		± 100		
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}$	N-Ch		1	μA	
		$V_{DS} = -40\text{ V}, V_{GS} = 0\text{ V}$	P-Ch		-1		
		$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	N-Ch		10		
		$V_{DS} = -40\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	P-Ch		-10		
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} = 5\text{ V}, V_{GS} = 10\text{ V}$	N-Ch	30		A	
		$V_{DS} = -5\text{ V}, V_{GS} = -10\text{ V}$	P-Ch	-30			
Drain-Source On-State Resistance ^b	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 6.8\text{ A}$	N-Ch		0.015	Ω	
		$V_{GS} = -10\text{ V}, I_D = -8\text{ A}$	P-Ch		0.017		
		$V_{GS} = 8\text{ V}, I_D = 6.7\text{ A}$	N-Ch		0.016		
		$V_{GS} = -8\text{ V}, I_D = -6.5\text{ A}$	P-Ch		0.019		
		$V_{GS} = 4.5\text{ V}, I_D = 6.6\text{ A}$	N-Ch		0.018		
		$V_{GS} = -4.5\text{ V}, I_D = -5\text{ A}$	P-Ch		0.022		
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 6.8\text{ A}$	N-Ch		37	S	
		$V_{DS} = -15\text{ V}, I_D = -6.7\text{ A}$	P-Ch		35		
Dynamic^a							
Input Capacitance	C_{iss}	N-Channel $V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$ P-Channel $V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	N-Ch		1321	pF	
Output Capacitance	C_{oss}		P-Ch		1345		
			N-Ch		745		
Reverse Transfer Capacitance	C_{rss}		P-Ch		792		
			N-Ch		214		
Total Gate Charge	Q_g		$V_{DS} = 20\text{ V}, V_{GS} = 10\text{ V}, I_D = 10\text{ A}$	N-Ch			13.3
		$V_{DS} = -20\text{ V}, V_{GS} = -10\text{ V}, I_D = -10\text{ A}$	P-Ch		13	20	
Gate-Source Charge	Q_{gs}	N-Channel $V_{DS} = 20\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$	N-Ch		6.5	10	
			P-Ch		21.7	33	
Gate-Drain Charge	Q_{gd}	P-Channel $V_{DS} = -20\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -10\text{ A}$	N-Ch		2.3		
			P-Ch		5.6		
Gate Resistance	R_g	$f = 1\text{ MHz}$	N-Ch	0.3	1.3	2.6	
			P-Ch	1.3	6.4	12.8	

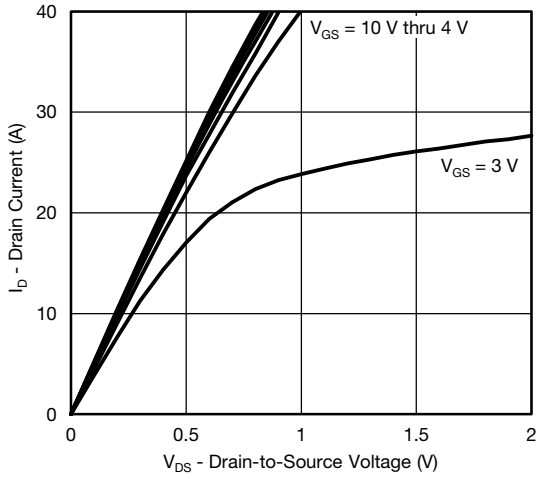
SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
Parameter	Symbol	Test Conditions	Min.	Typ. ^a	Max.	Unit	
Dynamic^a							
Turn-On Delay Time	t _{d(on)}	N-Channel V _{DD} = 20 V, R _L = 3.7 Ω I _D ≅ 5.4 A, V _{GEN} = 10 V, R _g = 1 Ω	N-Ch		5	10	ns
Rise Time	t _r		P-Ch		10	20	
Turn-Off Delay Time	t _{d(off)}	P-Channel V _{DD} = -20 V, R _L = 2 Ω I _D ≅ -10 A, V _{GEN} = -10 V, R _g = 1 Ω	N-Ch		16	25	
Fall Time	t _f		P-Ch		50	90	
Turn-On Delay Time	t _{d(on)}	N-Channel V _{DD} = 20 V, R _L = 3.7 Ω I _D ≅ 5.4 A, V _{GEN} = 4.5 V, R _g = 1 Ω	N-Ch		11	22	
Rise Time	t _r		P-Ch		42	75	
Turn-Off Delay Time	t _{d(off)}	P-Channel V _{DD} = -20 V, R _L = 2 Ω I _D ≅ -10 A, V _{GEN} = -4.5 V, R _g = 1 Ω	N-Ch		12	22	
Fall Time	t _f		P-Ch		40	70	
			N-Ch		17	26	
			P-Ch		40	70	
			N-Ch		7	14	
			P-Ch		18	35	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	N-Ch			5.6	A
			P-Ch			-5.6	
Pulse Diode Forward Current ^a	I _{SM}		N-Ch			40	A
			P-Ch			-40	
Body Diode Voltage	V _{SD}	I _S = 5.4 A	N-Ch		0.81	1.2	V
		I _S = -2 A	P-Ch		-0.77	-1.2	
Body Diode Reverse Recovery Time	t _{rr}	N-Channel I _F = 5 A, dI/dt = 100 A/μs, T _J = 25 °C	N-Ch		17	34	ns
			P-Ch		41	80	
Body Diode Reverse Recovery Charge	Q _{rr}	P-Channel I _F = -5 A, dI/dt = -100 A/μs, T _J = 25 °C	N-Ch		10	20	nC
			P-Ch		32	65	
Reverse Recovery Fall Time	t _a		N-Ch		10		ns
			P-Ch		15		
Reverse Recovery Rise Time	t _b		N-Ch		7		ns
			P-Ch		26		

Notes:

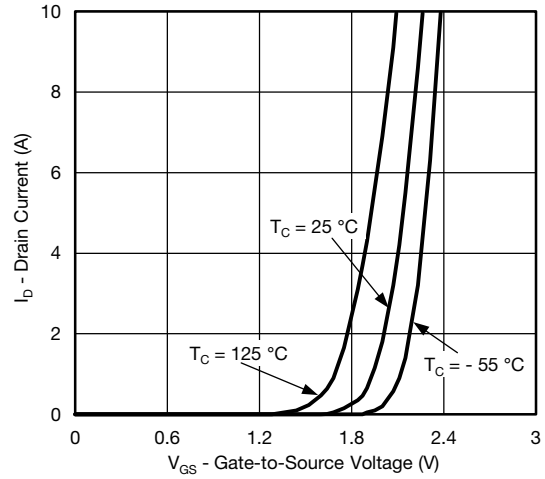
- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

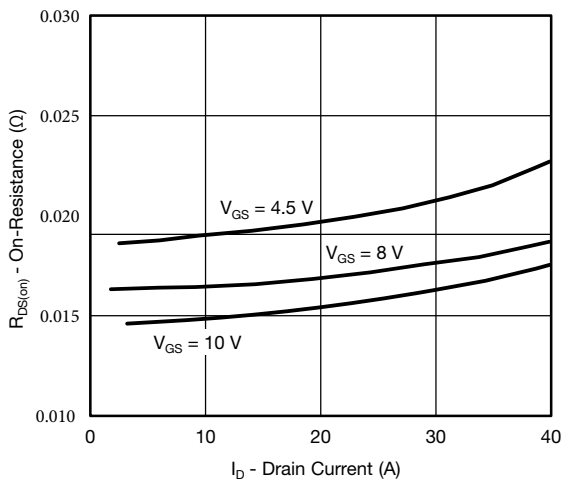
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



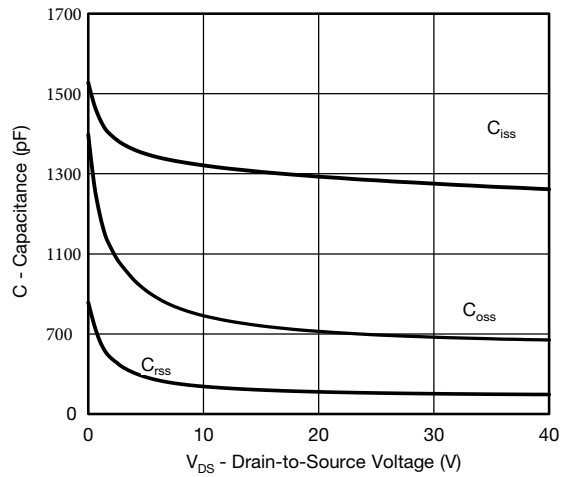
Output Characteristics



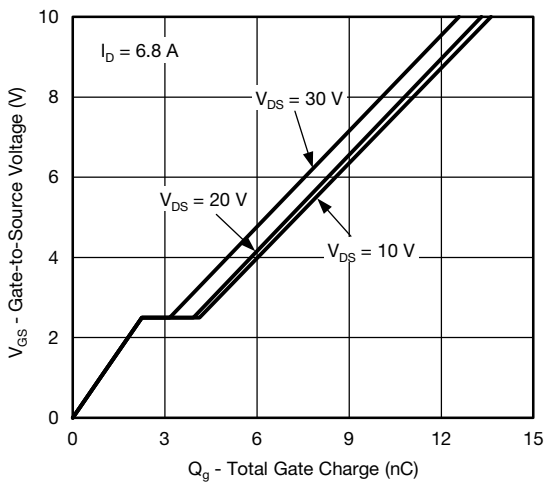
Transfer Characteristics



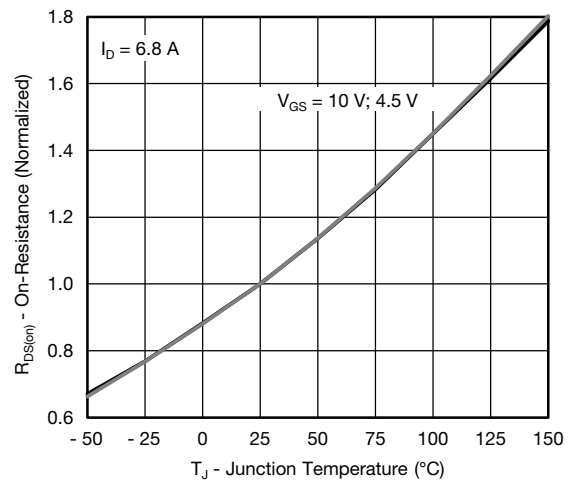
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

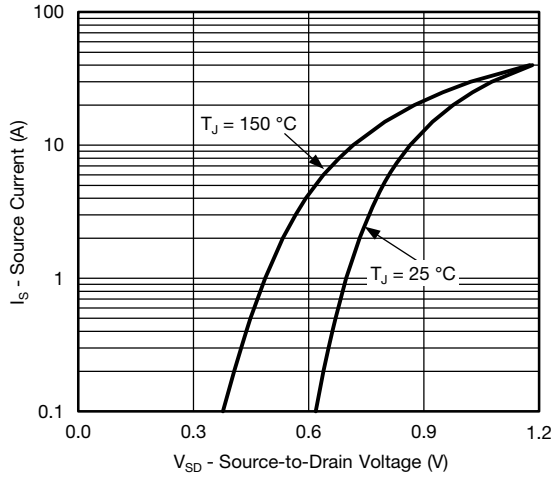


Gate Charge

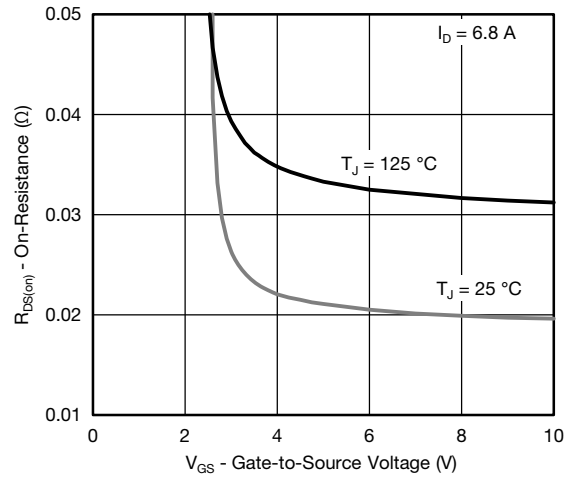


On-Resistance vs. Junction Temperature

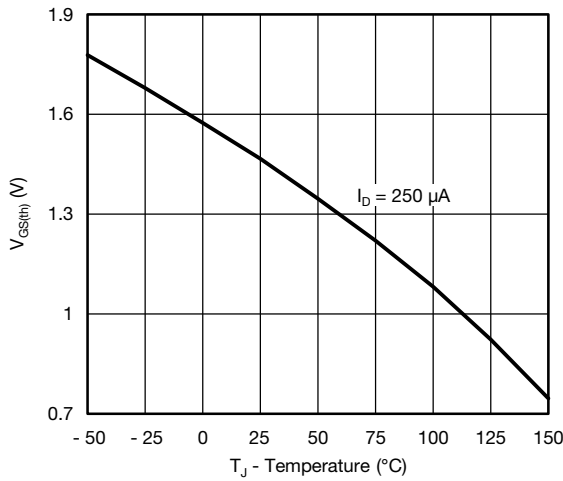
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



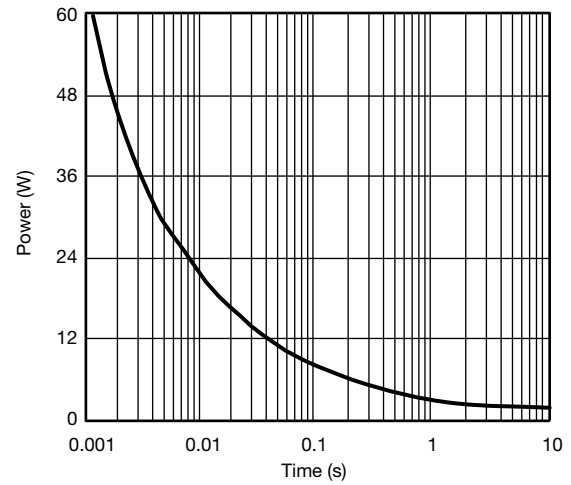
Source-Drain Diode Forward Voltage



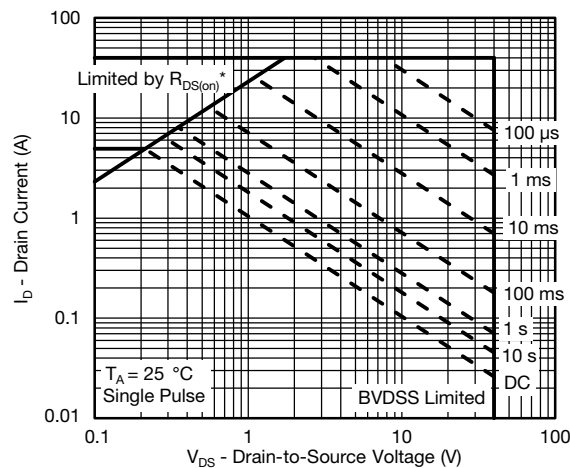
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

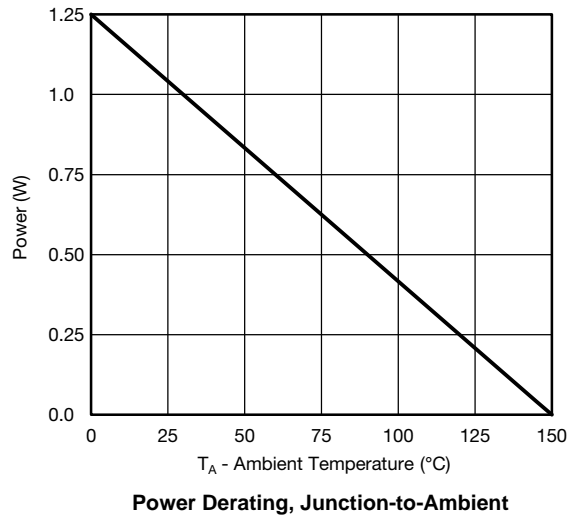
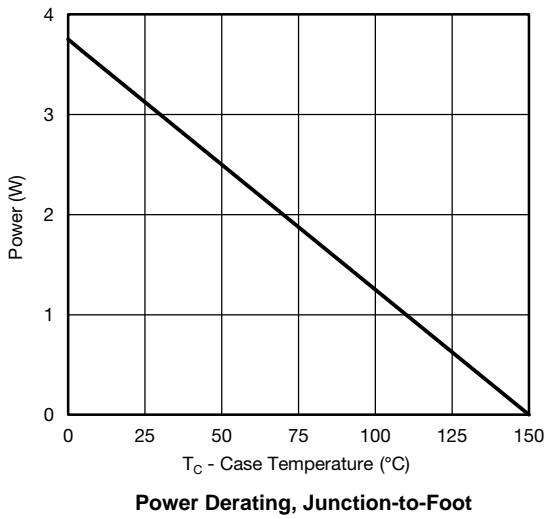
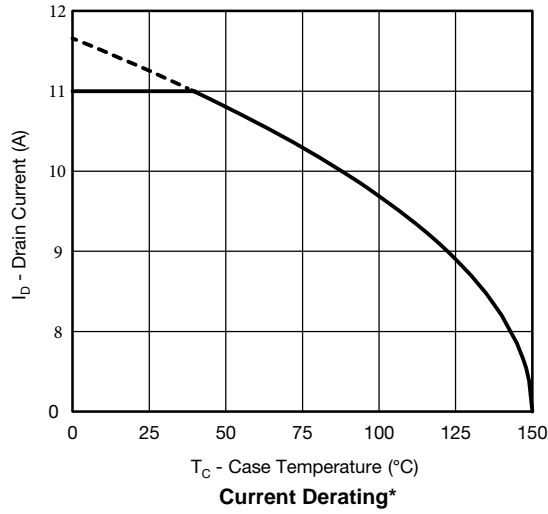


Single Pulse Power, Junction-to-Ambient



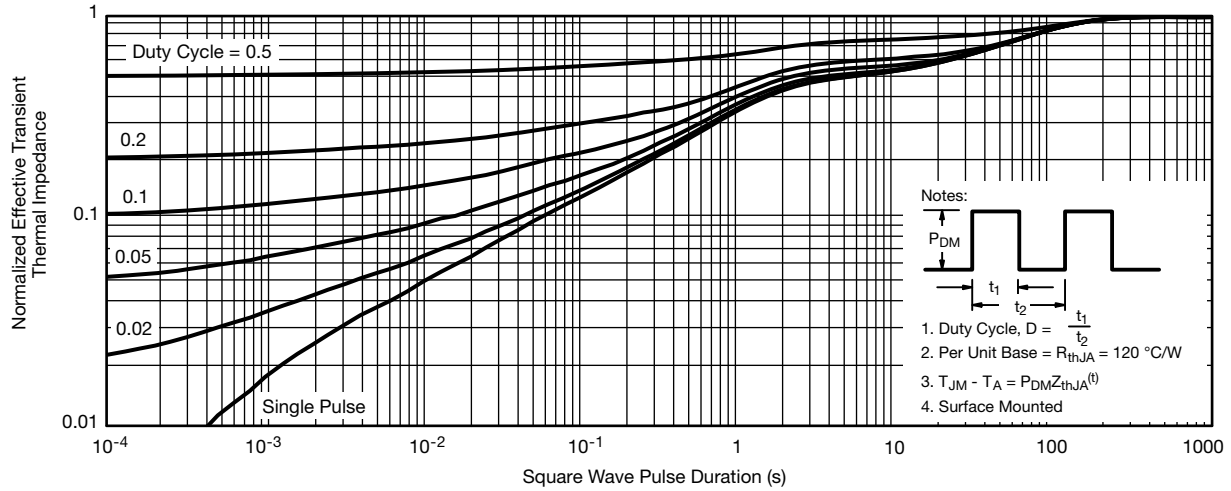
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified
Safe Operating Area, Junction-to-Ambient

N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

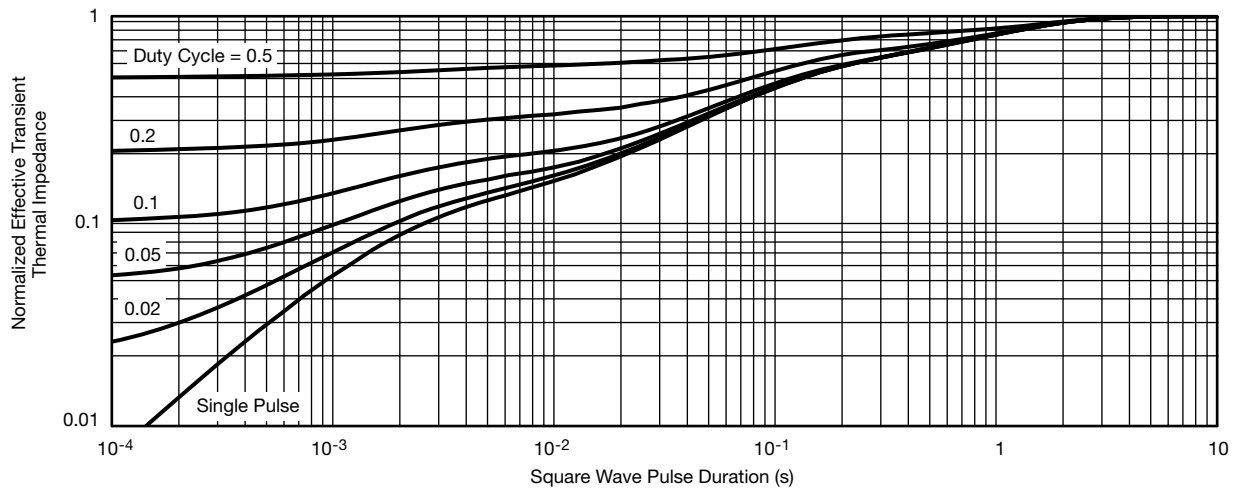


* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

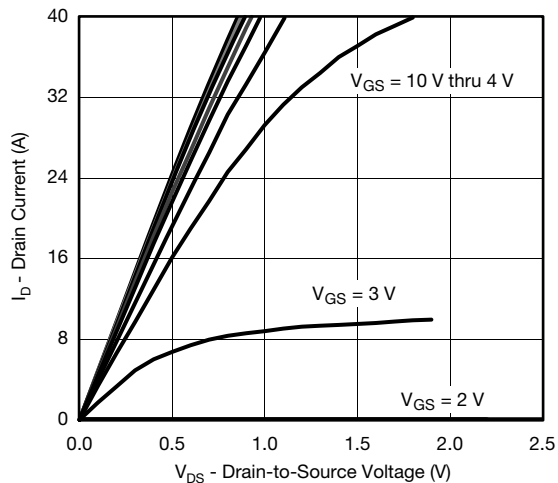


Normalized Thermal Transient Impedance, Junction-to-Ambient

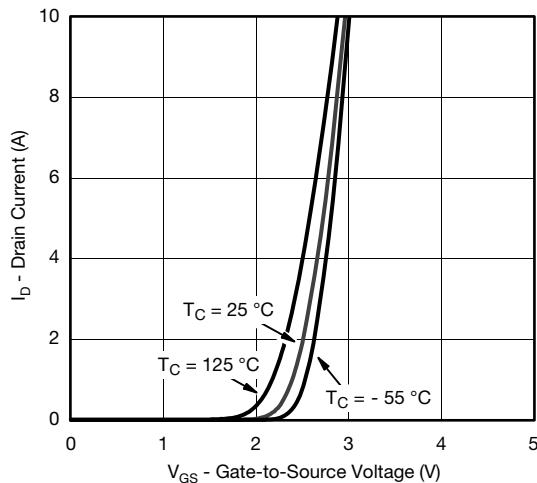


Normalized Thermal Transient Impedance, Junction-to-Foot

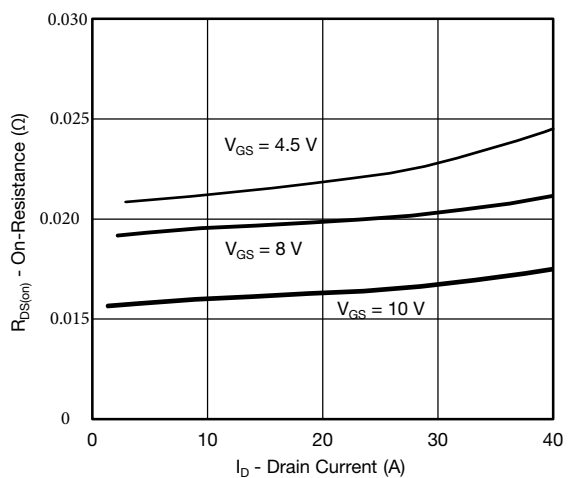
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



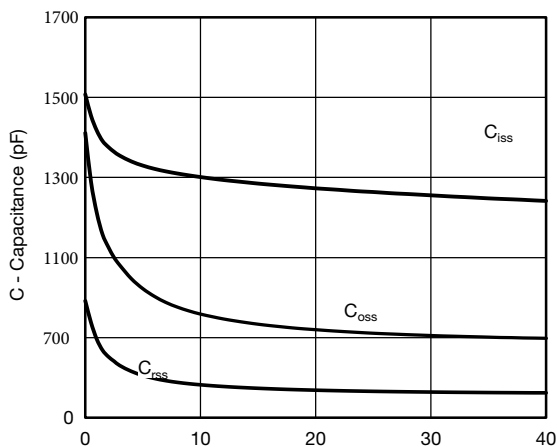
Output Characteristics



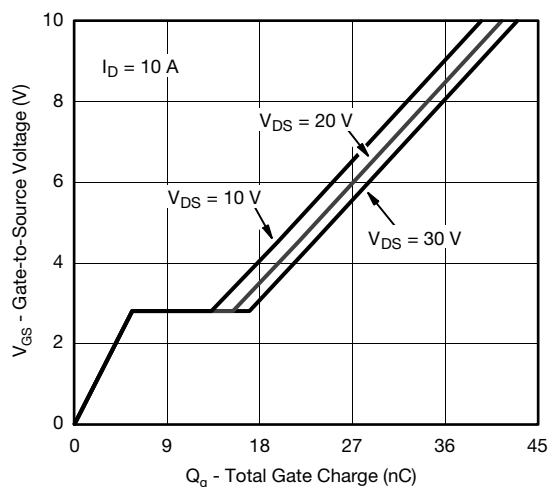
Transfer Characteristics



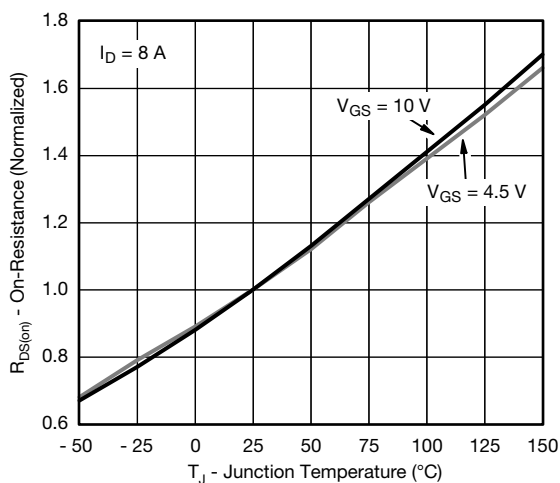
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

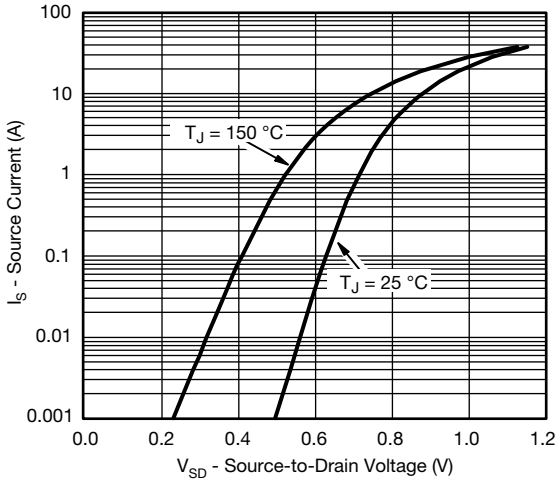


Gate Charge

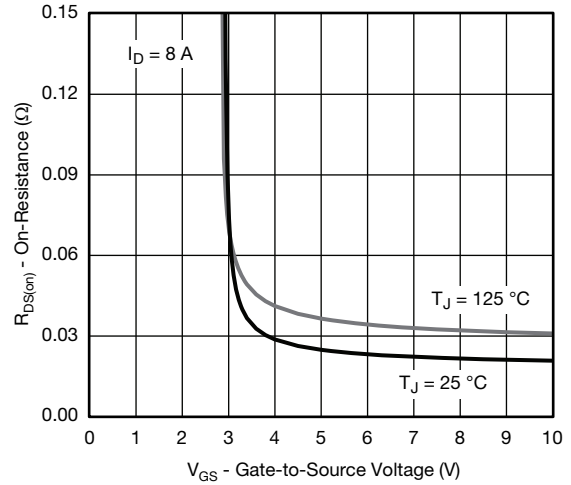


On-Resistance vs. Junction Temperature

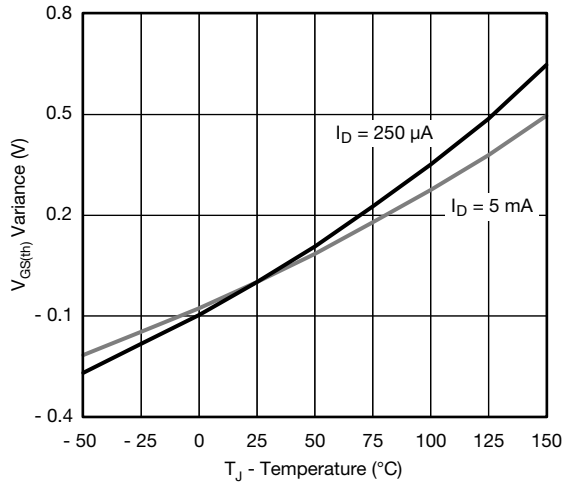
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



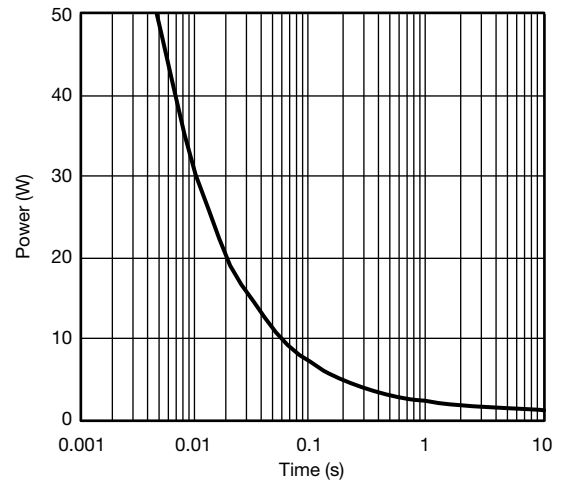
Source-Drain Diode Forward Voltage



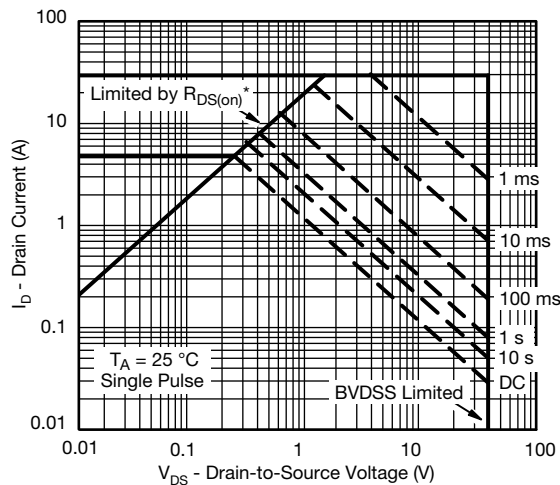
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

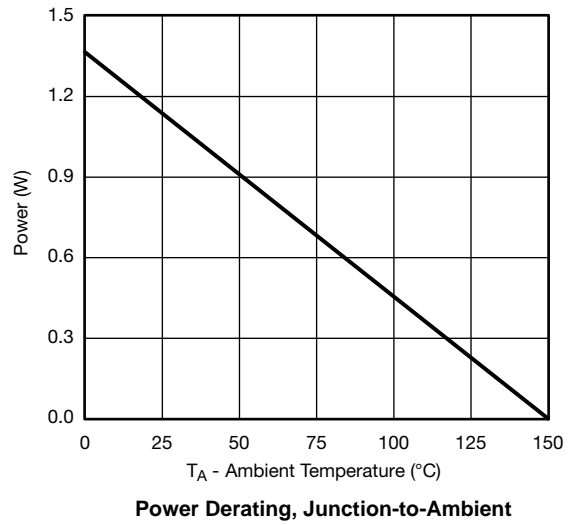
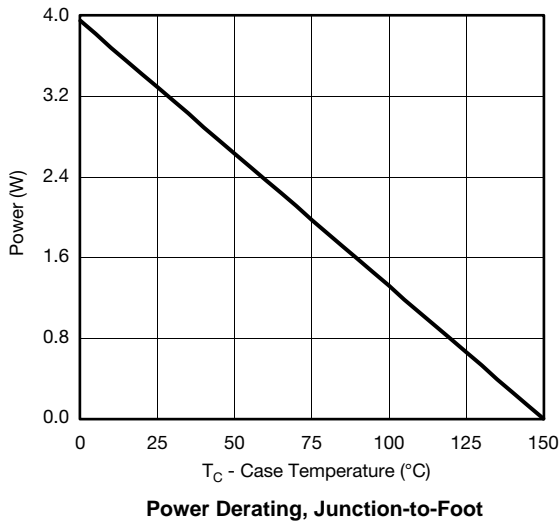
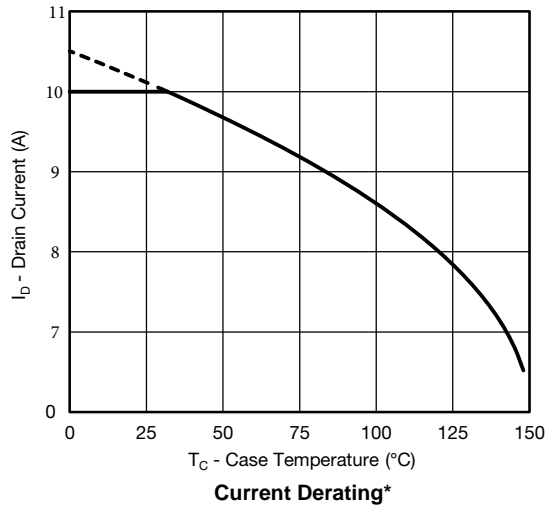


Single Pulse Power, Junction-to-Ambient



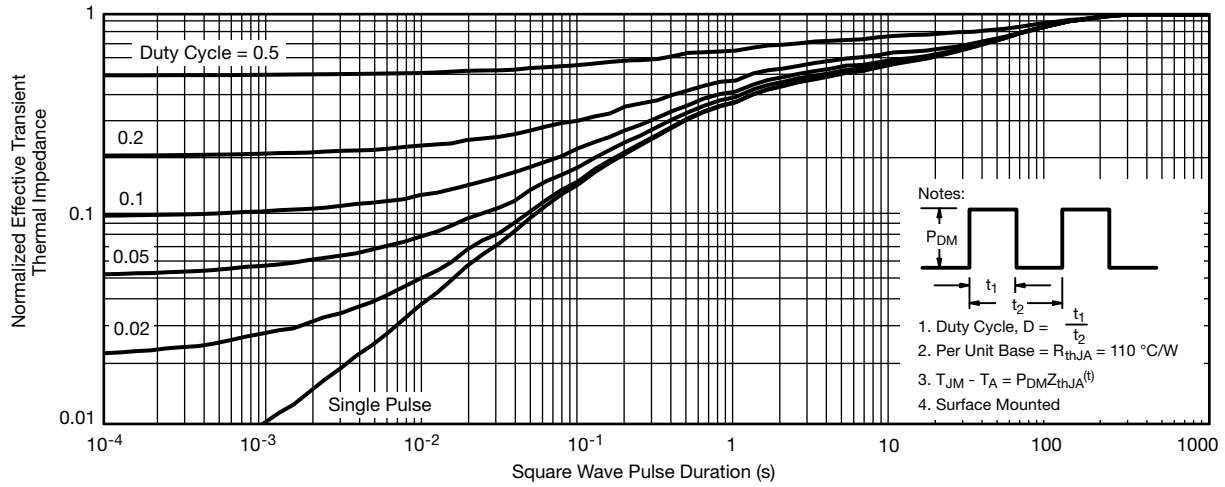
Safe Operating Area, Junction-to-Ambient

P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

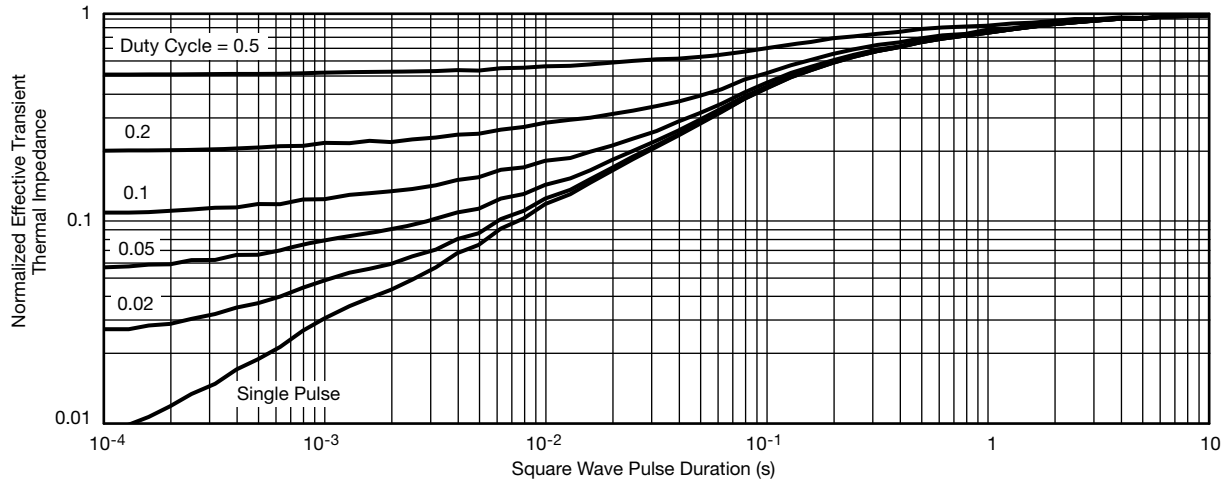


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P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



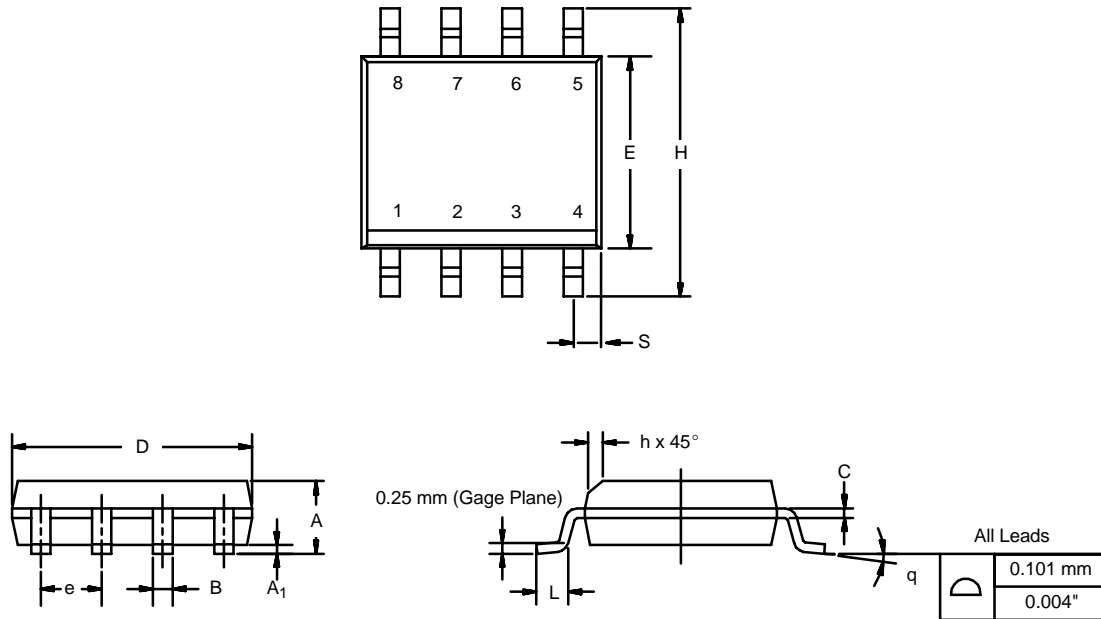
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

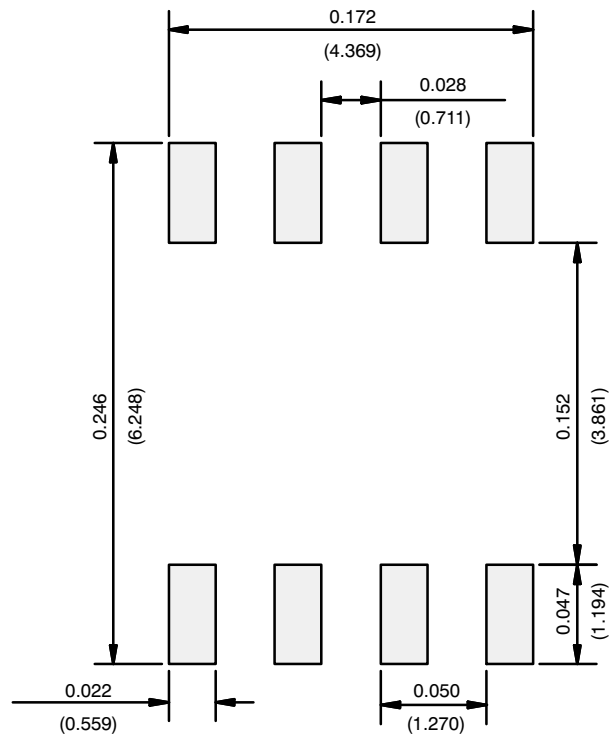
SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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Taiwan VBsemi Electronics Co., Ltd., hereby certify that all of the products are determined to be RoHS compliant and meets the definition of restrictions under Directive of the European Parliament 2011/65 / EU, 2011 Nian. 6. 8 Ri Yue restrict the use of certain hazardous substances in electrical and electronic equipment (EEE) - modification, unless otherwise specified as inconsistent.(www.VBsemi.com)

Please note that some documents may still refer to Taiwan VBsemi RoHS Directive 2002/95 / EC. We confirm that all products identified as consistent with the Directive 2002/95 / EC European Directive 2011/65 / .

Taiwan VBsemi Electronics Co., Ltd. hereby certify that all of its products comply identified as halogen-free halogen-free standards required by the JEDEC JS709A. Please note that some Taiwanese VBsemi documents still refer to the definition of IEC 61249-2-21, and we are sure that all products conform to confirm compliance with IEC 61249-2-21 standard level JS709A.