

## 4565M-VB Datasheet

### N- and P-Channel 60-V (D-S) MOSFET

PRODUCT SUMMARY				
	V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (Typ.)
N-Channel	60	0.026 at V <sub>GS</sub> = 10 V	5.3	6 nC
		0.029 at V <sub>GS</sub> = 4.5 V	4.7	
P-Channel	- 60	0.055 at V <sub>GS</sub> = - 10 V	- 4.9	8 nC
		0.060 at V <sub>GS</sub> = - 4.5 V	- 4.5	

#### FEATURES

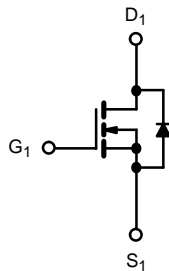
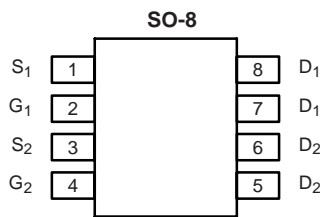
- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET<sup>®</sup> Power MOSFET
- 100 % R<sub>g</sub> and UIS Tested

#### APPLICATIONS

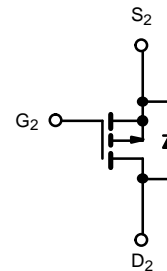
- CCFL Inverter



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**  
Available



N-Channel MOSFET



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T <sub>A</sub> = 25 °C, unless otherwise noted					
Parameter	Symbol	N-Channel	P-Channel	Unit	
Drain-Source Voltage	V <sub>DS</sub>	60	- 60	V	
Gate-Source Voltage	V <sub>GS</sub>	± 20			
Continuous Drain Current (T <sub>J</sub> = 150 °C)	I <sub>D</sub>	T <sub>C</sub> = 25 °C	5.3	- 4.9	A
		T <sub>C</sub> = 70 °C	4.3	- 4.2	
		T <sub>A</sub> = 25 °C	4.3 <sup>b, c</sup>	- 4.0 <sup>b, c</sup>	
		T <sub>A</sub> = 70 °C	3.4 <sup>b, c</sup>	- 3.4 <sup>b, c</sup>	
Pulsed Drain Current (10 μs Pulse Width)	I <sub>DM</sub>	20	- 25	A	
Source Drain Current Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	2.6		- 2.8
		T <sub>A</sub> = 25 °C	1.7 <sup>b, c</sup>		- 1.7 <sup>b, c</sup>
Pulsed Source-Drain Current	I <sub>SM</sub>	20	- 25	mJ	
Single Pulse Avalanche Current	I <sub>AS</sub>	11	15		
Single Pulse Avalanche Energy	E <sub>AS</sub>	6.1	11	W	
Maximum Power Dissipation	P <sub>D</sub>	T <sub>C</sub> = 25 °C	3.1		3.4
		T <sub>C</sub> = 70 °C	2		2.2
		T <sub>A</sub> = 25 °C	2 <sup>b, c</sup>		2 <sup>b, c</sup>
		T <sub>A</sub> = 70 °C	1.3 <sup>b, c</sup>	1.3 <sup>b, c</sup>	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150		°C	

THERMAL RESISTANCE RATINGS						
Parameter	Symbol	N-Channel		P-Channel		Unit
		Typ.	Max.	Typ.	Max.	
Maximum Junction-to-Ambient <sup>b, d</sup>	R <sub>thJA</sub>	55	62.5	53	62.5	°C/W
Maximum Junction-to-Foot (Drain)	R <sub>thJF</sub>	33	40	30	37	

Notes:

a. Based on T<sub>C</sub> = 25 °C.

b. Surface Mounted on 1" x 1" FR4 board.

c. t = 10 s.

d. Maximum under Steady State conditions is 110 °C/W for N-Channel and P-Channel.

<b>SPECIFICATIONS</b> $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted								
Parameter	Symbol	Test Conditions	Min.	Typ. <sup>a</sup>	Max.	Unit		
<b>Static</b>								
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	N-Ch	60			V	
		$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	P-Ch	-60				
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$	N-Ch		55		mV	
		$I_D = -250\text{ }\mu\text{A}$	P-Ch		-50			
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250\text{ }\mu\text{A}$	N-Ch		-6		mV	
		$I_D = -250\text{ }\mu\text{A}$	P-Ch		4			
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	N-Ch	1		3	V	
		$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	P-Ch	-1		-3		
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$	N-Ch			100	nA	
			P-Ch			-100		
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$	N-Ch			1	$\mu\text{A}$	
			P-Ch			-1		
		$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	N-Ch			10		
			P-Ch			-10		
On-State Drain Current <sup>b</sup>	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	N-Ch	20			A	
		$V_{DS} \leq -5\text{ V}, V_{GS} = -10\text{ V}$	P-Ch	-25				
Drain-Source On-State Resistance <sup>b</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 4.3\text{ A}$	N-Ch		0.026		$\Omega$	
		$V_{GS} = -10\text{ V}, I_D = -3.1\text{ A}$	P-Ch		0.055			
		$V_{GS} = 4.5\text{ V}, I_D = 3.9\text{ A}$	N-Ch		0.029			
		$V_{GS} = -4.5\text{ V}, I_D = -0.2\text{ A}$	P-Ch		0.060			
Forward Transconductance <sup>b</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}, I_D = 4.3\text{ A}$	N-Ch		15		S	
		$V_{DS} = -15\text{ V}, I_D = -3.1\text{ A}$	P-Ch		8.5			
<b>Dynamic<sup>a</sup></b>								
Input Capacitance	$C_{iss}$	N-Channel $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	N-Ch		665		$\mu\text{F}$	
			P-Ch		650			
Output Capacitance	$C_{oss}$		P-Channel $V_{DS} = -15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	N-Ch		75		
				P-Ch		95		
Reverse Transfer Capacitance	$C_{rss}$			N-Ch		40		
				P-Ch		60		
Total Gate Charge	$Q_g$		$V_{DS} = 30\text{ V}, V_{GS} = 10\text{ V}, I_D = 4.3\text{ A}$	N-Ch		13	20	nC
				P-Ch		14.5	22	
		$V_{DS} = 30\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 4.3\text{ A}$	N-Ch		6	9		
			P-Ch		8	12		
Gate-Source Charge	$Q_{gs}$	$V_{DS} = -30\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -3.1\text{ A}$	N-Ch		2.3			
Gate-Drain Charge	$Q_{gd}$		P-Ch		2.2			
			N-Ch		2.6			
P-Ch			3.7					
Gate Resistance	$R_g$	$f = 1\text{ MHz}$	N-Ch		2	3	$\Omega$	
			P-Ch		14	20		

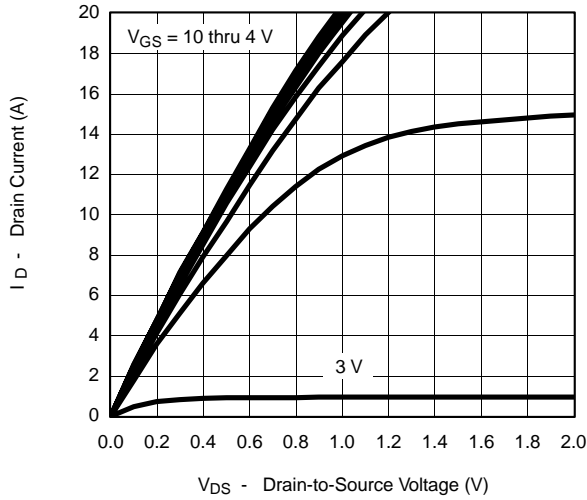
<b>SPECIFICATIONS</b> $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Typ. <sup>a</sup>	Max.	Unit	
<b>Dynamic<sup>a</sup></b>							
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 30\text{ V}$ , $R_L = 8.8\ \Omega$ $I_D \cong 3.4\text{ A}$ , $V_{GEN} = 4.5\text{ V}$ , $R_g = 1\ \Omega$	N-Ch		15	25	ns
Rise Time	$t_r$		P-Ch		30	45	
Turn-Off Delay Time	$t_{d(off)}$	P-Channel $V_{DD} = -30\text{ V}$ , $R_L = 12.5\ \Omega$ $I_D \cong -2.4\text{ A}$ , $V_{GEN} = -4.5\text{ V}$ , $R_g = 1\ \Omega$	N-Ch		65	100	
			P-Ch		70	105	
Fall Time	$t_f$		N-Ch		15	25	
			P-Ch		40	60	
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 30\text{ V}$ , $R_L = 8.8\ \Omega$ $I_D \cong 3.4\text{ A}$ , $V_{GEN} = 10\text{ V}$ , $R_g = 1\ \Omega$	N-Ch		10	15	
			P-Ch		10	15	
Rise Time	$t_r$		N-Ch		15	25	
			P-Ch		13	20	
Turn-Off Delay Time	$t_{d(off)}$	P-Channel $V_{DD} = -30\text{ V}$ , $R_L = 12.5\ \Omega$ $I_D \cong -2.4\text{ A}$ , $V_{GEN} = -10\text{ V}$ , $R_g = 1\ \Omega$	N-Ch		20	30	
			P-Ch		35	55	
Fall Time	$t_f$		N-Ch		10	15	
			P-Ch		30	45	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$	N-Ch			2.6	A
			P-Ch			-2.8	
Pulse Diode Forward Current <sup>a</sup>	$I_{SM}$		N-Ch			20	
			P-Ch			-25	
Body Diode Voltage	$V_{SD}$	$I_S = 1.7\text{ A}$	N-Ch		0.8	1.2	V
		$I_S = -2\text{ A}$	P-Ch		-0.8	-1.2	
Body Diode Reverse Recovery Time	$t_{rr}$	N-Channel $I_F = 1.7\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $T_J = 25\text{ }^\circ\text{C}$	N-Ch		30	60	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$		P-Ch		30	50	
Reverse Recovery Fall Time	$t_a$	P-Channel $I_F = -2\text{ A}$ , $di/dt = -100\text{ A}/\mu\text{s}$ , $T_J = 25\text{ }^\circ\text{C}$	N-Ch		32	50	nC
			P-Ch		35	60	
Reverse Recovery Rise Time	$t_b$		N-Ch		25		ns
			P-Ch		16		
			N-Ch		5		
			P-Ch		14		

Notes:

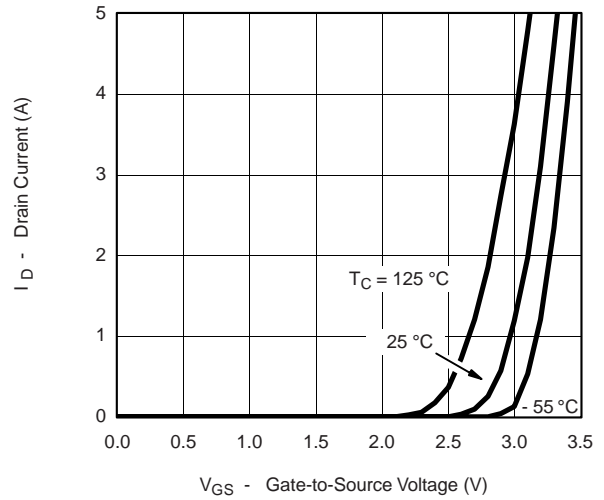
- a. Guaranteed by design, not subject to production testing.  
 b. Pulse test; pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

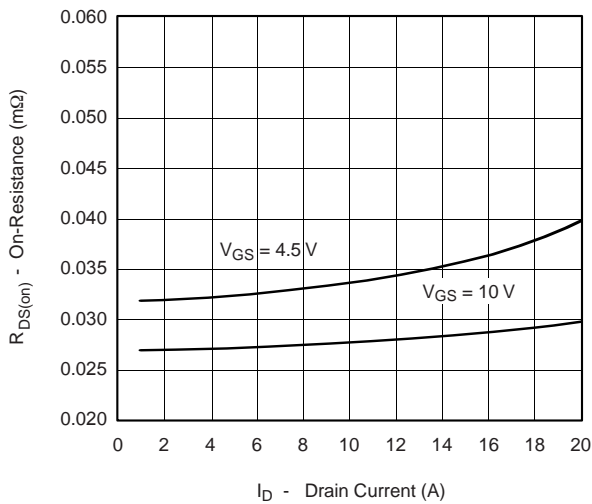
**N-CHANNEL TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



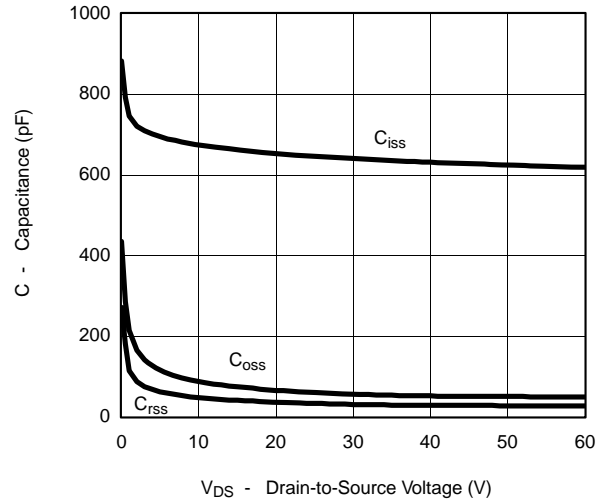
**Output Characteristics**



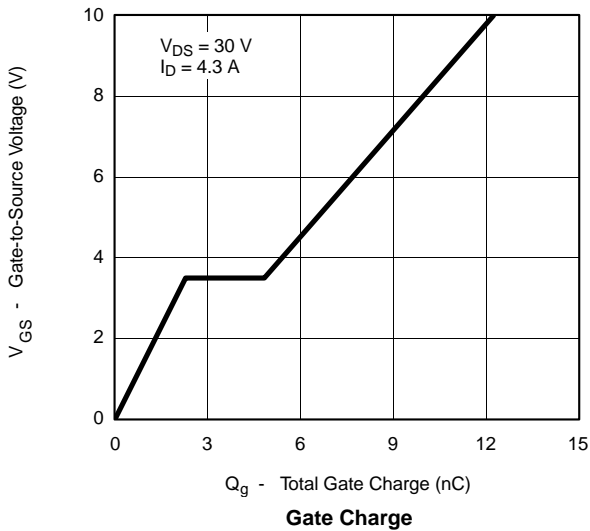
**Transfer Characteristics**



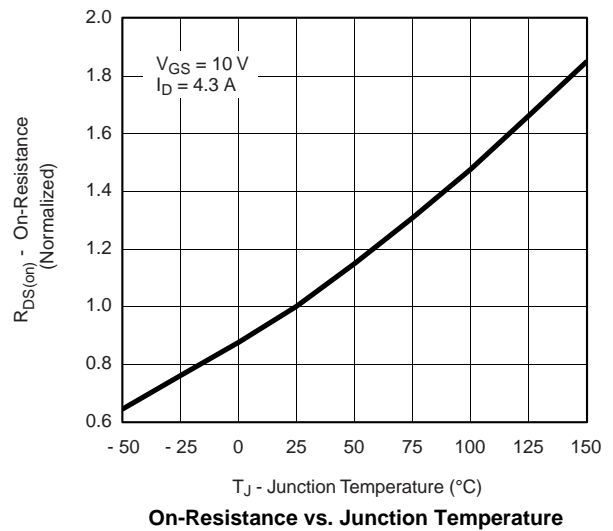
**On-Resistance vs. Drain Current and Gate Voltage**



**Capacitance**

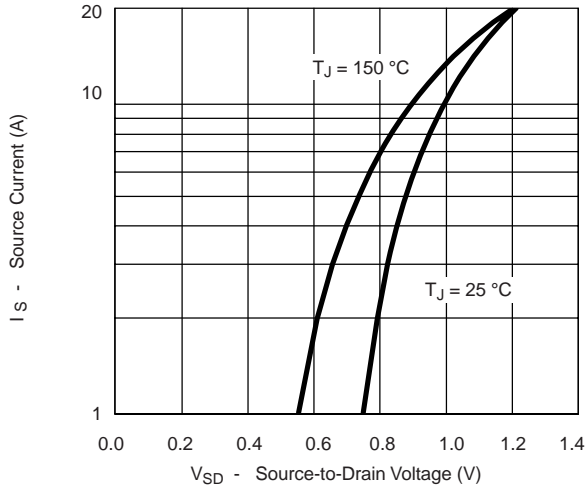


**Gate Charge**

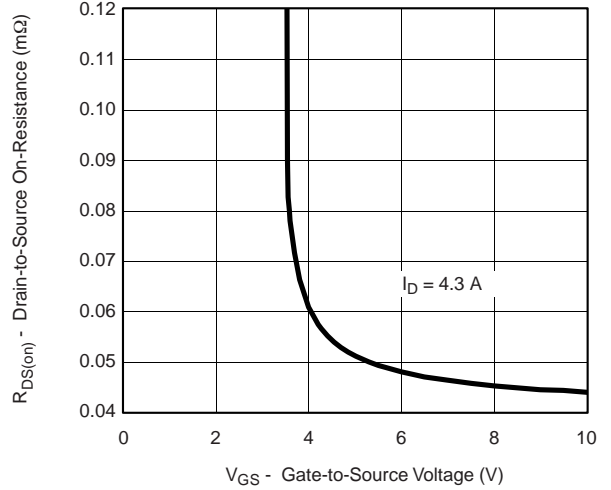


**On-Resistance vs. Junction Temperature**

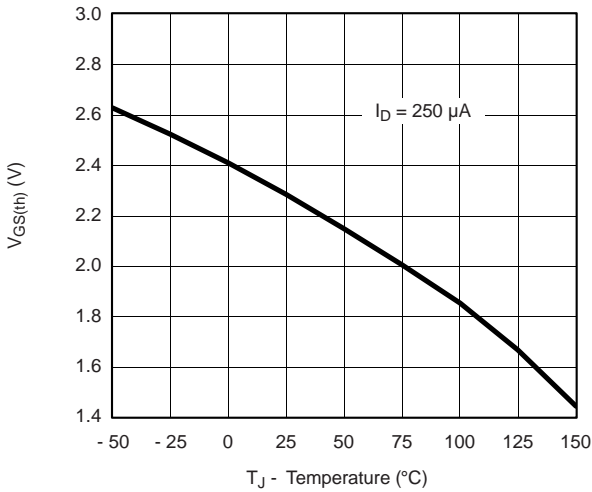
**N-CHANNEL TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



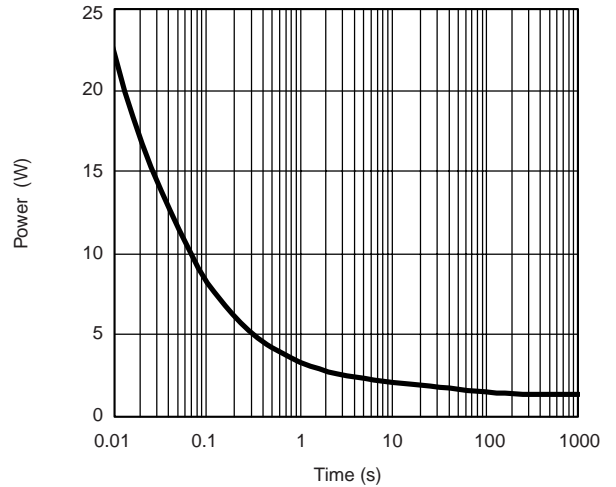
**Source-Drain Diode Forward Voltage**



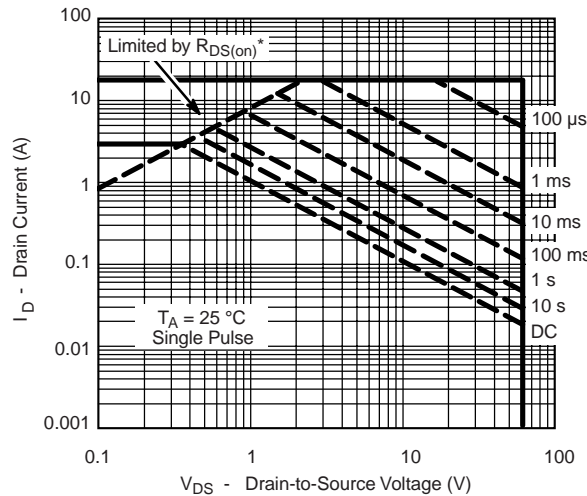
**On-Resistance vs. Gate-to-Source Voltage**



**Threshold Voltage**



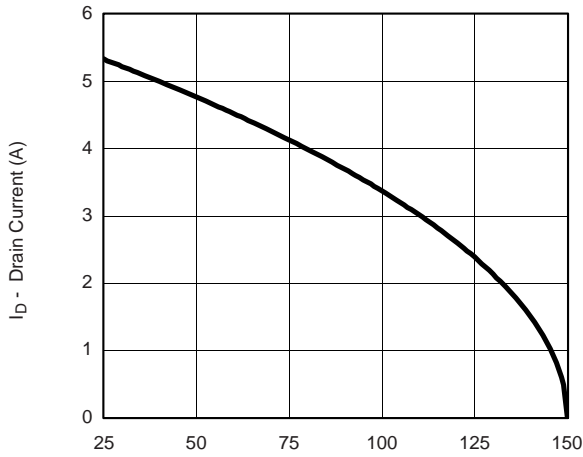
**Single Pulse Power, Junction-to-Ambient**



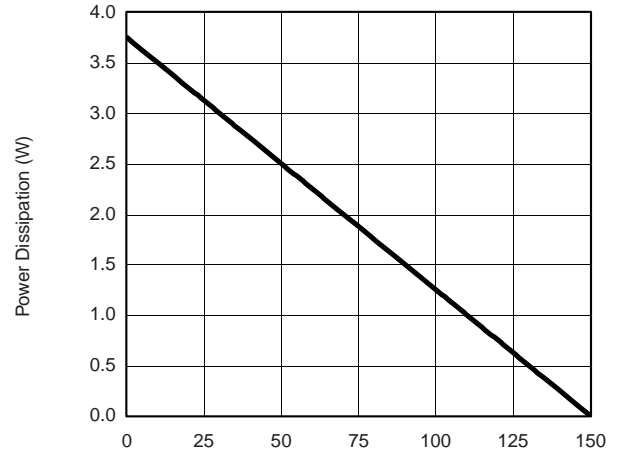
\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

**Safe Operating Area**

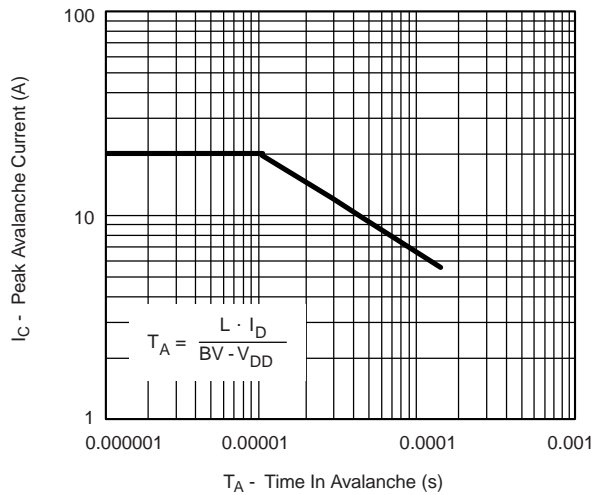
**N-CHANNEL TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



T<sub>C</sub> - Case Temperature (°C)  
**Current Derating\***



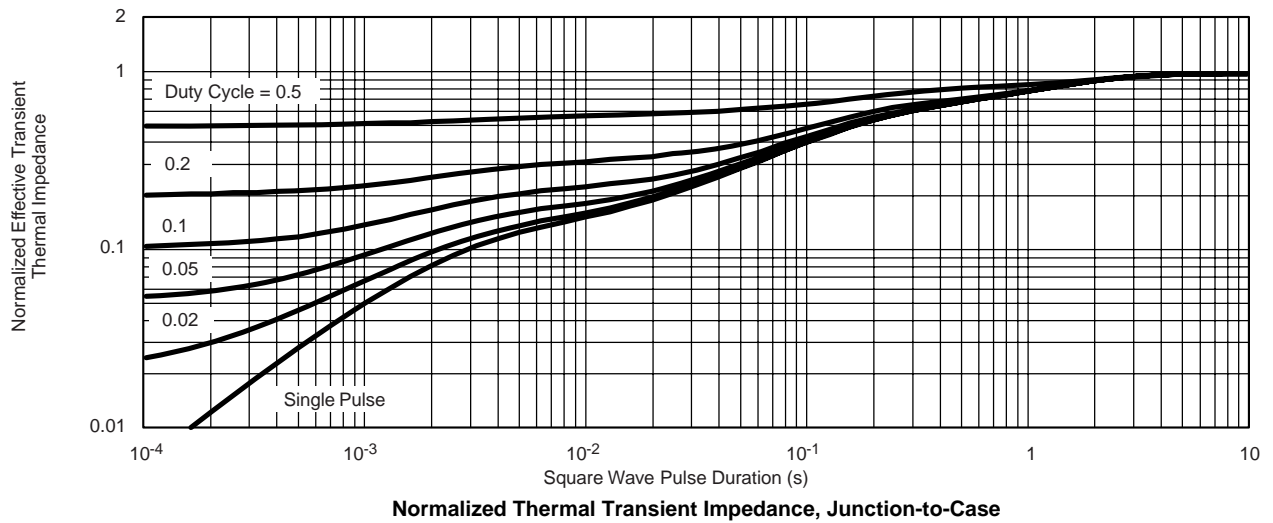
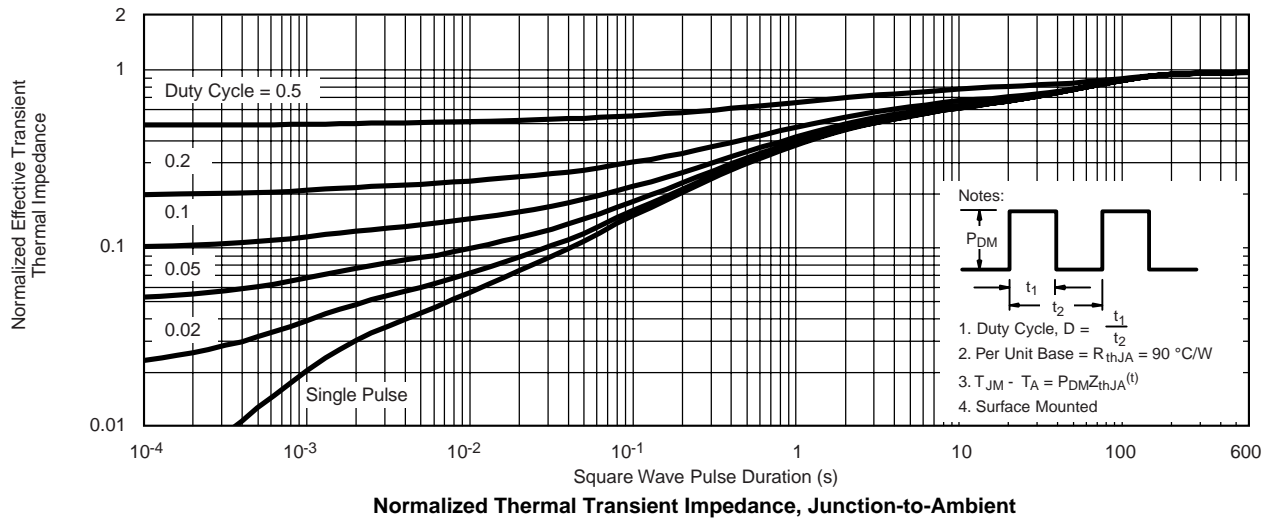
T<sub>C</sub> - Case Temperature (°C)  
**Power Derating**



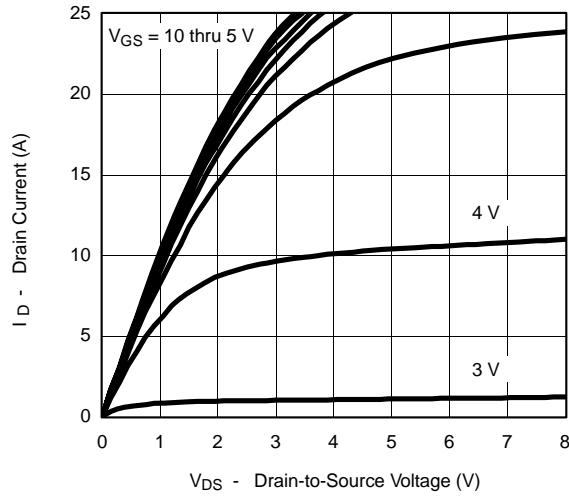
**Single Pulse Avalanche Capability**

\* The power dissipation P<sub>D</sub> is based on T<sub>J(max)</sub> = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

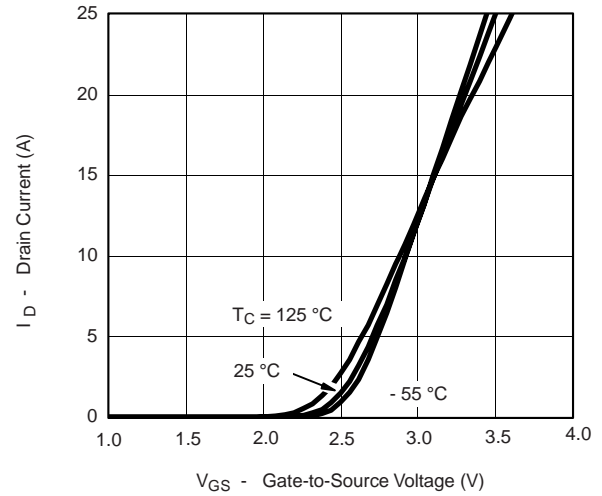
**N-CHANNEL TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



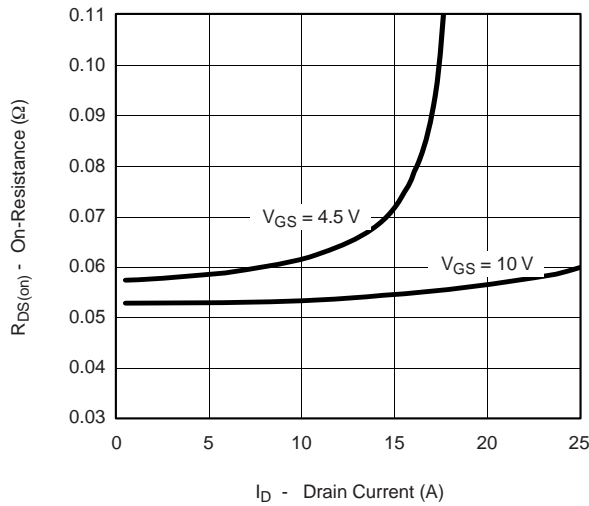
**P-CHANNEL TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



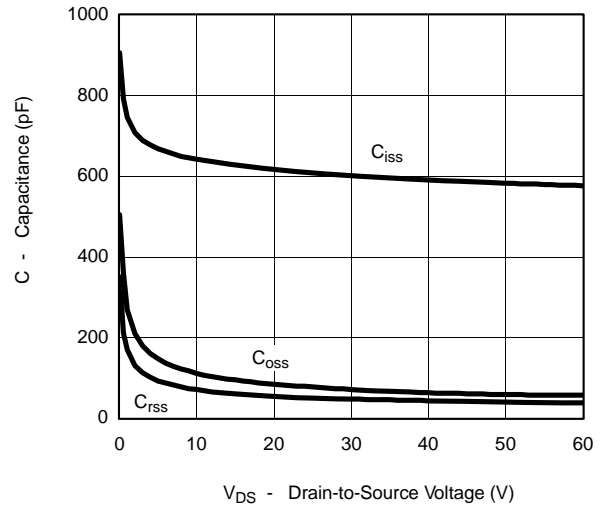
**Output Characteristics**



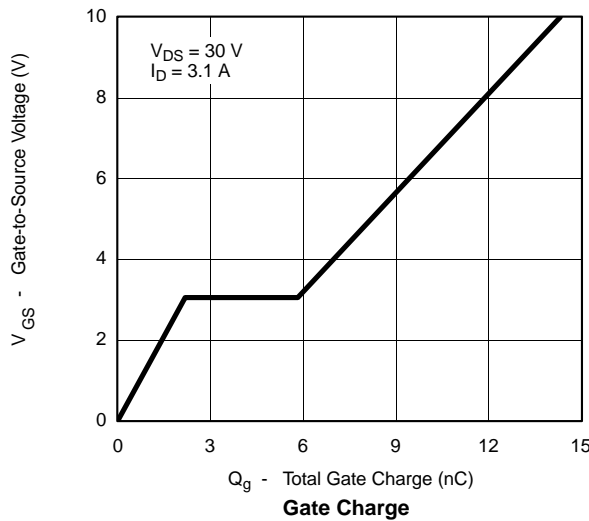
**Transfer Characteristics**



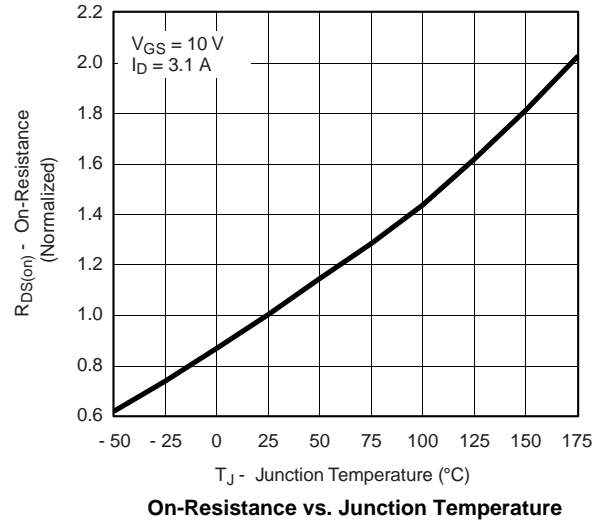
**On-Resistance vs. Drain Current**



**Capacitance**



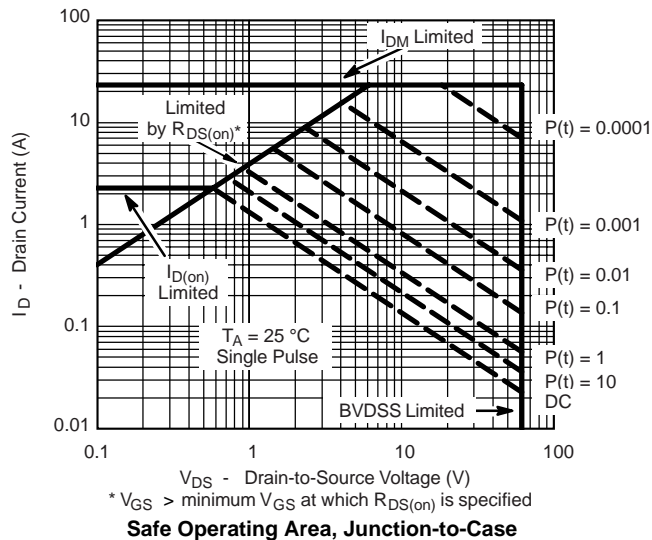
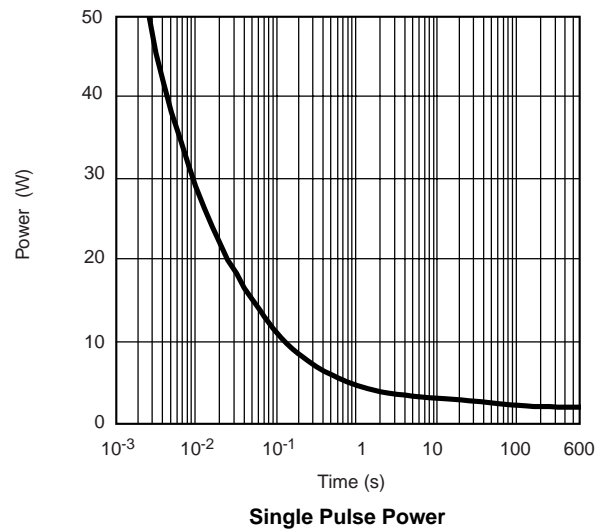
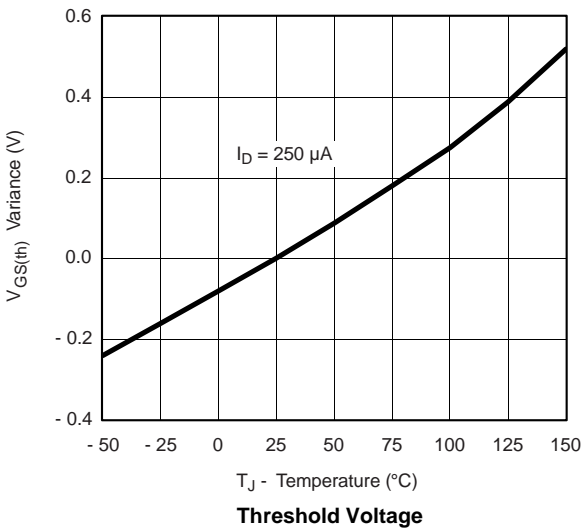
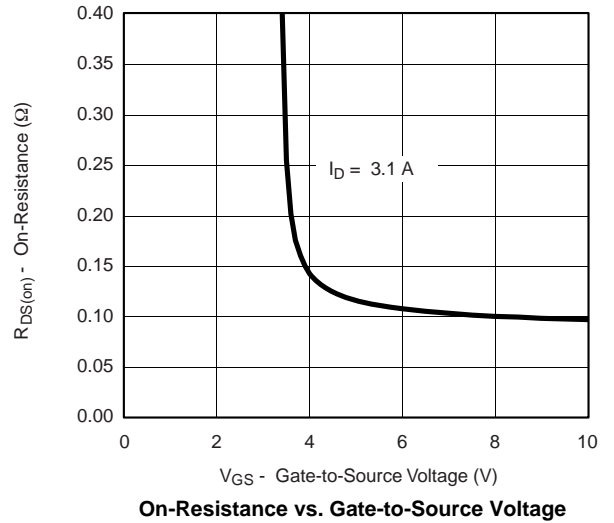
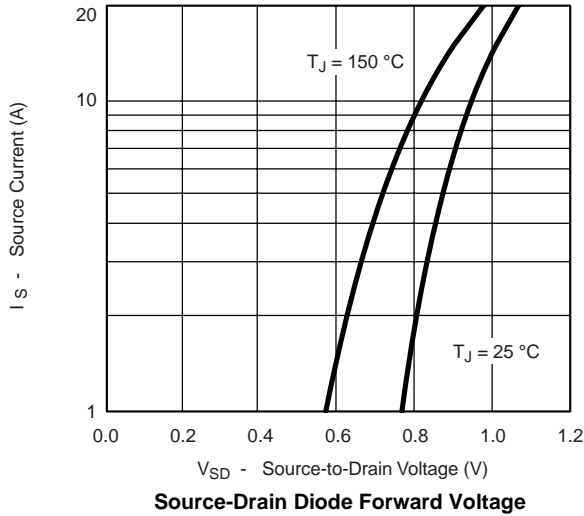
**Gate Charge**



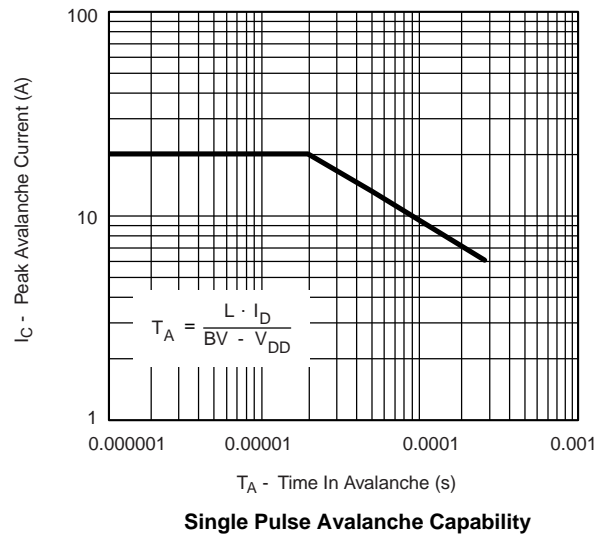
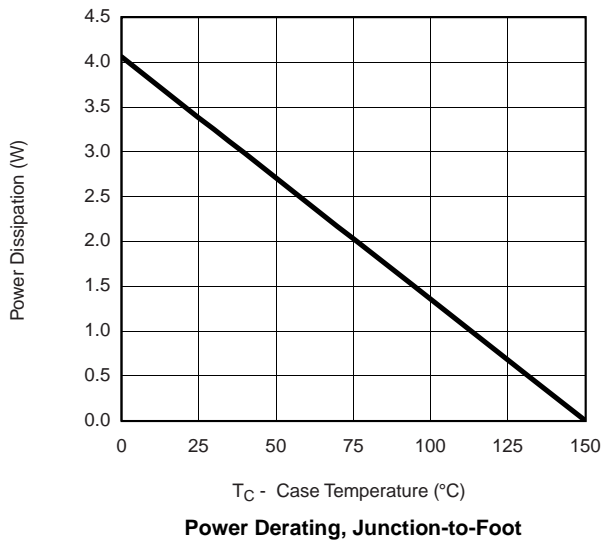
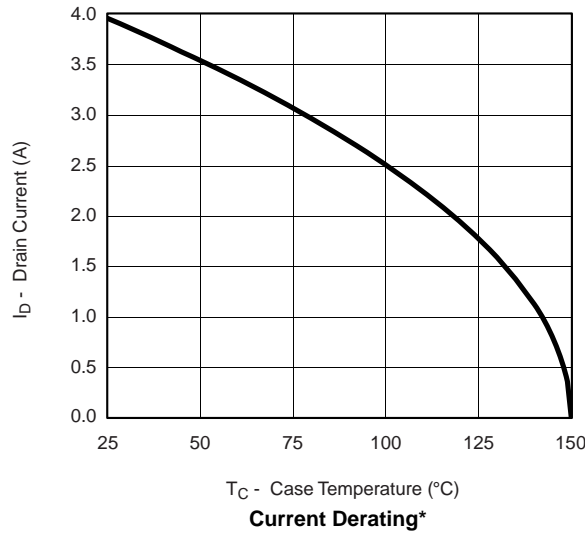
**On-Resistance vs. Junction Temperature**



**P-CHANNEL TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

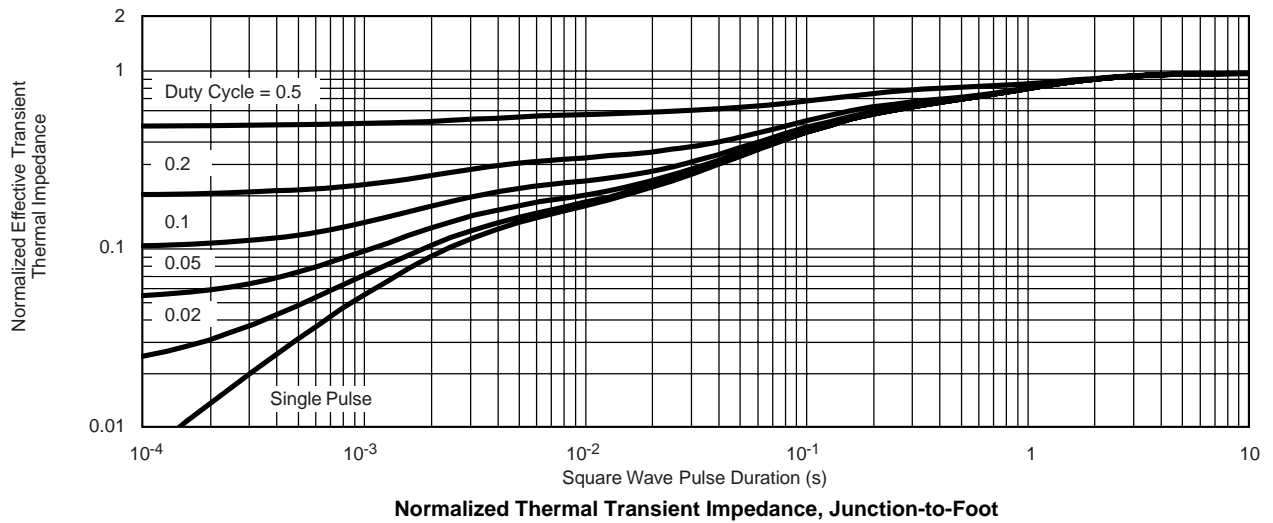
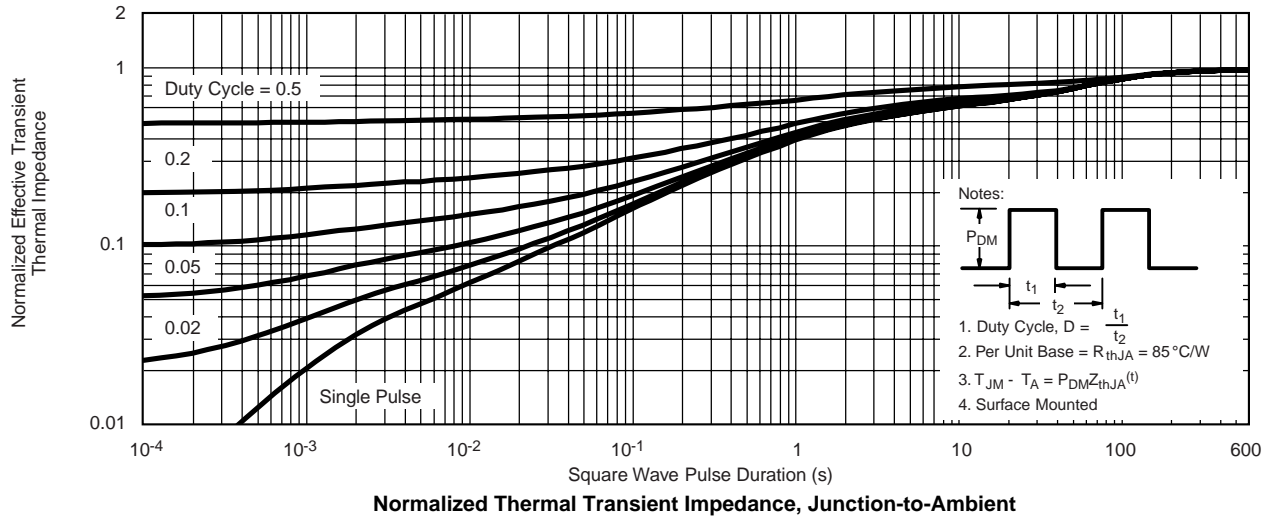


**P-CHANNEL TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



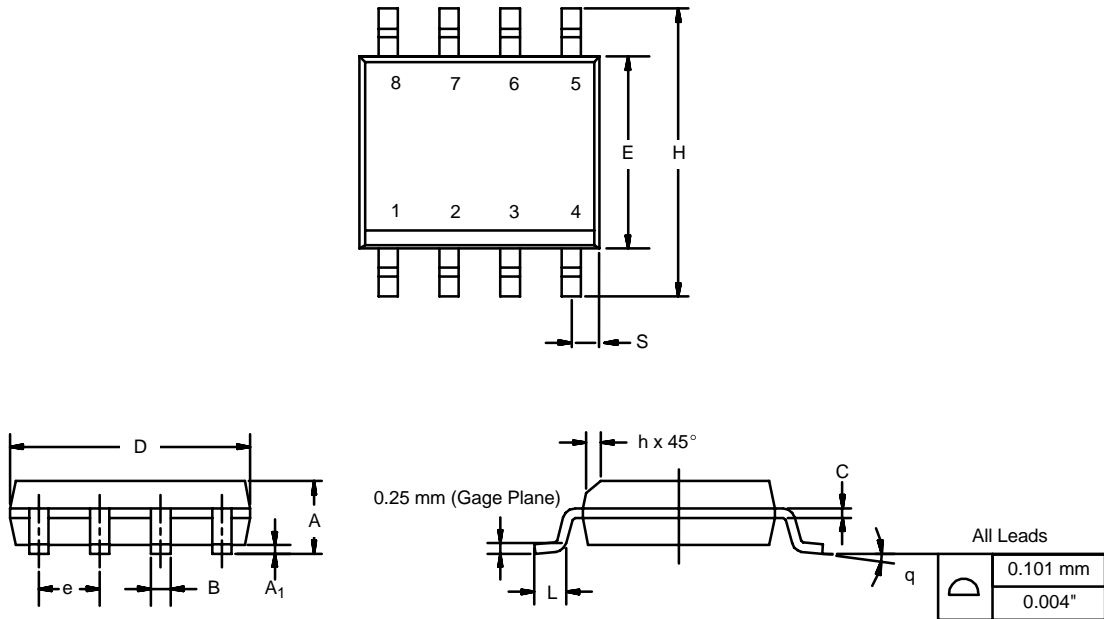
\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**P-CHANNEL TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



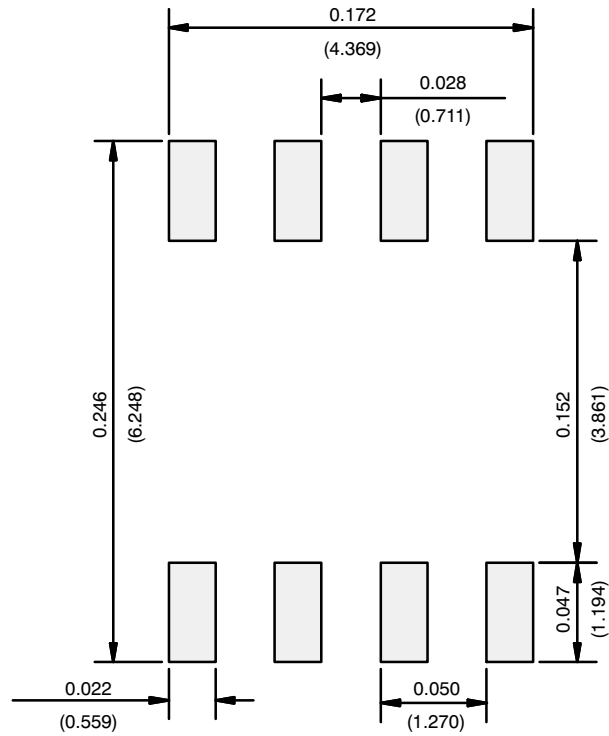
**SOIC (NARROW): 8-LEAD**

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A <sub>1</sub>	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads  
Dimensions in Inches/(mm)

# Disclaimer

All products due to improve reliability, function or design or for other reasons, product specifications and data are subject to change without notice.

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**Please note that some documents may still refer to Taiwan VBsemi RoHS Directive 2002/95 / EC. We confirm that all products identified as consistent with the Directive 2002/95 / EC European Directive 2011/65 / .**

**Taiwan VBsemi Electronics Co., Ltd. hereby certify that all of its products comply identified as halogen-free halogen-free standards required by the JEDEC JS709A. Please note that some Taiwanese VBsemi documents still refer to the definition of IEC 61249-2-21, and we are sure that all products conform to confirm compliance with IEC 61249-2-21 standard level JS709A.**